Design of low power 4-bit shift registers using conditionally pulse enhanced pulse triggered flip-flop

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Abstract: *The choice of flip-flop technologies is an essential importance in design of VLSI integrated circuits for high speed and high performance CMOS circuits. The main objective of the papert is to design a Low-Power Pulse-Triggered flip-flop. Flip-flops are the major storage elements in all SOC's of digital design. They accommodate most of the power that has been applied to the chip. Flip-flop is one of the most power consumption components. It is important to reduce the power dissipation in both clock distribution networks and flip-flops.*

The proposed low-power implicit-type P-FF design features a conditional pulse-enhancement scheme. First, the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Low power 4-bit shift registers are implemented using the proposed low power pulse triggered flip-flop with conditional pulse enhancement scheme.

Keywords: *IP-DCO, MHLFF,SCCER, SISO, SIPO, PIPO, PISO.*

I. Introduction

Basics of flip-flops

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. One latch or Flip-Flop can store one bit of information. Flip-flops, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even. Transitions on the inputs of a flip-flop may or may not lead to a state change. When input transitions do not change the state, the internal switching inside the flip-flop consumes some power. On the other hand, when the input transitions do change the state, a large amount of power is consumed. There are number of flip-flops. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations.

Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based flip-flop in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system.
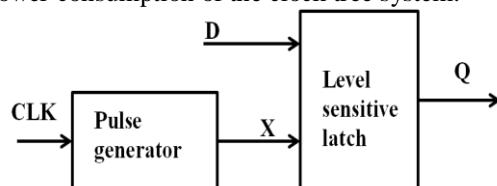
Fig 1. Block diagram of a pulse triggered Flip-flop

A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter.

Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network.

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Explicit-type P-FF designs face a pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

The paper comprises of the following sections: section II describes some of the conventional pulse triggered flip-flop designs and their disadvantages, section III discusses about a new pulse triggered flip-flop design overcoming the above disadvantages. Section IV comprises of shift registers as an application of the flip-flops.

II. Conventional Implicit Flip-Flop Designs
Implicit pulsed-Data Close to Output (IP-DCO) flip-flop
The circuit diagram of IP-DCO is shown in the Figure 2. In IP-DCO the clock signal and complement of the clock signal generates a narrow pulse of short pulse width [9].
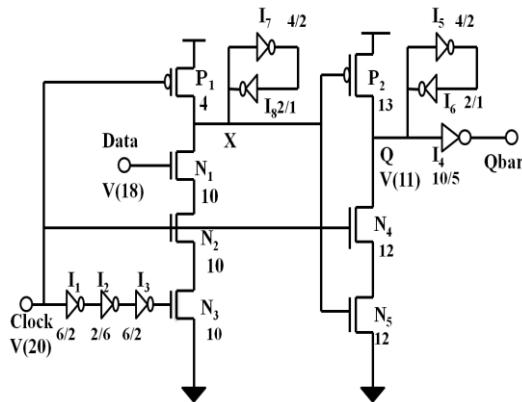
Fig. 2. Circuit Diagram of IP-DCO Flip-Flop.

During this pulse the output follows the input. First, during the rising edge, NMOS transistor s N2 and N3 are turned on. If data remains high, node x will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node x controls two larger MOS transistors (P2 and N5). The large capacitive load to node 'x' causes speed and power performance degradation. When the x as denoted floating node, The node x controls two larger transistors P2 and N5, this leads to large capacitive load to node x causes power performance degradation. The Implicit pulsed Data Close to Output flip-flop [9] contains an AND logic-based pulse generator and a semi dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3.

Modified Hybrid Latch Flip-flop (MHLFF)
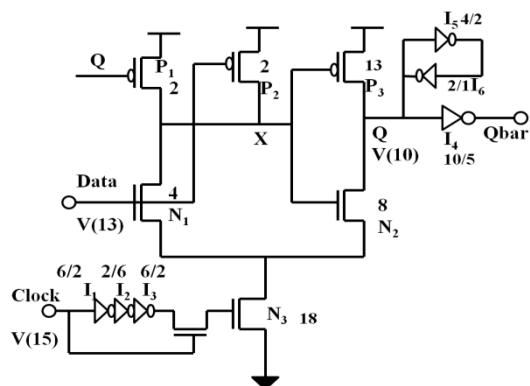
Fig. 3 Circuit diagram of Modified Hybrid Latch Flip-flop.

 The Modified Version of Hybrid Latch Flip-Flop also falls under the hybrid category of flip flop that has impressive delay property and can have negative setup time with brief transparency period. The modified hybrid latch flip-flop shown in fig. 3 is modified version of HLFF flip flop that has Lower number of transistors as well as less power consumption. It is by employing a static latch structure. Node X is no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the flip-flop output signal Q is used to maintain the node X level at high when Q is zero and which eliminates the unnecessary discharging problems at the node X.

Single Ended Conditional Capture Energy Recovery(SCCER) flip-flop

SCCER [5] is a design which is a modification over the ip-DCO design. In this design, the back to back inverters which are used instead of pull up and pull down resistors is replaced by a weak pull up transistor P1 and inverter to reduce the load capacitance of node. The series connection of two NMOS transistors N1 and N2 is used in the discharge path. An extra NMOS transistor N3 is used to eliminate the unwanted switching activity.

Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The timing of this design occurs when input data is "1" transistors in series, N1 through N4, while combating with the pull up transistor P1.
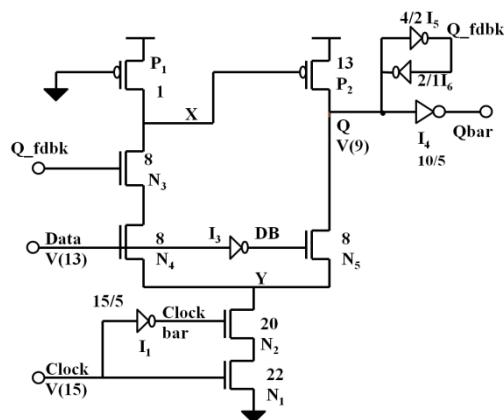
Fig. 4 Circuit Diagram of SCCER Flip-flop.

A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

III.   Proposed Flip-Flop

The proposed design, as shown in Fig. 5, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 4, the upper part latch design is similar to the one employed in SCCER design[5].
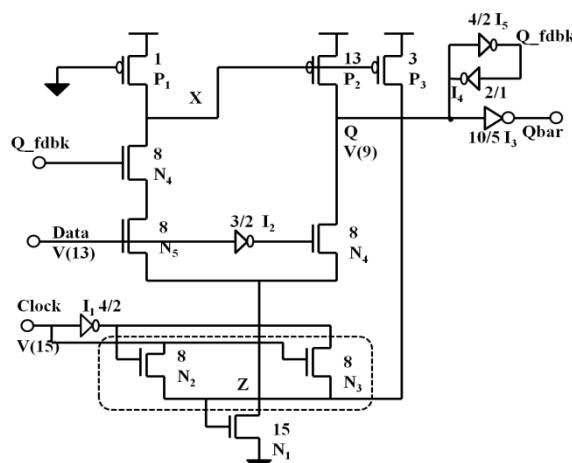
Fig. 5. Circuit diagram of the proposed P-FF design with pulse control scheme.

As opposed to the transistor stacking design in Fig. 2 and 4 , transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass

transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time.

When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1.

The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLFF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time.

It steps in when node X is discharged to $|V_{TP}|$ below the V_{DD}. This provides additional boost to node Z(from $V_{DD}-V_{TH}$ to V_{DD}). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach.

IV. Shift Registers

The above mentioned existing pulse triggered flip-flops and the proposed flip-flop are implemented in the following shift registers and the power consumption of those shift registers are calculated and compared.

Serial-in and Serial-out shift register

The serial in/serial out shift register accepts data serially that is, one bit at a time on a single line.
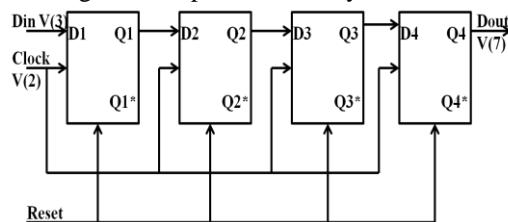
Fig 6. Serial-in and Serial-out shift register.

It produces the stored information on its output also in serial form. The Fig 6 shows the block diagram of 4 bit serial-in and serial-out shift register with Din as the input and Dout as output.

Serial-in and parallel-out shift register

This configuration allows conversion from serial to parallel format. Data is input serially, as described in the SISO section above.
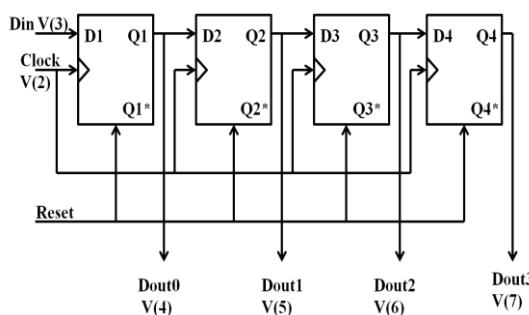
Fig 7. Serial-in and parallel-out shift register.

Once the data has been input, it may be either read off at each output simultaneously, or it can be shifted out and replaced. Serial in parallel out diagram is shown in fig 7. For this kind of register, data bits are entered serially

in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register.

Parallel-in and parallel-out shift register

For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit shown in fig. 8 is a four-bit parallel in - parallel out shift register. Both the inputs as well as the outputs performs the parallel operation. A global clock is given to activate all the flip-flops connected as shown below. The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the d inputs appear at the corresponding q outputs simultaneously.
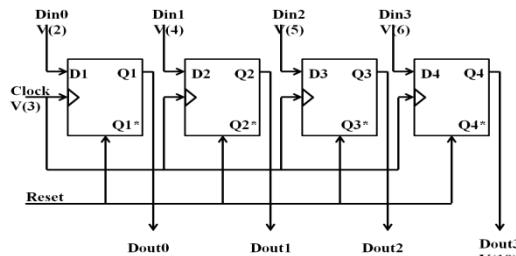
Fig. 8 Parallel-in and Parallel-out Shift Register.

Parallel -in and Serial-out shift register

This configuration has the data input on lines d1 through d4 in parallel format. To write the data to the register, the write/shift control line must be held low. To shift the data, the write/shift control line is brought high and the registers are clocked. The arrangement now acts as a PISO shift register, with d1 as the data input. However, as long as the number of clock cycles is not more than the length of the data-string, the data output, q, will be the parallel data read off in order as shown in Fig. 9.
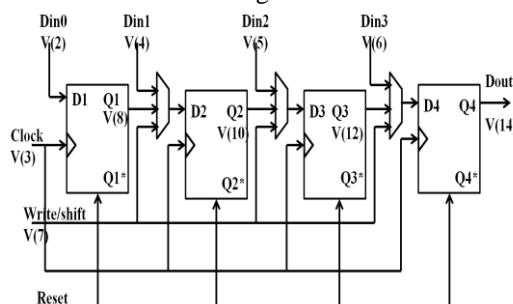
Fig 9. Parallel-in and Serial-out shift register.

V.   Implementation Details & Results

Simulation and analysis are carried out using H-spice and Cosmos scope tools.

Output waveforms of flip-flops

The Output waveforms of the flip-flops and shift registers are shown below. The Figs 10,11,12,13 show the outputs of the IP-DCO, MHLFF, SCCER and the proposed flip-flop respectively. The waveforms are observed over a period of 20ns. Clock and Data are inputs to the flip-flop and Q is the output of the flip-flop. It can be observed that Output follows the input for all the flip-flops.
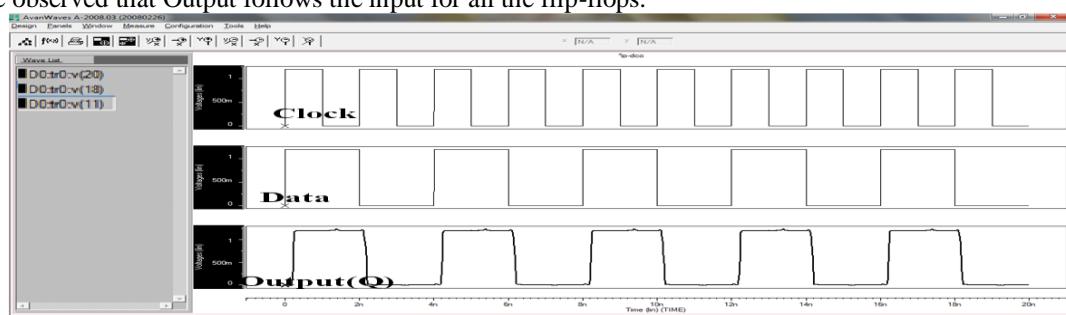
Fig. 10 Output of IP-DCO Flip-flop.
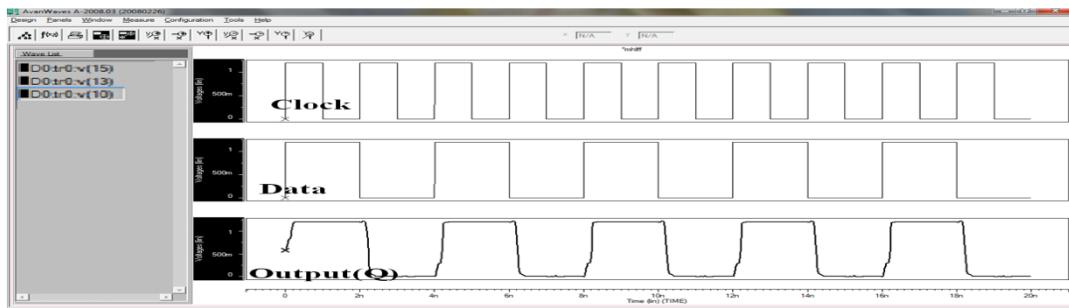
Fig 11. Output of Modified Hybrid Latch Flip-flop.
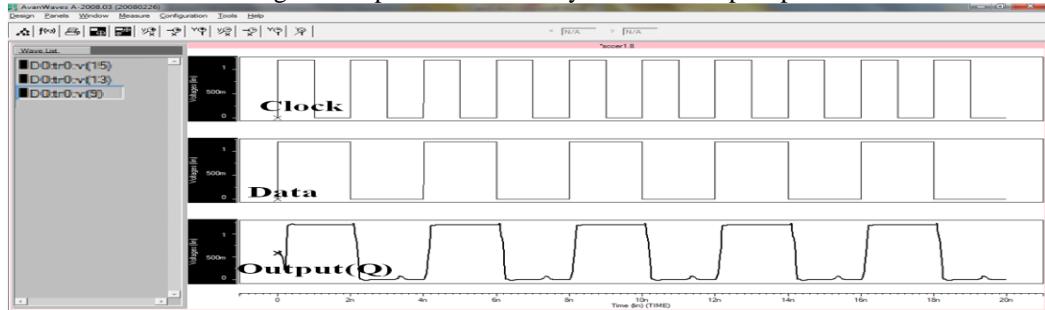
Fig 12. Output of SCCER Flip-flop.

Fig 13. Output of proposed pulse triggered Flip-flop.

Outputs of shift registers

The output waveforms of all the four types of shift registers SISO, SIPO, PISO, PIPO are shown in the following sections. The output waveforms are observed in a period of 100ns.

Outputs of Serial-in and Serial-out shift registers:

The input data is serially given out after four clock cycles for serial-in and serial-out shift register and this can be observed in the Fig. 14, Fig. 15, Fig. 16, Fig. 17, when implemented using IP-DCO, MHLFF, SCCER and proposed flip-flop respectively.
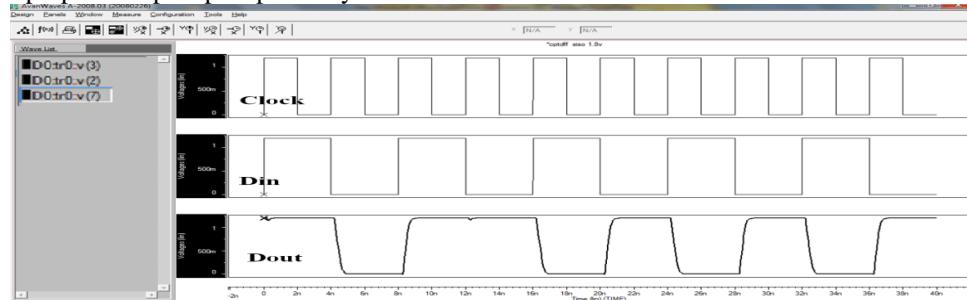
Fig 14. Output of serial-in and serial-out shift register using IP-DCO flip-flop.
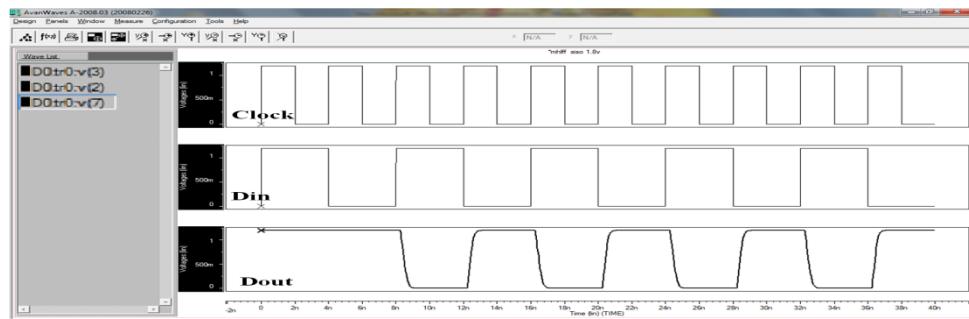
Fig 15. Output of serial-in serial-out shift register using MHLLF flip-flop.
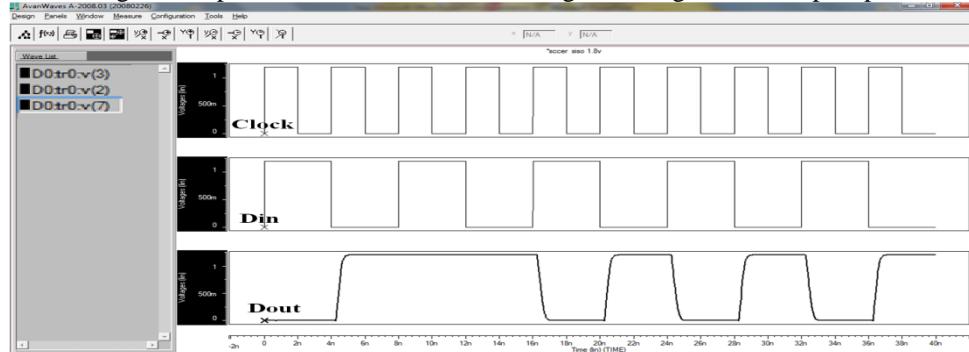
Fig 16 Output of serial-in and serial-out shift register using SCCER flip-flop.
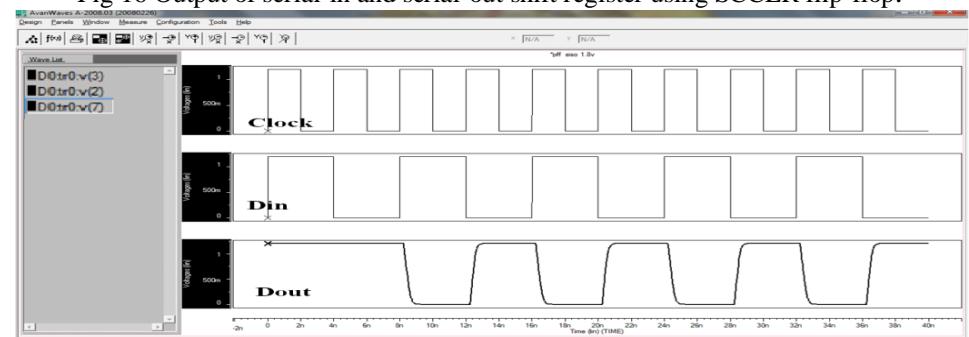
Fig 17. Output of serial-in and serial-out shift register using proposed flip-flop.

Outputs of Serial-in and Parallel-out shift registers

The input data is given in serially and given out parallely at Dout0,Dout1,Dout2,Dout3 for serial-in and parallel-out shift register and this can be observed in the Fig. 18, Fig. 19, Fig. 20, Fig. 21, when implemented using IP-DCO, MHLFF, SCCER and proposed flip-flop respectively.
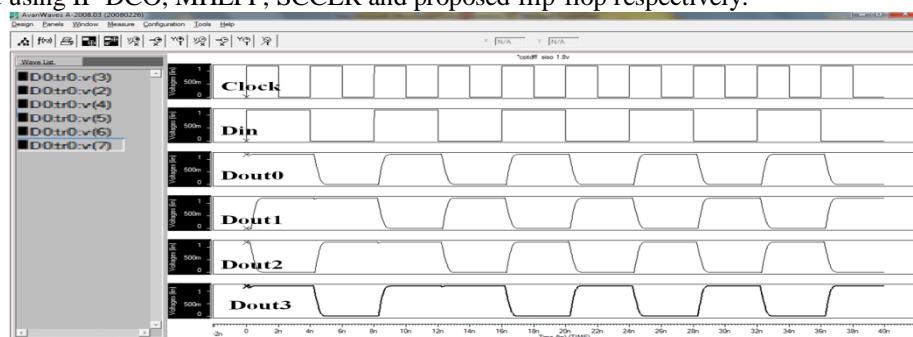
Fig 18. Output of serial-in and parallel-out shift register using IP-DCO flip-flop.
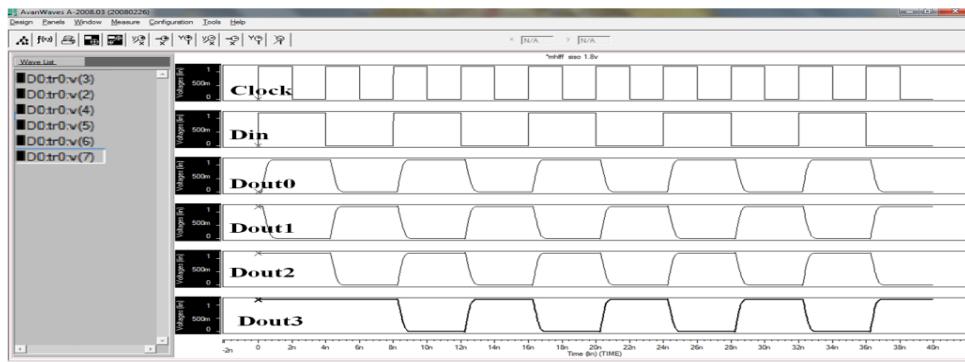
Fig 19. Output of serial-in and parallel-out shift register using MHLLF flip-flop.
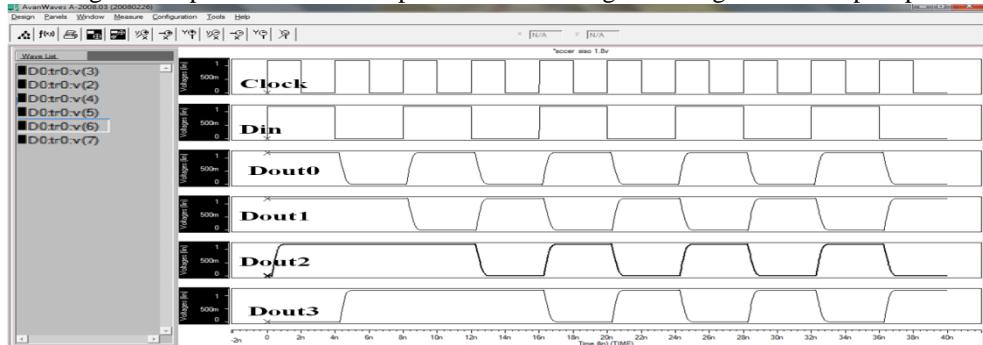
Fig 20. Output of serial-in and parallel-out shift register using SCCER flip-flop.
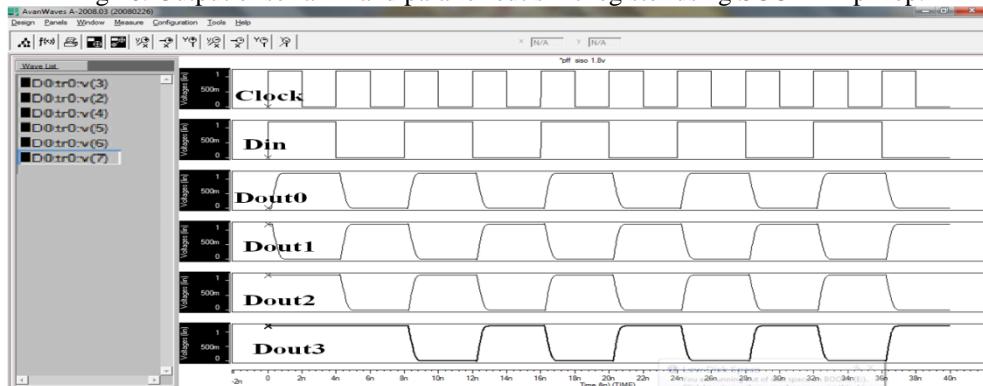
Fig 21. Output of serial-in and parallel-out shift register using proposed flip-flop.

Outputs of parallel-in and parallel-out shift register

The input data is parallely given in and given out for parallel-in and prallel-out shift register and this can be observed in the Fig. 22, Fig. 23, Fig. 24, Fig. 25, when implemented using IP-DCO, MHLFF, SCCER and proposed flip-flop respectively.
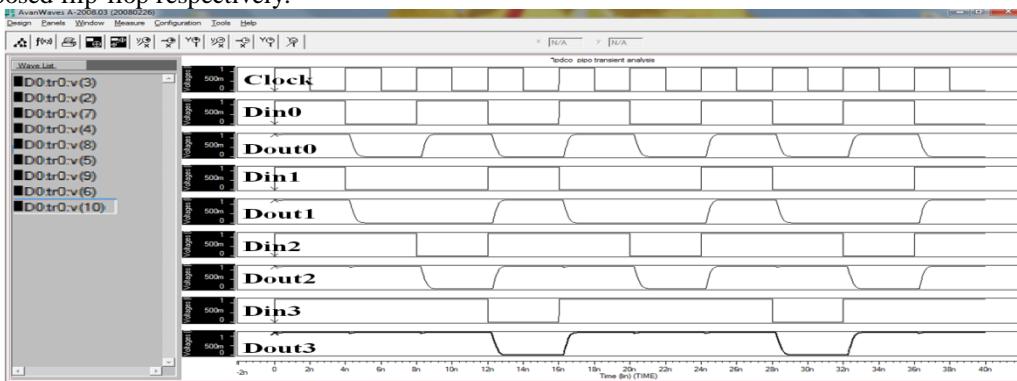
Fig 22. Output of parallel-in and parallel-out shift register using IP-DCO flip-flop.
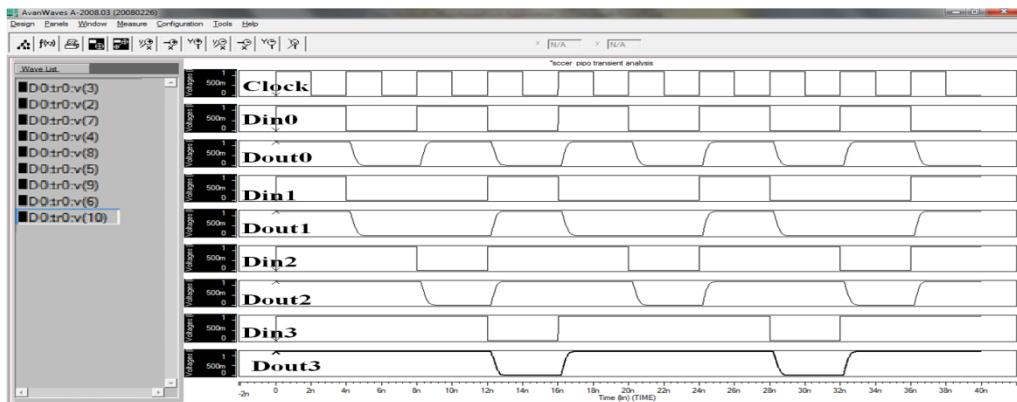
Fig 23. Output of parallel-in and parallel-out shift register using SCCER flip-flop.
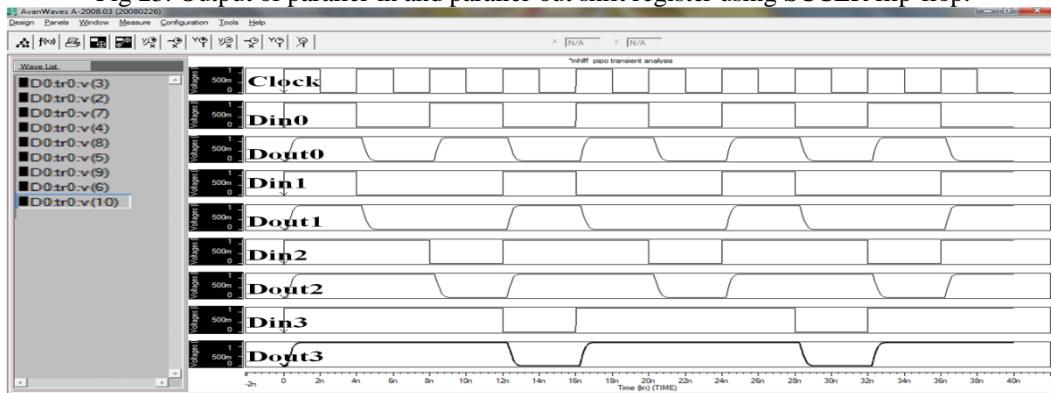
Fig 24. Output of parallel-in and parallel-out shift register using MHLLF flip-flop.
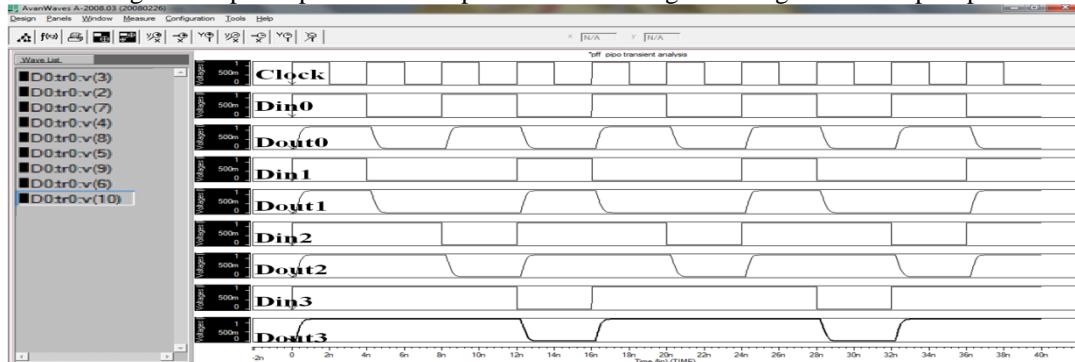
Fig 25. Output of parallel-in and parallel-out shift register using proposed flip-flop.

Outputs of parallel-in and serial-out shift registers

The input data is given in parallely a given out serially Parallell-in and Serial-out shift register and this can be observed in the Fig. 26, Fig. 27, Fig. 28, Fig. 29, when implemented using IP-DCO, MHLFF, SCCER and proposed flip-flop respectively.
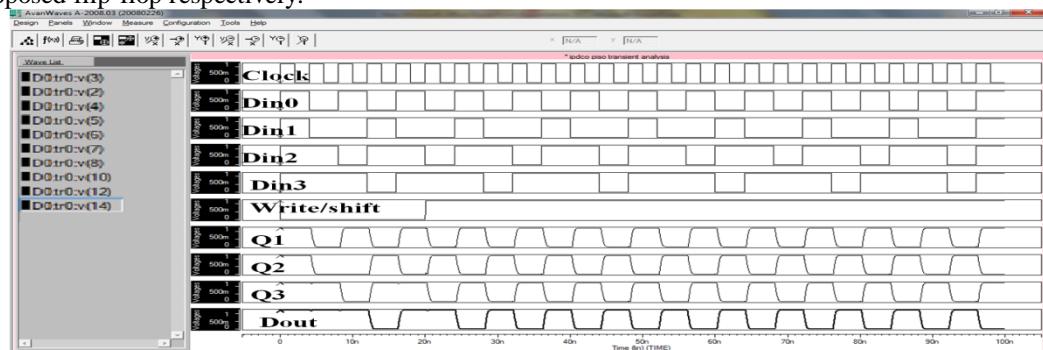
Fig 26. Output of parallel-in and serial-out shift register using IP-DCO flip-flop.
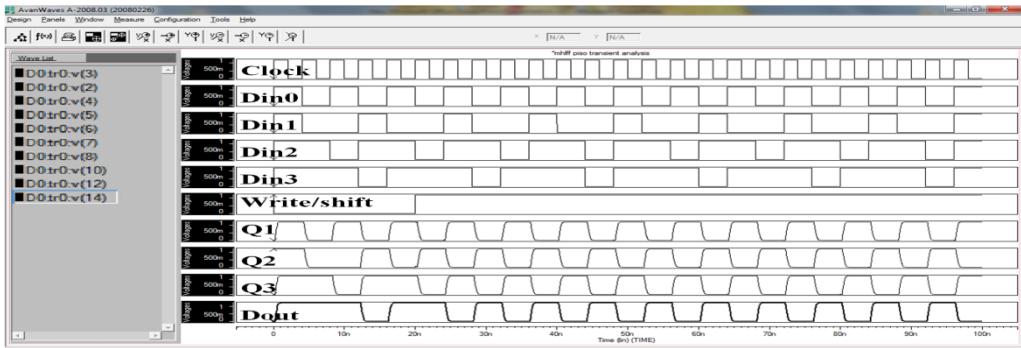
Fig 27. Output of parallel-in and serial-out shift register using MHLLF flip-flop.
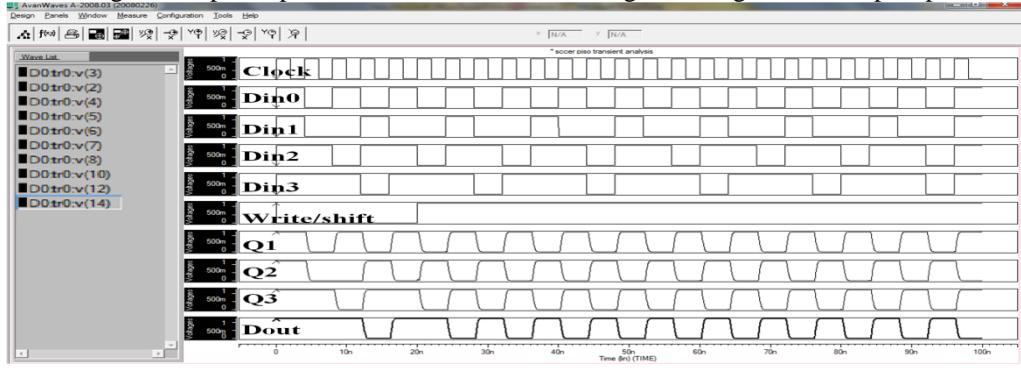
Fig 28. Output of parallel-in and serial-out shift register using SCCER flip-flop.
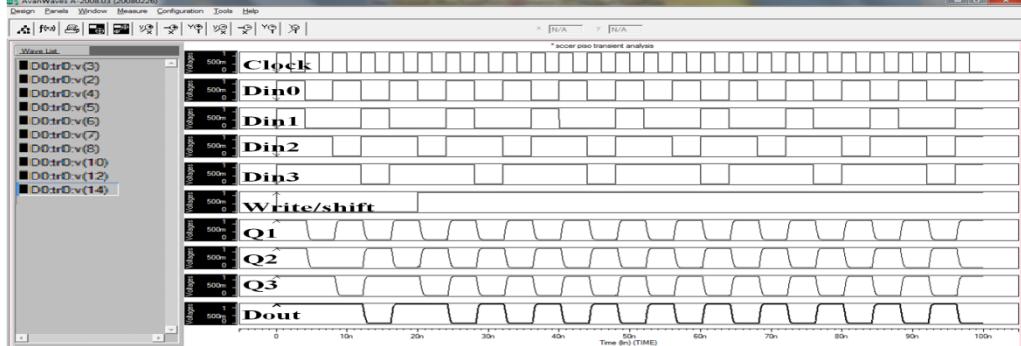
Fig 29. Output of parallel-in and serial-out shift register using proposed flip-flop.

Table1. describes The simulation results of the pulse triggered flip-flops discussed above. Average power, Minimum Data to Q delay , power delay product are described in the table and it can be noted that the proposed flip-flop excels in all the parameters when compared to the other flip-flop designs.

Table1. Comparison of pulse triggered flip-flops.

Parameter	Pulse triggered flip-flops			
	IP-DCO	MHLFF	SCCER	Proposed
Number of transistors	23	19	17	19
Average power(μW)	37.30	34.66	36.31	29.82
Minimum Data to Q Delay(pS)	223.8	221.98	195.38	156.02
Power Delay Product(fJ)	8.347	7.693	7.094	4.652

Table2 describes the average power of the shift registers SISO, SIPO, PIPO, PISO using the flip-flops IP-DCO, MHLFF, SCCER, and proposed flip-flop. It can be observed that the average power of shift registers is less when implemented using proposed flip-flop in all the cases.

Table2. Average power comparison of shift registers

Pulse triggered flip-flops	Average power(□w) of shift registers			
	SISO	SIPO	PIPO	PISO
IPDCO	121.1	121.1	119.1	124.5
MHLLF	200.6	200.6	104.5	190.5
SCCER	117.7	117.7	88.3	125.8
PROPOSED	103.5	103.5	79.97	106.2

VI. Conclusions

Conventional implicit type flip-flops IP-DCO,MHLLF,SCCER are analyzed in particular and are simulated. It is known that larger transistors are required to enhance the discharging capability in those designs. In an attempt to overcome the above drawbacks a low power pulse triggered flip-flop is devised by employing two new design metrics. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic, the second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum.

Simulation results of the proposed pulse triggered flip-flop design show that it excels in terms of average power, power delay product when compared to the other flip-flop designs IP-DCO, MHLLF and SCCER.

The proposed flip-flop when implemented in shift registers, works well and the average power of the shift registers implemented using proposed flip-flop is less when compared to the other shift registers implemented with existing pulse triggered flip-flops.

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