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Gdi Technique Based Carry Look Ahead Adder Design

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Abstract: *Low Power design is main object in the Very Large Scale Integration (VLSI) Design Gate Diffusion Input (GDI): a new technique for designing the low power digital circuits. This technique allows reducing the power consumption, propagation delay and area of digital circuits. In this paper, a Full Swing Gate Diffusion Input (FS-GDI) methodology is proposed for designing the low power digital circuits. This proposed technique is applied to a 180 nm technology with 1v supply voltage carry look ahead adder (CLA) using MENTOR GRAPHICS.*
Keywords: *Pass Transistor Logic, Transmission Gate, GDI, Full Swing GDI, Power Dissipation, Delay.*

I. Introduction

VLSI technology has played a development of portable digital applications, the applications demand for increasing the speed, implementation of a wide range of complex functions, less power dissipation. Mainly it is focusing on power consumption and area reduction of the digital circuits. Power is the disconcerting factor in portable applications. And another thing is area, it is directly possessions the cost and size of the devices. And also, to improve the performance of logic circuits based on the CMOS technology. The CMOS technology made by the complementary of a pull-up PMOS transistor and Pull-down NMOS transistor. MOSFET networks are the most predictable, but at circuit level an optimized design is desirable having less numbers of transistors, small power consumption and reduces delay. The low power digital Circuits is Pass Transistor Logic (PTL), it is only obtainable by the nmos transistor. Where a control signal is applied to the gate of nmos transistors, another data signal is applied to the source of nmos transistor. There are many sorts of PTL techniques that anticipated solving the problems. Transmission Gate (TG) uses to realize complex logic functions by using a small number of complementary transistors. It solve by the low level swing using pmos as well as nmos. There is much machinery proposed to improve power dissipation, area. Gate Diffusion Input (GDI) is one of the techniques to reduce the power dissipation, delay and area. It is implemented in Standard CMOS logic [3]. It approaches to realization of a wide range of complex logic functions using only two transistors. GDI, which is suitable for fast and less power dissipation as compared to a existing PTL,TG techniques. In this paper some of the digital circuits are implanted by using PTL, TG, GDI techniques. The paper prepared as follows: Section II literature survey of the previous work. Proposed CLA implementation presented in Section III, Simulation results and layouts are presented in Section IV, conclude the paper in Section V.

II. Literature Survey Of The Previous Works

1. Pass Transistor Logic

The pass transistor logic [6] is used as a switch n relaying the signals. The path through each switch is isolated from the signal activating the switch. This allows the designer to have a considerable freedom in implementing architectural features as compared with bipolar logic-based design. The advantages of the pass transistor logic, which is reduced to the interconnecting of wires and also reduced to the number of transistors to occupy the small area. The disadvantage of the pass transistor logic, operation is very slow. The basic AND and OR gates by using Pass Transistor logic shows below. Figure 2 and 3.

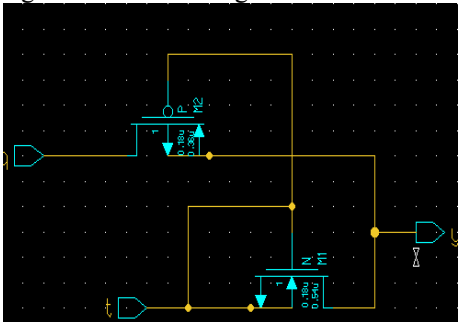


FIG.2. AND

The operation of the AND gate by using pass transistor logic which requires to the two transistor such as PMOS, NMOS. When '1' applied to the inputs of a and b, the PMOS transistor will turn off and NMOS transistor will turn on. Then the output will be '1'. When '0' applied to the inputs of a and b, the PMOS transistor will turn on and NMOS transistor will turn off. Then the output will be '0'.

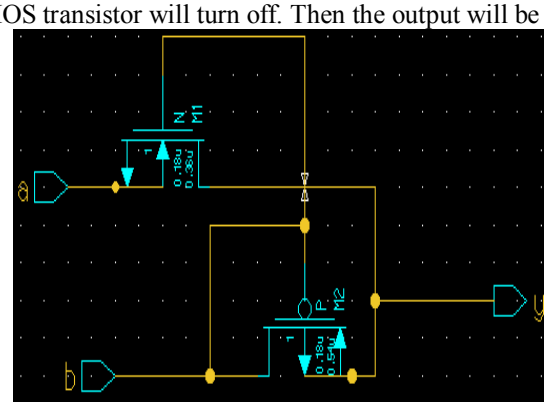


FIG.3. OR

The operation of the OR gate by using pass transistor logic which requires to the two transistors such as PMOS, NMOS. When '1' applied to the inputs of the a and b, the PMOS transistor will turn off and NMOS transistor will turn on. Then the output will be '1'. When '0' applied to the inputs of the a and b, the PMOS transistor will turn on and NMOS transistor will turn off. Then the output will be '0'.

2. Transmission Gate

The transmission gates are complementary switches made up of a P-pass and N-pass transistor in parallel. The transmission gate is free from any such degradation of logic levels although it occupies more area and requires the more complementary signals to drive it. Also, the on resistance of transmission gates lower than that of simple pass transistor switches. The basic AND and OR gates by using Transmission gate logic shows below of figures 4 and 5.

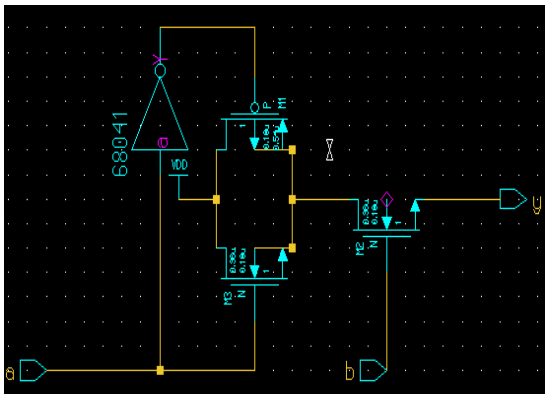


FIG.4 AND

The operation of the AND gate by using Transmission gate which requires to the two transistor such as PMOS, NMOS, and control signal. The control signal is working at inverter. When '0' applied to the inputs of a and b, the PMOS transistor will turn on and NMOS transistor will turn off the logic '0' passed through another NMOS. Then the output will be '1' or logic '0'

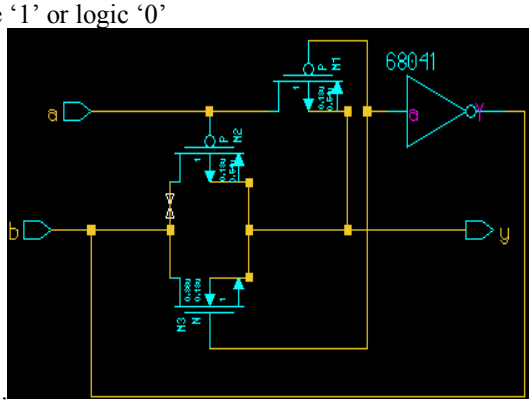


FIG. 5 OR

3. Gate Diffusion Input (Gdi)

Gate Diffusion Input, allows to implementation of a wide range of complex logic functions using only two transistors. The inputs are directly diffused into the gates PMOS, NMOS transistors. So, it is called a gate diffusion input [3][4]. This method is suitable for fast, the low power circuits reducing to the number transistors as compared to CMOS. This method is based on the simple cell as shown in the figure.6.

The GDI cell contains four terminals, they are:

1. G: Common gate input of PMOS and NMOS
2. P: Input to the source/ drain of PMOS
3. N: Input to the source/drain of NMOS
4. Bulks of both PMOS and NMOS are connected to N or P.

It must be remarked that not only possible all the logic functions in Standard p-well CMOS process but can be susses fully implemented in Twin Well CMOS Process or SOI technologies.

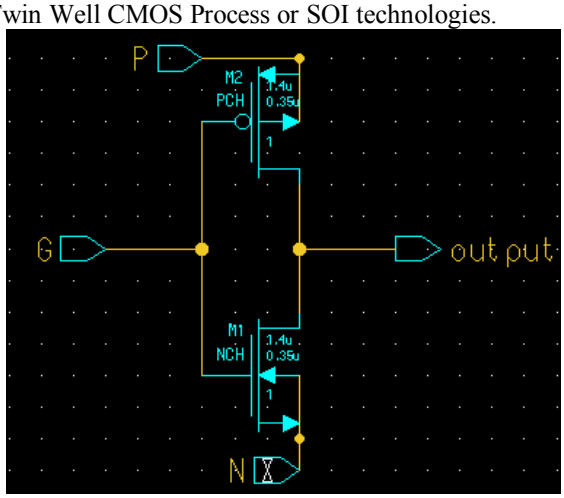


FIG 6. GDI CELL

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+B’A	XOR
B	B	A	AB+A’B’	XNOR

Table.1 Different Inputs Are Using In Gdi Cell

The basic AND and OR gates are using GDI technique shown bellow of the figures 7 and 8. The operation of the AND gate by using Gate Diffusion Input Technique which requires to the two transistor such as PMOS, NMOS. When ‘0’ applied to the inputs of a and b, the PMOS transistor will turn on and NMOS transistor will turn off .Then the output will be ‘0’. When ‘1’ applied to the inputs of a and b, the PMOS transistor will turn off and NMOS transistor will turn on .Then the output will be ‘1’.

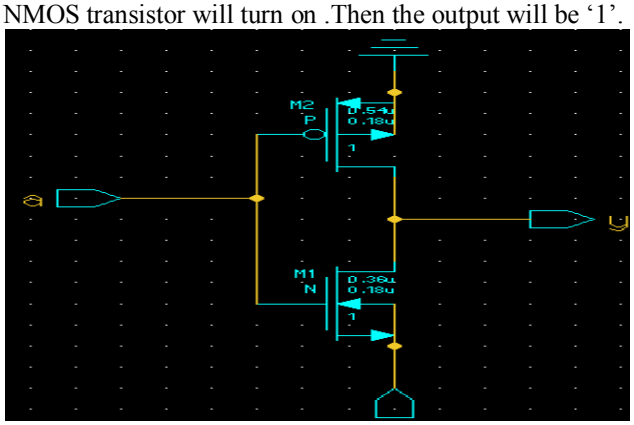


Fig. 7 AND

The operation of the OR gate by using Gate Diffusion Input Technique which requires to the two transistors such as PMOS, NMOS. When '0' applied to the inputs of the a and b, the PMOS transistor will turn on and NMOS transistor will turn off .Then the output will be '0'. When '1' applied to the inputs of a and b, the PMOS transistor will turn off and NMOS transistor will turn on .Then the output will be '1'.

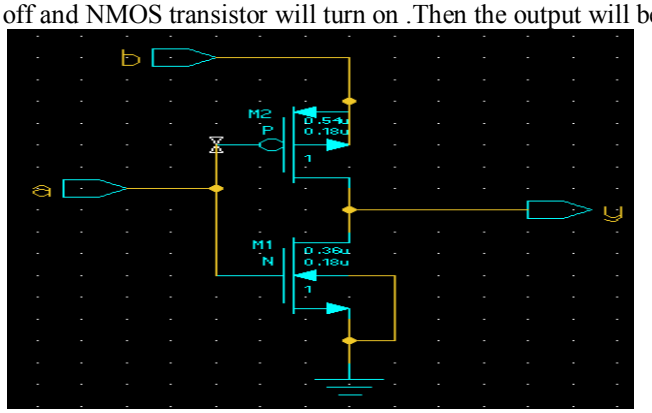


Fig. 8. OR

Pass transistor, Transmission gate, Gate Diffusion Input techniques are using different implementation of a digital circuits. These three techniques implemented by the 4*1 Multiplexer, 8*3 Encoder, BCD counter and Mealy Machine. The Table.2 shows by the comparison of power dissipation and Table. 3. Shown by the Transistor count using these PTL, TG and GDI techniques.

3.1 Multiplexer

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single input line. The basic multiplexer has several data input lines and single output line. It provides the digital equivalent of an analogy selector switch. The figure 9 Shows 4*1 multiplexer by using PTL, TG, and GDI with supply voltage 1V. The power dissipation and transistor count shown in table.2.

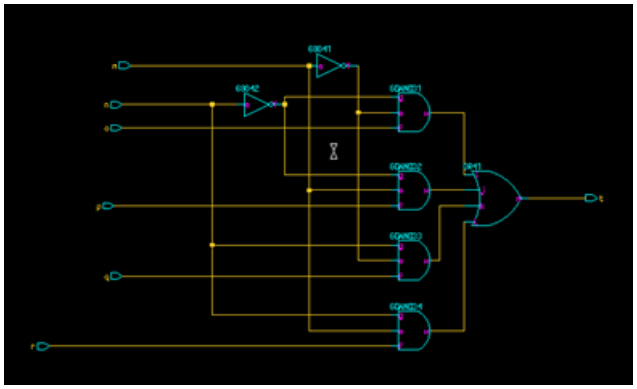


Fig.9. 4*1 Multiplexer

3.2 8*3 Encoder

An encoder is a digital circuit that performance the inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generated the binary code corresponding to the input value. The 8*3 Encoder implemented with PTL, TG and GDI with supply voltage 1v. The figure10 Shows bellow. The power dissipation and transistor count shown in table.2.

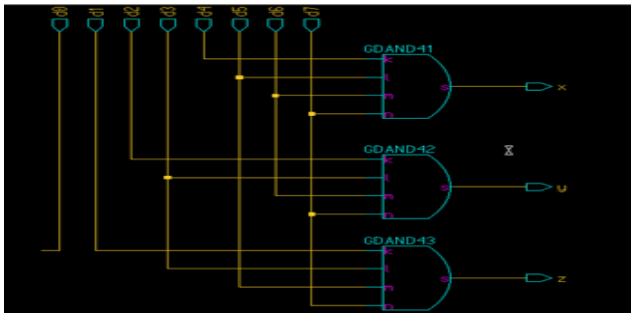


Fig.10. 8*3 Encoder

3.3 Bcd Counter

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, periodically is affiliation to a clock signal.

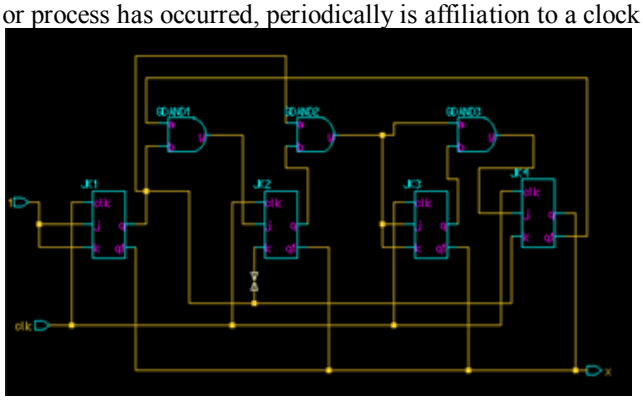


Fig. 11 BCD Counter

The BCD Counter implemented with PTL, TG and GDI with supply voltage 1v. The figure.11 Shows bellow. The power dissipation and transistor count shown in table.2.

3.4 Mealy Machinne

Mealy machine, output of the sequential circuit depends on both present states of the flip flop(s) and on the input(s). The figure 12 shows mealy machine by using PTL, TG and GDI with supply voltage 1V. Clock pulse can not affect the state of the flip-flop. The advantage of the mealy machine is used to reduce the number of stages. The power dissipation and transistor count shown in table.2.

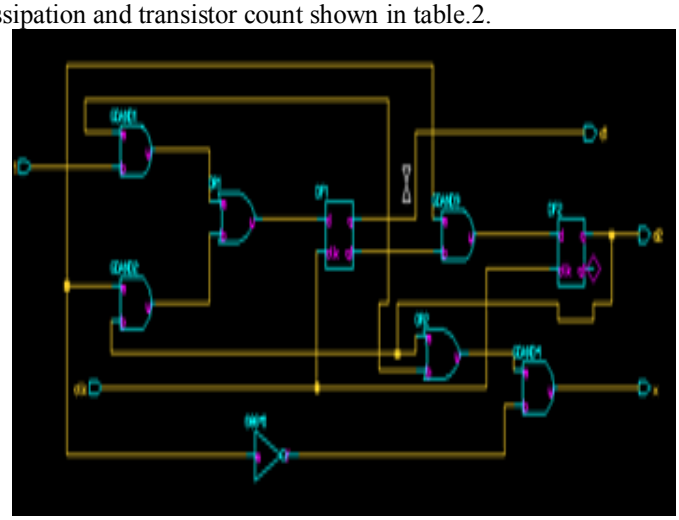


Fig 12. Mealy Machine.

Table.2. and 3 Comparision Of Powerdissipation Using Ptl, Tg And Gdi

	POWER DISSIPATION		
	PTL	TG	GDI
4*1 MUX	98.655 PW	21.3089 PW	1.8570 PW
8*3 Encoder	63.926 PW	18.354 PW	0.75PW
BCD Counter	13.284 µW	20.652 µW	9.284 µW
Mealy Machine	6.225 µW	87.716 µW	5.775 µW

Table 2. Power Dissipation

	TRANSISTOR COUNT		
	PTL	TG	GDI
4*1 MUX	48	32	26
8*3 Encoder	36	24	18
BCD Counter	86	73	54
Mealy Machine	58	72	36

Table 3 Transistor Count

III. Proposed Work

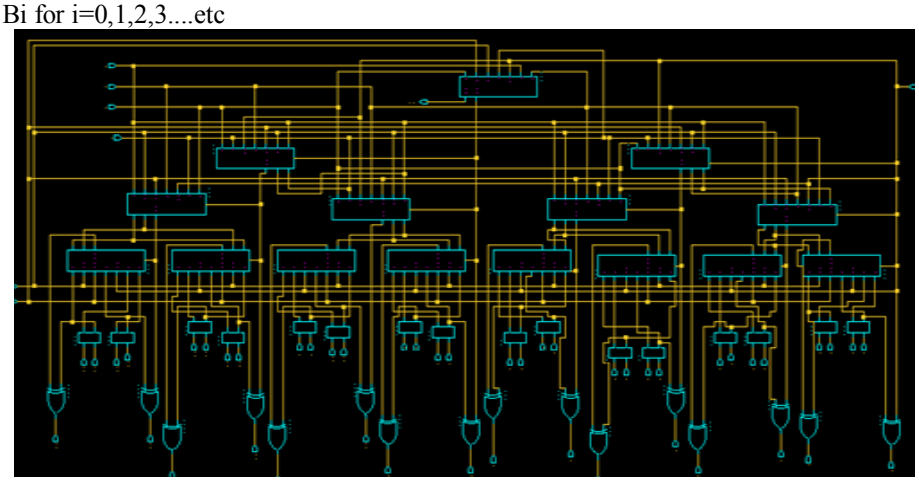
4. Carry Look Ahead Adder

CLA, consists of three stages, a propagate block/ generate block, a sum generator and carry generator. General block diagram of the 16 bit CLA adder shown bellow. Generate block can be realized using the expression

Gi=Ai.Bi for i=0, 1, 2, 3.....etc

Propagate block can be realized using the expression

Pi=Ai $\oplus$ Bi for i=0,1,2,3....etc



The CLA adder is designed to overcome the latency introduced by the rippling effect the carry bits. The propagation delay occurred in the parallel adders can eliminated by the carry look ahead adder.This adder reduces the carry delay and reducing the number of gates through which a carry signal must propagate. This adder implementing by the gate diffusion input technique.

5. Full Swing GDI

GDI technique may suffer from the threshold voltage drop. Whenever, threshold voltage drop occurred at gates the drive current reduce and also affect the performance of the gate [3]. These drops also increase at static power dissipation at the cascading of the inverter. So, it used for swing restoration (SR). The GDI technology uses a basic logic function. Shows the table.1, F1 and F2 are using NAND and NOR gates. Generally, NAND and NOR gates are implemented with four transistors. In GDI method, NAND and NOR gates are implemented with two transistors, be like the basic CMOS inverter. This technology reduces to the number of transistors, which is very competent for running of various gates. Such as MUX, AND, OR. Etc which are shown in table. 1. Structure of the full swing F1 and F2 cell shows below of the figure 13, 14.

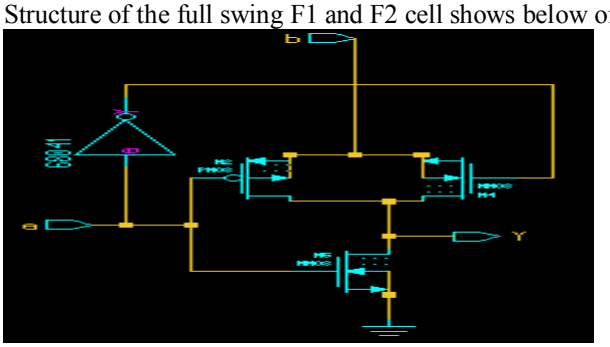


Fig 13. F1

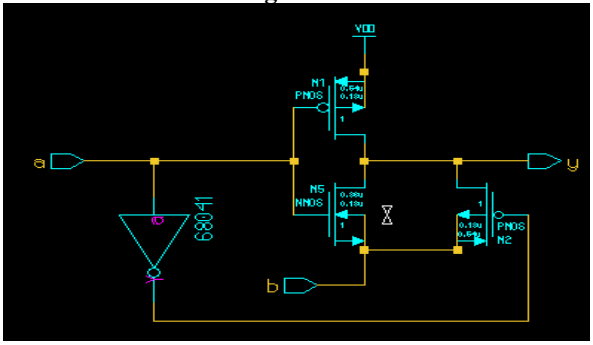


Fig14. F2

`When voltage drop occurred at the output, the SR transistor activated. The threshold voltage drop occurs only at logical levels. SR transistors only certify the full swing operation. The basic diagram of the CLA design using with GDI F1 and F2 gates, shown fig 15 bellow.

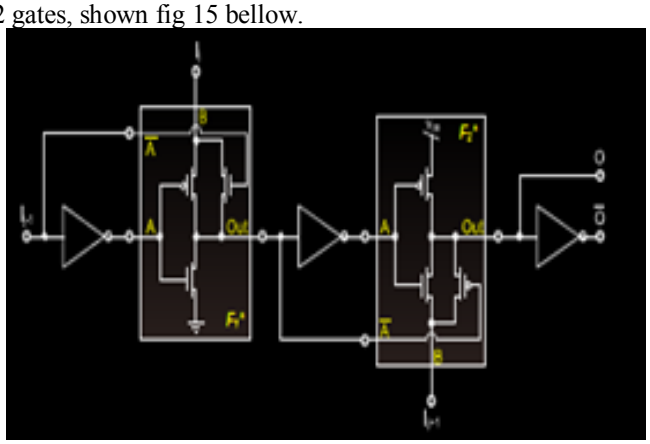


Fig .15 CLA using GDI cell

The basic 2 bit GDI CLA implemented with LCG and PG. The block diagram of 2 bit GDI CLA shown in figure 16.

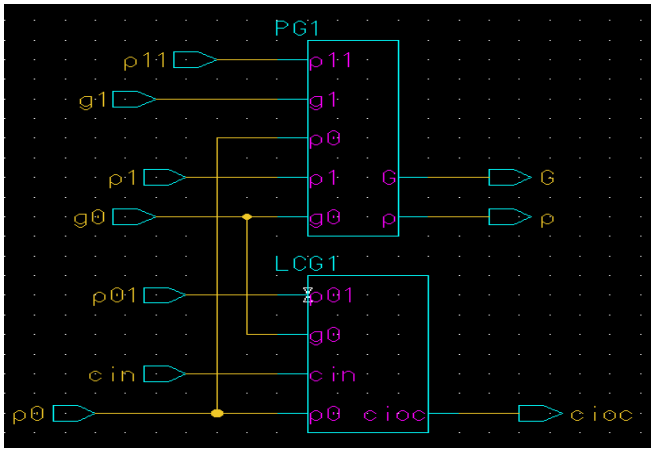


Fig .16 2 bit GDI CLA ADDER

Generate block and Propagate block expressions using full swing GDI,

g= A B, (F1 (A' B) Table.1 shown)

p= A ⊕ B, (GDI XOR gate)

The figure 17 shown bellow, of generate block (g) and propagate block (p) using full swing GDI technique.

In propagate block, GDI XOR gate using. In GDI technology the XOR gate having only four transistors. Comparing with basic CMOS transistor the GDI technique reduces to the number of transistors. The XOR gate implementing with Pass Transistor logic, Transmission gate and Gate diffusion Input technique. The GDI implementation greatly advantage in terms of Transistor count and area [2].

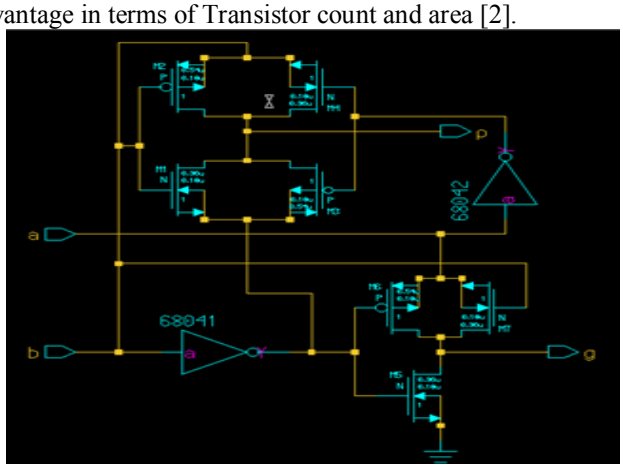


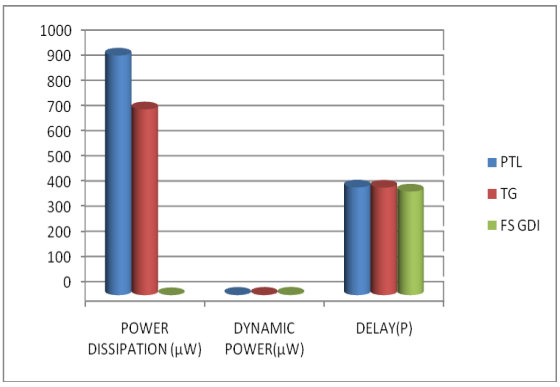
Fig.17 p and g blocks using GDI technique

IV. Simulation Results And Layouts

The proposed circuit 16 bit CLA simulated using MENTOR GRAPHICS in the TSMC180nm technology in the 27^0c and the supply voltage used in the simulations is 1V. Table 4 shows the power dissipation at 27^0C, Dynamic power and Delay, also output of the 16 bit CLA using GDI technique.

	POWER DISSIPATION	DYNAMIC POWER	DEALY
PTL	952.705µw	1.6159MW	428.41P
TG	738.7136µw	1.6965MW	427.44P
FS GDI	938.767 FW	1.9402MW	411.94P

Table.4 16 BIT CLA ADDER POWER DISSIPATION, DYNAMIC POWER AND DELAY



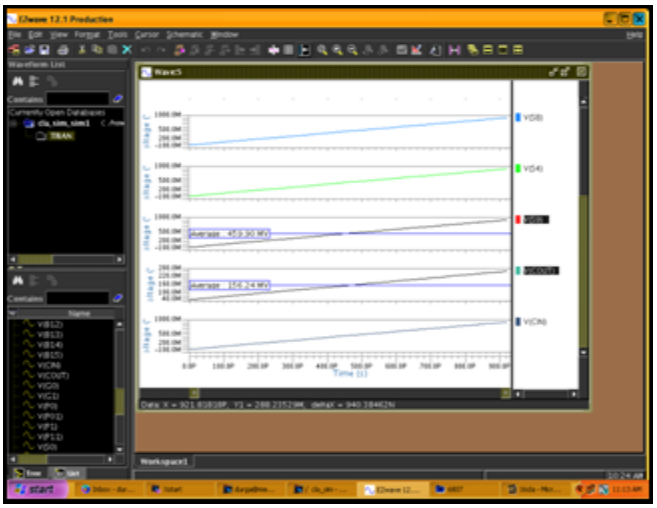


Fig 18 Output of 16 bit CLA using GDI technique

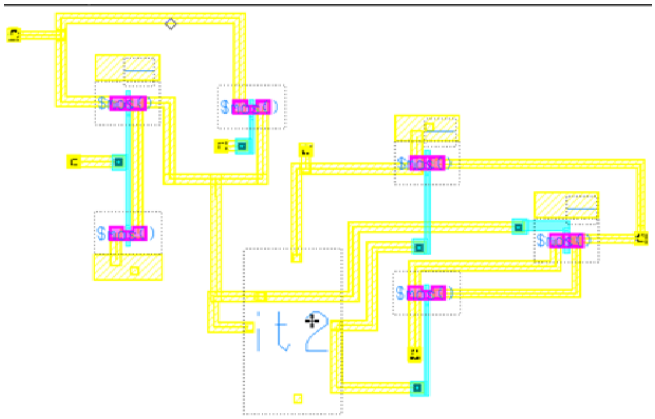


Figure 19 layout diagram of the LCG

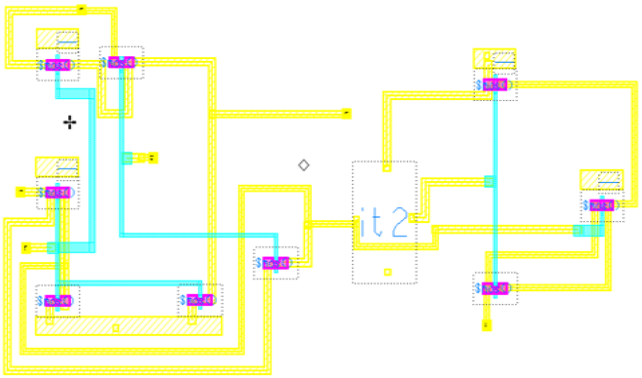


Figure 20 layout diagram of the PG block

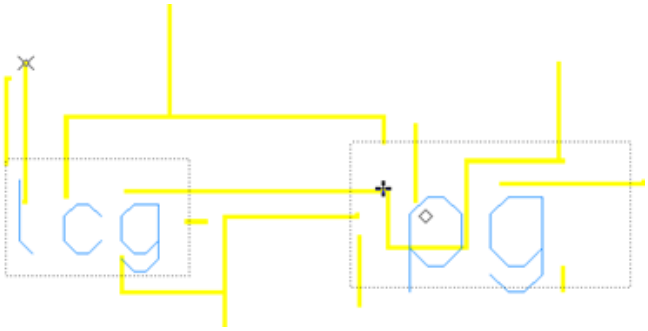


Figure 21 layout diagram of the 2 bit CLA adder

V. Conclusion

The Carry look ahead adder is evaluated using FS-GDI methodology. Simulation results shown exhibits the beneficial performance of the proposed FS-GDI methodology compared to the conventional GDI methodology. The FS GDI achieves 36%, 18% power is reduced compared to PTL, TG methodologies.

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