

## Performance of low power Domino Circuits using pseudo dynamic buffer

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**Abstract:** *this paper proposes a buffer circuit for footed domino logic circuit. It minimizes redundant switching at the output node. This circuit prevents propagation of precharge pulse to the output node during precharge phase which saves power consumption. We have calculated the power consumption, delay and power delay product of proposed circuits and compared the results with existing domino circuit for different logic function, loading condition, clock frequency and power supply. Our proposed circuit reduces power consumption and power delay product of the domino circuit as compare to other domino circuit proposed earlier. All the simulation result is carried out TSMC -0.18 $\mu$ m CMOS technology at 1.8V power supply.*

**Keywords:** *Buffer, Dynamic circuit, Power consumption, Delay, Precharge pulse*

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### I. Introduction

The rapid integration of VLSI circuit is due to the increased use of portable wireless systems with low power budget and microprocessors with higher speed. To achieve high speed and lower power consumption transistor technology and power supply must be scaled down simultaneously. As the technology scales down the threshold voltage ( $V_{th}$ ) of the transistor also lowers in the same proportionate (Das and Brown 2005). Scaling of threshold voltage results in exponential increase of sub threshold leakage current in the evaluation transistor and makes the domino logic less noise immune. This logic family offers a number of interesting features compared to static logic, namely reduced transistor count as well as reduced load capacitance and hence improved speed. The operation of a dynamic logic gate is controlled by a clock signal and can be implemented in either Pull-up (P-type) or Pull-down (N-type) configurations [1].

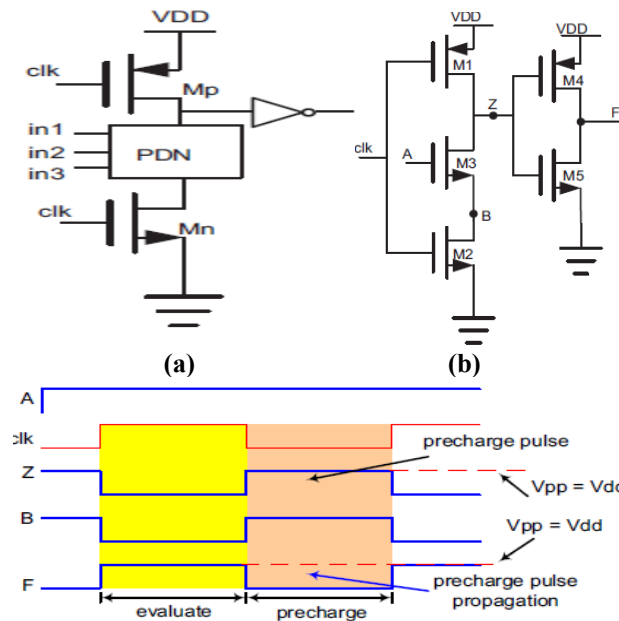
The voltage at the output of the dynamic circuit is stored on a parasitic capacitance, which is typically buffered before it is sent to the next stage. This temporary voltage is affected not only by charge sharing of the internal parasitic capacitances [2], but also by the consequent dynamic circuit. Normally, a buffer at the output of the dynamic logic is required to drive the next stage. A typical domino gate [1] consists of a P-type or N-type network followed by a static inverter. But domino logic use dual phase namely precharge and evaluation to implement complex circuit with single evaluation network [3]. Domino circuit has drawback of high power consumption due to clock loading and reduce noise margin due to charge sharing and charge leakage. Buffer is required to drive the output of the domino logic circuit into the next stage [4]. It is seen that static logic circuit consume power due to redundant switching at the output node. But domino logic circuit consumes power due to redundant switching at dynamic and output node [5]. This redundant switching increase the power consumption.

The rest of the paper is organized as follows : In section –II previous work ,section III-Proposed Circuit Buffer, section IV-Simulation result.

### II. Previous Work

Fang Tang et al [6], designed pseudo dynamic buffer (PDB) for footed domino logic circuit implementation of Fig.1 and Fig.2. Fig. 1(a) & (b) shows the schematic and implementation of a conventional footed clock controlled domino logic circuit, which consists of a dynamic N-type gate (Pull-down network PDN) followed by a static inverter. The circuit operates in two phases, namely precharge and evaluation phases. During the precharge phase the clock signal  $clk$  is pulled low thus turning on the PMOS transistor M1 enabling to precharge the dynamic node Z. During the evaluation phase, the clock signal  $clk$  is pulsed high, thus turning on the NMOS transistor M2. When the input A is low, the logic at node Z is kept high regard less of the operating phase. However, when the input A is high, two phases (evaluation and precharge) should be discussed as depicted in Fig. 1(C). During the precharge phase, node Z is charged up to  $V_{dd}$  as well as node B. The voltage at node F drops down to '0', resulting in a propagation of the precharge phase to the output of the buffer. The

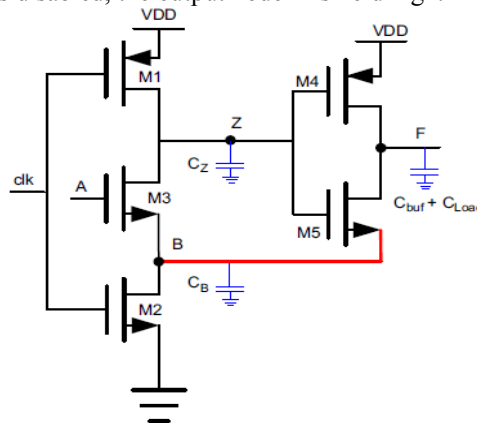
propagation of the precharge pulse from node Z through the static buffer results in increased power consumption.

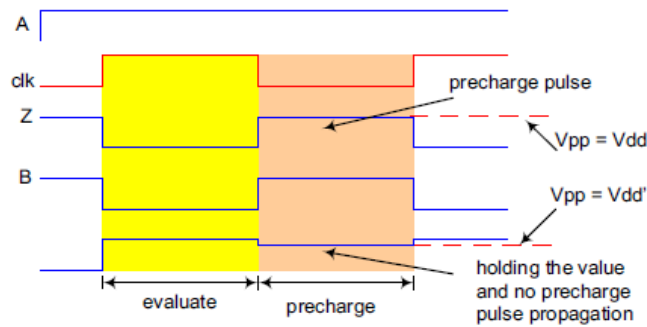


**Fig-1(a)** domino logic circuit using the conventional buffer. **(b)** The buffer is a static inverter, which connects the source of  $M5$  to  $Gnd$ . **(c)** Timing diagram of the conventional domino logic circuit, when input logic  $A$  is '1'.

Another circuit designed in Fig. 1 (a) illustrates the issue of performance degradation due to the propagation of the precharge pulse inherent in domino logic gates. The designed PDB-based implementation overcomes this problem using the circuit structure shown in Fig. 2 (a) & (b). In the designed implementation of the buffer, the source of the buffer's NMOS transistor  $M5$  is connected to node  $B$  instead of  $Gnd$ . Using such a circuit topology, the value at node  $Z$  cannot propagate to the output  $F$  during the precharge phase of the gates since during this phase, the evaluation transistor  $M2$  is turned off. For our designed gate, when the input logic  $A$  is low, the floating node  $Z$  is always high and then, the output node  $F$  is kept low regardless of the operating phase. On the other hand, if the input  $A$  is high, the precharge and evaluation phases will lead to the following situation [7]:

- During the evaluation phase, node  $Z$  is discharged to  $Gnd$  as well as node  $B$ , resulting in enabling the PMOS transistor  $M4$ , while pulling up the output  $F$  to  $V_{dd}$ .
- During the precharge phase, node  $Z$  is charged up to  $V_{dd}$ , followed by the voltage at node  $B$ . Since the NMOS evaluation transistor  $M2$  is disabled, the output node  $Z$  is held high.

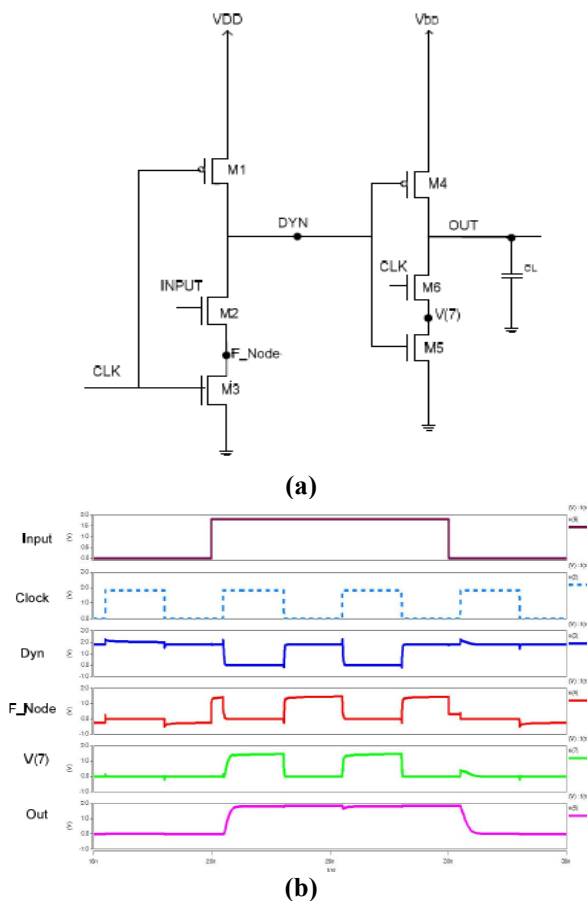




**Fig. 2.(a)** Domino logic circuit using the PDB. **(b)**Timing diagram of domino logic circuit. Note that there is an expected small voltage drop  $V_{0pp}$  at the output node F during the precharge phase.

### 2.1 True Single Phase Clock (TSPC) Dynamic Logic

TSPC dynamic logic [7] is shown in Fig. 3(a) and its characteristics at different node is shown in Fig. 3(b). This circuit is similar to standard footed domino logic except extra nMOS transistor is connected in the output inverter. This circuit requires 3 clock transistor and it increase the load capacitance of the clock signal and the power consumption. In this circuit, during precharge phase transistor M6 is OFF which helps the output to hold its previous value.



**Fig. 3.(a)**TSPC dynamic logic circuit, **(b)** Its selected node characteristics [7].

**Amit Kumar Pandey et al [8]** designed two proposed circuit Fig.4 (a) & 5(a) and its voltage characteristic at different node is shown in Fig. 4(b) & 5(a).

In Fig.4 (a) implementation of this buffer, consist of extra transistor in the output inverter as compared to standard domino circuit. It consists of three clock transistor M1, M3 and M6. The drain of M6 is connected to the dynamic node and its source is connected to the gate of transistor M5. Using this technique, it avoid precharge pulse not to propagates to the output node. Operation of this circuit is explained by considering the

input logic. When input logic is low, dynamic node remains high regardless of operating phase and output node is kept low. When input is high, there are two different cases depending on the operating phase.

**(a)** During evaluation phase, dynamic node is discharge to ground. Transistor M4 turns ON and charges the output node to VDD. On the other hand, high clock turns ON the M6 which turns OFF the M5. M6 avoid short circuit current in the output inverter.

**(b)** During precharge phase, pull up transistor M1 turns ON and M3 turns OFF, dynamic node charged to VDD. Transistor M6 is OFF, which turns OFF the M5 and it helps the output node to hold the previous value. In this circuit topology, output node is isolated from ground during precharge phase means it helps to avoid propagation of precharge pulse to the output pulse.

In Fig.5 (a) buffer is similar to fig.4 (a) circuit except gate of M6 is connected to F\_Node through inverter. Advantage of this circuit is avoiding propagation of precharge pulse during precharge phase to the output node. Operation of the circuit is explained by considering the input logic. When input is low, F\_node voltage is low, dynamic node remains high regardless of operating phase and output node is kept low. When input is high, F\_Node voltage is similar to dynamic node voltage; there are two different cases depending on the operating phase.

**(a)** During evaluation phase, dynamic node and F\_Node is discharge to ground. Output node is charged to VDD by M4. M6 turns ON due to low voltage at F\_Node. M6 pass low dynamic voltage to the gate of M5, this turns OFF the M5.

**(b)** During precharge phase, transistor M3 is OFF, pull up transistor M1 precharge the dynamic node and F\_Node is charge to high voltage due to parasitic capacitance at this node. High voltage at F\_Node turns OFF the transistor M6, which turns OFF the M5 and it helps the output node to hold its previous value.

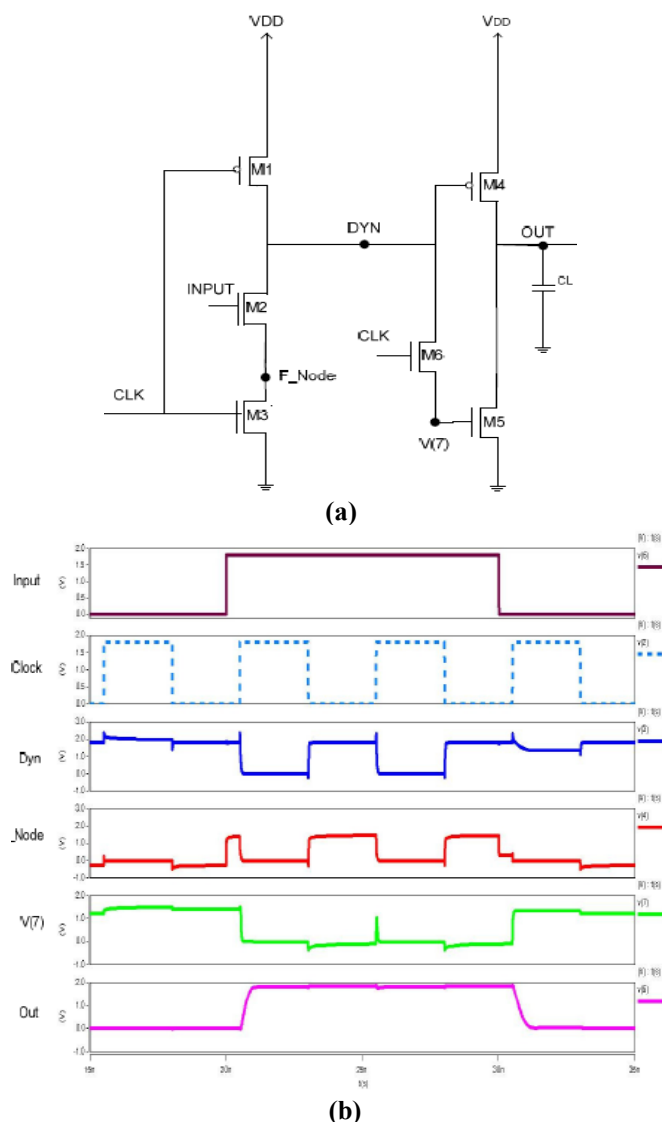


Fig. 4. (a) Domino logic circuit using the PDB, (b) Its selected node characteristics

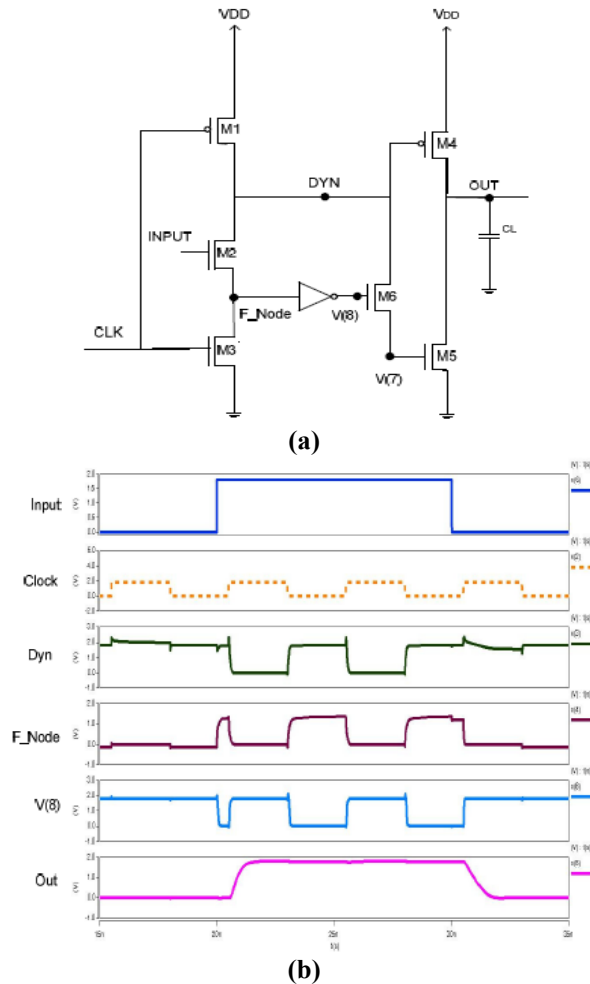


Fig. 5. (a) Domino logic circuit using the PDB, (b) Its selected node characteristics.

### III. Proposed domino circuit

To illustrate the issue of performance degradation due to the propagation of the precharge pulse inherent in domino logic gates. The proposed circuit PDB-based implementation overcomes this problem using the circuit structure shown in Fig.6 (a). This buffer is similar to fig. 1(a) and Fig.2 (a) circuit except gate of M5 is connected to A through inverter. Advantage of this circuit is avoiding propagation of precharge pulse during precharge phase to the output node. Operation of the circuit is explained by considering the input logic. In the designed implementation of the buffer, the source of the buffer's NMOS transistor M5 is connected to inverter. Using such a circuit topology, the value at node Z cannot propagate to the output F during the precharge phase of the gates since during this phase, the evaluation transistor M3 is turned off. For our designed gate, when the input logic A is low, the floating node Z is always high and then, the output node F is kept low regard less of the operating phase. On the other hand, if the input A is high, the precharge and evaluation phases will lead to the following situation:

- During the evaluation phase, node Z is discharged to Gnd as well as node B, resulting in enabling the PMOS transistor M4, while pulling up the output F to Vdd.
- During the precharge phase, node Z is charged up to Vdd, followed by the voltage at node B. Since the NMOS evaluation transistor M2 is disabled, the output node Z is held high.

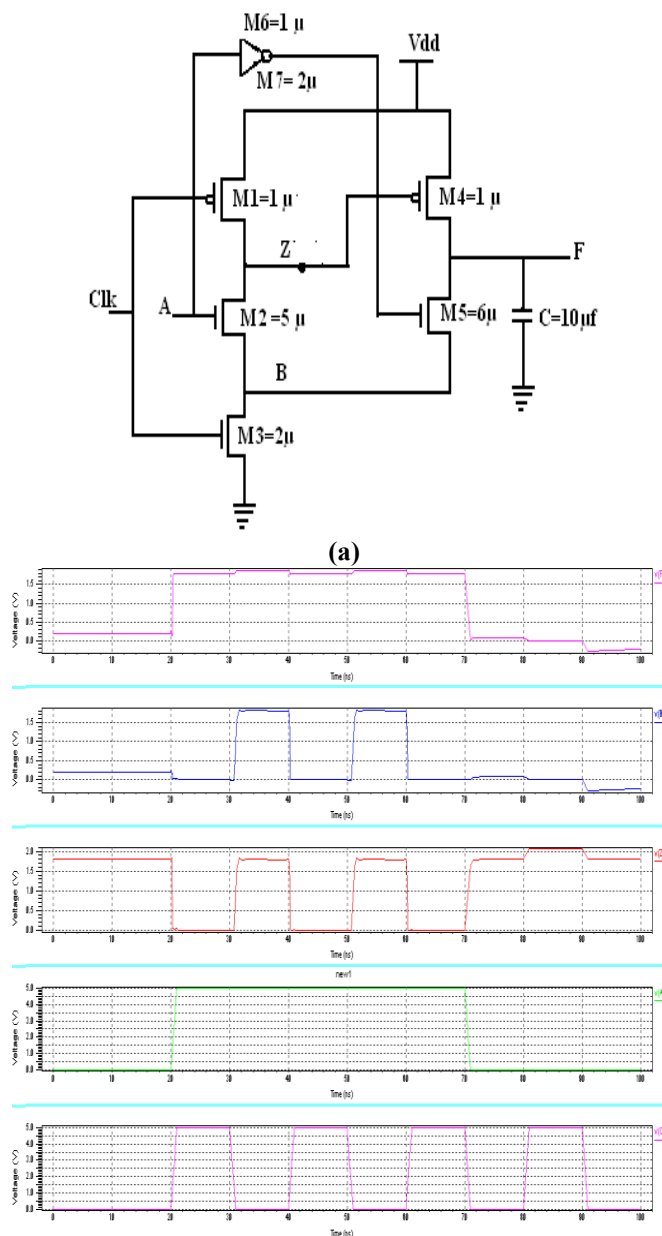


Fig.6 (a) proposed Dynamic Buffer (b) Waveform of proposed dynamic buffer.

#### IV. Simulation Results

In order to validate the claimed power saving of our proposed domino logic, extensive simulations were performed using a set of logic circuits as illustrated in Table 1. In this comparison, the clock frequency, the supply voltage and the load capacitance were set to 100 MHz, 1.8 V and 10 fF, respectively.

Table 1: Power and delay savings comparison for different load capacitances in 0:18 nm technology.

Dynamic Buffer	Total delay (n)	Power consumption(f)	PDP
Fig.1	3.58	7.45	26.67
Fig.2	2.59	3.91	10.12
Fig.3	2.06	9.47	19.50
Fig.4	3.43	6.95	23.83
Fig.5	2.90	7.38	21.40
Fig.6(pro)	2.55	6.10	15.55

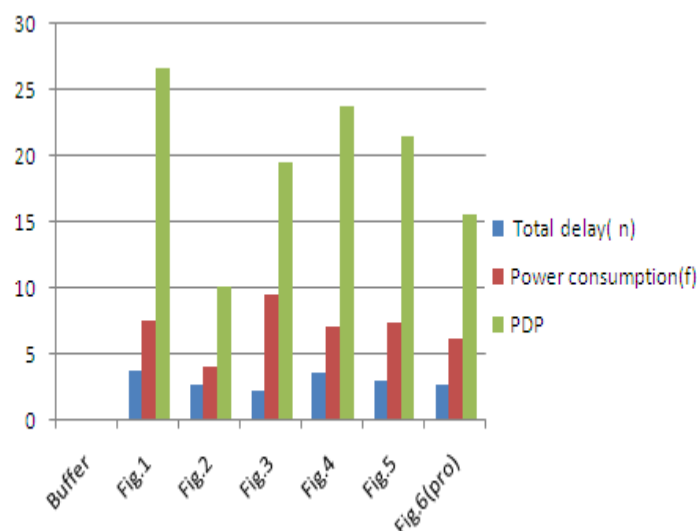


Fig.7 Delay, Power consumption and PDP comparison between the proposed domino circuits with standard domino circuit.

Comparison of power saving for various logic function of proposed circuits with domino circuit is tabulated in Table 2. In this comparison, clock frequency, input frequency and load capacitance were set to 200MHz, 50MHz and 100fF. From the table, increase of fan-in, increases the power consumption and OR gate logic consumes more power as compare to AND gate logic.

Table 2. Comparison of Power Saving with Different Logic Function to our proposed circuit in 0.18μm (VDD=1.8V, Clock Frequency=200MHz, Input Frequency=50MHz and load capacitance=100fF)

Logic Function	Standard Circuit Fig.1	Fig.4 Circuit	Fig.5 Circuit	Proposed Circuit Fig.6	Power saving by Proposed to Standard Circuit	Power saving by Proposed to Fig.4 Circuit	Power saving by Proposed to Fig.5 Circuit
A	46.04	31.86	45.95	12.95	71.87%	59.35%	71.81%
AB	46.57	33.09	46.00	25.90	44.17%	21.72%	43.69%
A-B	47.17	31.29	42.87	28.72	39.11%	8.21%	33.00%
ABC	47.24	34.64	46.50	35.33	33.71%	-1.95%	24.02%
A-B-C	48.20	30.97	42.96	35.91	25.49%	-15.95%	16.41%
ABCD	47.82	36.30	47.00	39.99	16.37%	-10.16%	14.91%
A-B-C-D	49.00	30.93	41.06	40.90	16.53%	-32.23%	0.38%

## V. Conclusions

In footed domino logic circuit, the precharge pulse is propagated to the output stage, which increases substantially the power and limits the cascading performance of the gate. In this paper new buffer circuit is proposed. This circuit is using to minimize the redundant switching at the output node and saves power as compared to the other the circuit discussed in literature. These circuits solve the problem of propagation of precharge pulse during precharge phase in standard domino circuit. The proposed circuits and domino circuit are simulated in 0.18μm using HSPICE. The performances structure is calculated by using 100MHz clock frequency and Input frequency 50MHz with load capacitor 100Pf.

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