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Implementation of High Reliable 6T SRAM Cell Design

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Abstract: *Memory can be formed with the integration of large number of basic storing element called cells. SRAM cell is one of the basic storing unit of volatile semiconductor memory that stores binary logic '1' or '0' bit. Modified read and write circuits were proposed in this paper to address incorrect read and write operations in conventional 6T SRAM cell design available in open literature. Design of a new highly reliable 6T SRAM cell design is proposed with reliable read, write operations and negative bit line voltage (NBLV). Simulations are carried out using MENTOR GRAPHICS.*
Keywords: *Memory, Read, Write, SRAM, NBLV.*

I. Introduction

A random-access memory is a class of semiconductor memory in which the stored data can be accessed in any fashion and its access time is uniform regardless of the physical location [1,2]. RAM can be classified based on the storage mode of the memory: volatile and non-volatile memory. Volatile memory retains its data as long as power is supplied, while non-volatile memory will hold data indefinitely [3,4]. RAM is referred as volatile memory, while ROM is referred as nonvolatile memory. Memory cells used in volatile memories can be further classified into static or dynamic structures. Static RAM (SRAM) cells use feedback (or cross coupled inverters) mechanism to maintain their state, while dynamic RAM (DRAM) cells use floating capacitor to hold charge as a data. The charged stored in the floating capacitor is leaky, so dynamic cells must be refreshed periodically to retain stored data[5]. The positive feedback mechanism, between two cross coupled inverters in SRAM provides a stable data and facilitates high speed read and write operations. However, SRAMs are faster and it requires more area per bit than DRAMs. SRAMs continue to be critical components across a wide range of microelectronics applications from consumer wireless to high performance server processors, multimedia and System on Chip (SOC) applications[6]. It is also projected that the percentage of embedded SRAM in SOC products will increase further from the current 84% to as high as 94% according to the International Technology Roadmap for Semiconductors (ITRS). This trend has mainly grown due to ever increased demand of performance and higher memory bandwidth requirement to minimize the latency.

II. Conventional 6T SRAM Cell Design

SRAM cell is the key component in memories. A typical SRAM cell uses two cross-coupled inverters forming a latch and access transistors for enabling access to the cell during read and write operations and provide cell isolation during the not-accessed state. SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention) as long as cell is powered. Conventional 6T SRAM cell design is shown in figure-1, four transistors (q1−q4) comprise cross-coupled cmos inverters and two nmos transistors q5 and q6 provide read and write access to the cell.

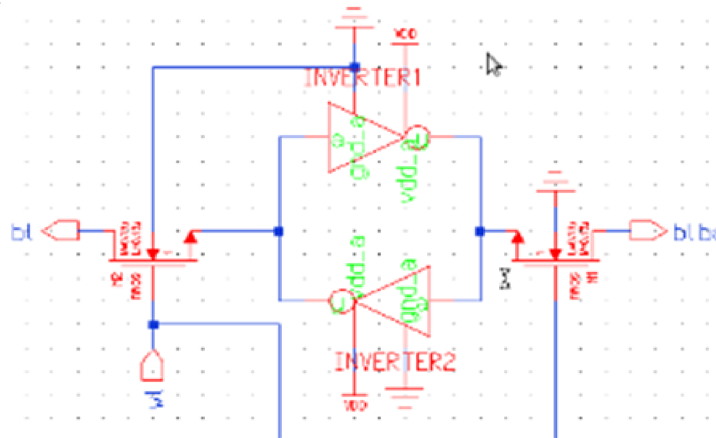

Figure 1: Conventional 6T SRAM cell design

From the open literature survey the main disadvantage of conventional 6T SRAM cell is not having an individual write and read circuits.

III. Read Operation

In this paper new read and write circuits are proposed to overcome the disadvantages in conventional 6T SRAM cells[7].A new read circuit is proposed which is shown in figure 2 in which individual read operation will be performed and the bit lines are precharged to VDD. The read operation is initiated by enabling the word line (WL) and connecting the precharged bit lines, BL and BLB, to the internal nodes of the cell[8]. Upon read access, the bit line voltage VBL remains at the precharge level. The complementary bit line voltage VBLB is discharged through transistors Q1 and Q5 connected in series. Effectively, transistors Q1 and Q5 form a voltage divider whose output is now no longer at zero volt and is connected to the input of inverter Q2−Q4. Sizing of Q1 and Q5 should ensure that inverter Q2−Q4 do not switch causing a destructive read.

Before reading a value from the storage nodes, both bit lines (BL) are pre-charged to VDD. The word line is then asserted to VDD. The storage node that stores a 1 will stay at 1 since it is connected to a pre-charged bit line [9]. The storage node that stores a 0 is statically connected to ground and will drain the charges on the bit line, which means that the bit line has just read a 0. Note that at the instant when the word line is turned on, the storage node that stores a 0 will jump to an intermediate voltage because there is now a current path from the bit line to Ground[10].

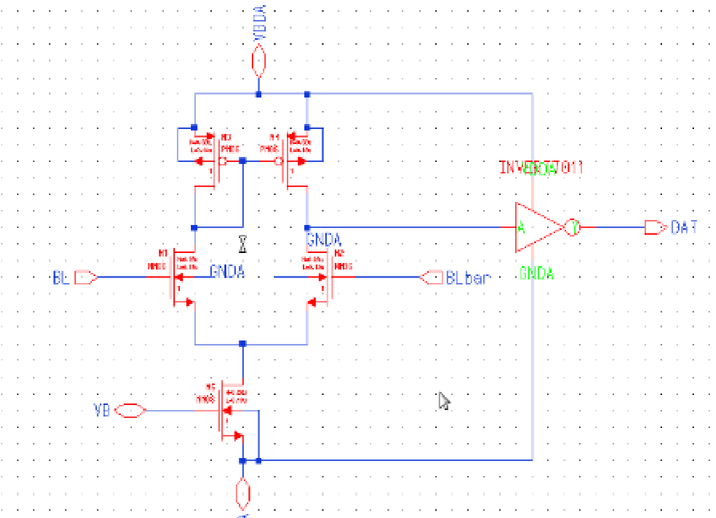

Figure 2: Proposed Read circuit for conventional 6T SRAM cell design

The intermediate voltage is determined by voltage dividers constructed by one of the access transistors and the NMOS transistors (M1 or M3) of the cross-coupled inverters. Since the storage nodes are coupled, intermediate voltage should not jump too high, otherwise it will invert the data stored at the other storage node. Therefore, the NMOS transistors of the cross-coupled inverters are made larger than the access transistors to ensure that the intermediate voltage does not flip the content of the other storage node[11].

Write operation:

Standard write operation of a 6T SRAM cell is performed using a NOR logic, by lowering one of the BITLINE to ground. To write a '0' BL is lowered, while writing a '1' also requires BL is to be lowered. When writing a '1' the cell has a'0'stored. The last operational state of the SRAM is the writing operation, during which the system has to have the ability to successfully write new data to the bit-cells[12]. The new data might be the same as or opposite of the stored ones, nevertheless, opposite data is always assumed as it involves more actions (e.g. flipping the cells) and hence it represents the worst case writing. Based on that successful writing involves discharging the node holding high voltage, through its corresponding bit-line, below the opposite inverter trip point within the time when access transistors are enabled. Write driver is the component in charge of driving the bit-line to discharge that node, where the final voltage of the high voltage node is determined by the voltage divider between the corresponding pull-up transistor and access transistor. Moreover, since the access transistors are enabled for a limited time only, the final voltage is also affected by the discharging current, that is the difference in ON current between the pull-up and access transistor. Proposed write circuit for correct write operation is shown in figure 3 .Modified conventional 6T SRAM with both proposed write and read circuits is presented in figure 4. Read and write operation of the 6T SRAM with the proposed circuit are presented in figure 5&6 respectively. In this write operation is based on BITLINE and BITLINE BAR. The

WORDLINE will raise either from 0 to 1 or 1 to 0 for high reliable write operation. Conventional 6T SRAM cell has been widely used in the implementation of high performance microprocessors and on-chip caches. However, aggressive scaling of CMOS technology presents a number of distinct challenges for embedded memory fabrics.

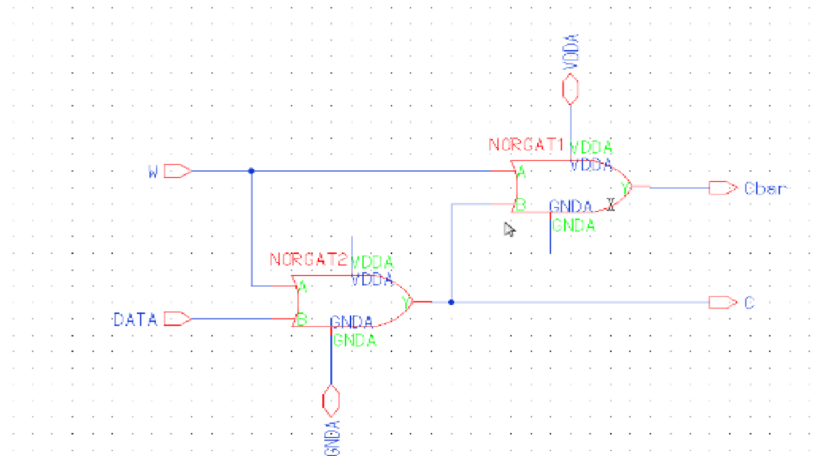

Figure 3: Write circuit of a 6T SRAM cell.

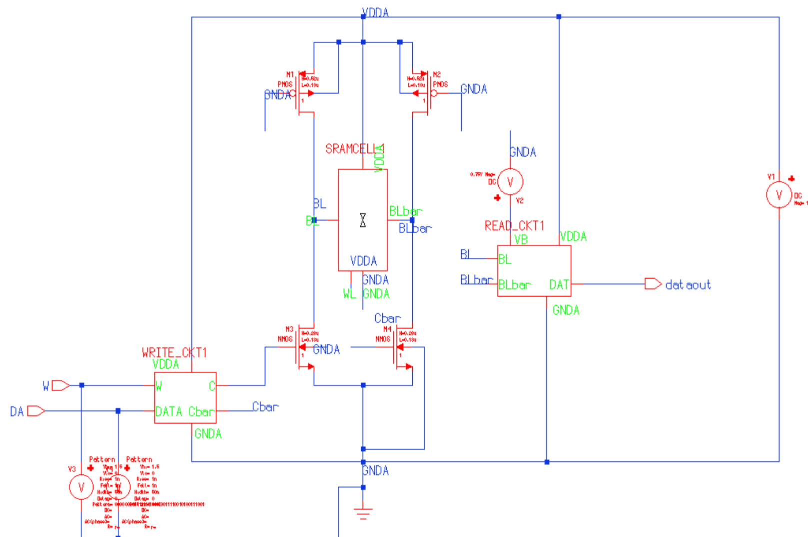

Figure 4: 6T SRAM cell with proposed Read and Write circuits

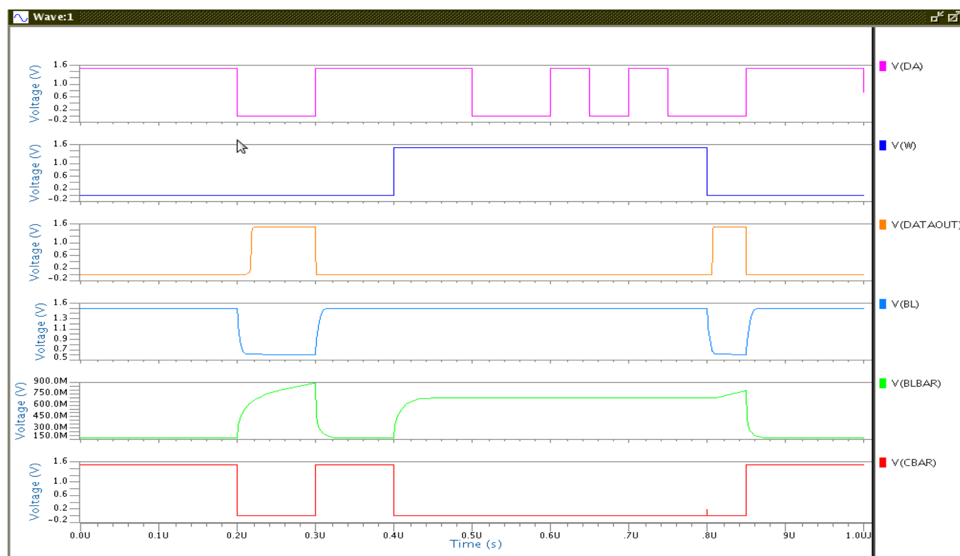

Figure 5: Waveform of Read operation of 6T SRAM cell

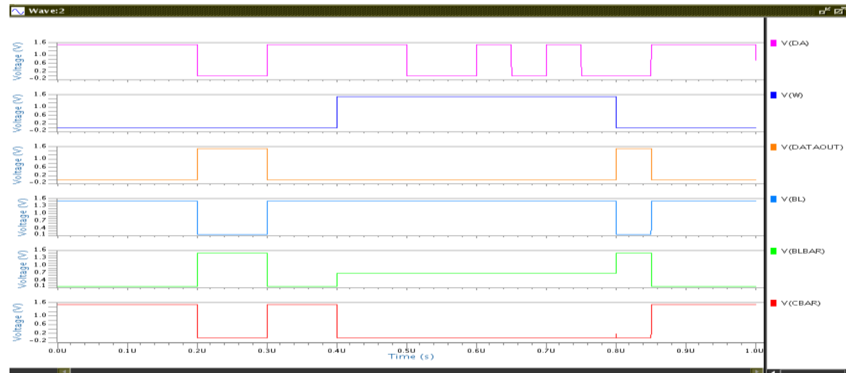

Figure 6: Waveform of Write operation of 6T SRAM cell

The stability of the circuit depends on the inputs and number of transistors used. To reduce number of inputs and to increase the stability a new modified 6T SRAM is presented in figure 7.

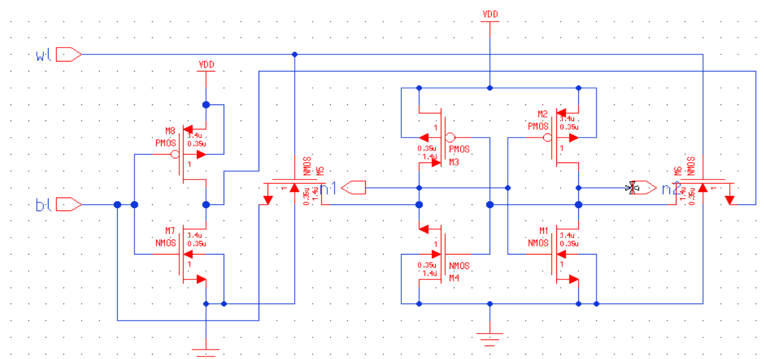

Figure 7: 6T SRAM using a inverter as a power source.

A pulse voltage and DC voltage is given to inputs and its error report is verified for the results of dc analysis and transient analysis at different voltages from 0.5v to 2.5v with WL variation from 20ns to 60ns. From the results it can be observed that perfect write operation is derived.

Write operation will be observed with the terms of BL, BLBAR and WL when applying the inputs BL and BLBAR will be in opposite condition and WL should raise either from 0 to 1 or from 1 to 0. In the above circuit the voltage constraint is reduced using inverter condition but it consume more area than the conventional 6T SRAM cell. So, a new design is proposed which uses transmission gates in place of pass transistors.

IV. Proposed 6T SRAM Cell Design

The proposed SRAM cell is shown in Figure 8, it consists of two transmission gates in place of pass (access) transistors. The transmission gates have low voltage drop compared to pass transistors. The additional NMOS in the circuit acts as a switch and also it is necessary to restrict a short circuit current when the data is written in the elementary cell. Read and Write circuits presented in figure 3&4 can be used with proposed 6T SRAM cell design.

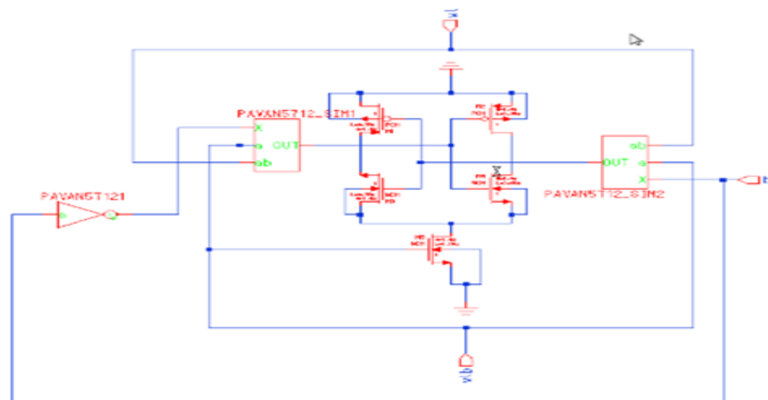

Figure 8: Proposed 6T SRAM with transmission gates

If more negative voltage peak is generated by negative bit line voltage, less will be reliability of the circuit. To overcome this problem, a capacitor is connected (whose other end is connected to ground) to the output of the NBLV generator which increases the absolute capacitance of the NBLV. This capacitor works as a low pass filter which smoothes out the negative voltage spike. When level of negative voltage spike decreases, VGS of MOSFET reduces which reduces the strength of electric field. Due to low strength of electric field, there will be very low chances of dielectric breakdown and hence less chances of transistors to get damaged, hence reliability of the circuit is increased.

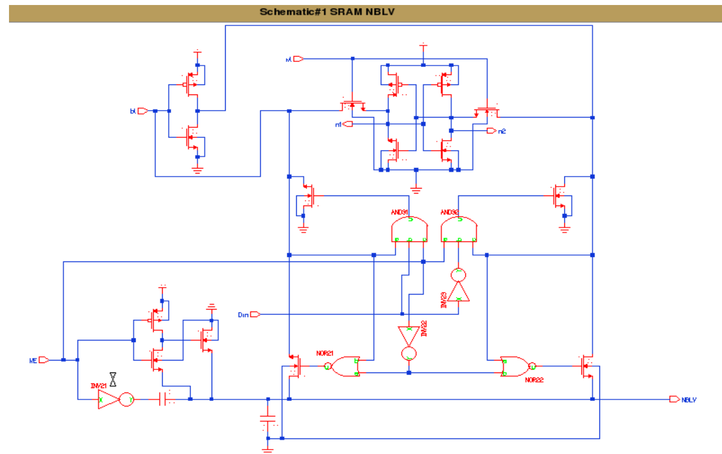

Figure 9: 6T SRAM with NBLV circuit

In the above NBLV circuit the 6T SRAM cell is used for write assist scheme and verified the write operation to increase the reliability of the circuit.
Level of negative voltage generated by NBLV generator is reduced. But due to this reduced level of negative bit line voltage, the assisting effect of NBLV write assist scheme reduces which may cause the memory to fail. So, this reduced influence of assist circuit needs to be compensated to achieve high write ability and hence high efficiency of the SRAM. By implementing the NBLV schemes with 6T SRAM cell together high reliability as well as write ability can be achieved.

Results

Simulations are carried out using MENTOR GRAPHICS tools using 130nm technology. . Observed the results using both DC and transient response . DC output response, write failure and correct write operations waveforms are shown in figure 10, 11& 12 respectively, write operation of 6T SRAM using NBLV is presented in figure 13.

Comparison of delay & power dissipation for the conventional and proposed 6T SRAM is presented in table 1

Table 1: Comparison between conventional and proposed 6T SRAM

Parameters	Conventional 6TSRAM	Proposed 6TSRAM
Delay	**32.7ps**	**24.3ps**
Power dissipation	**541.62µw**	**483µw**

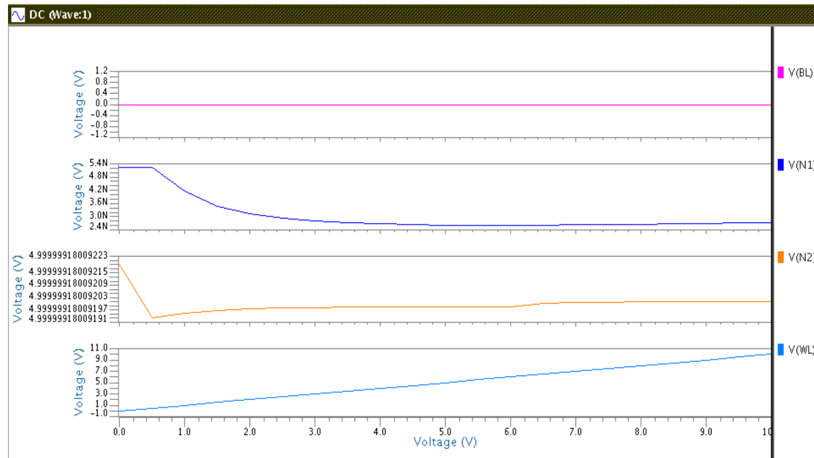

Figure 10: DC output of a proposed 6T SRAM cell.

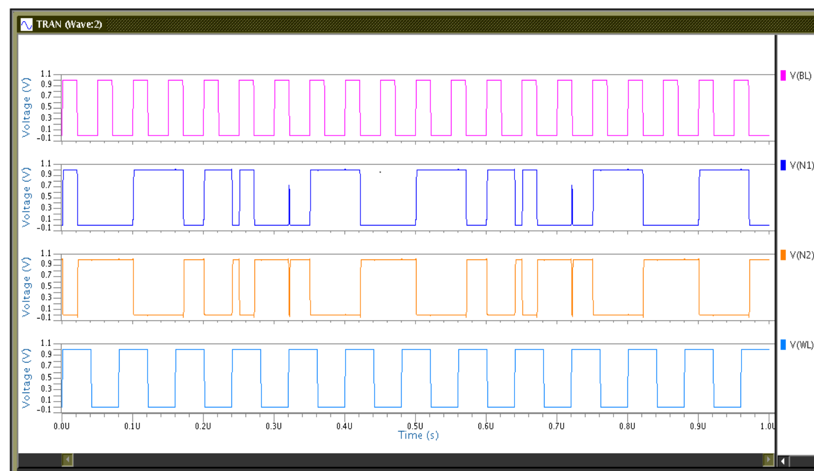

Figure 11: Transient ouput write failure case

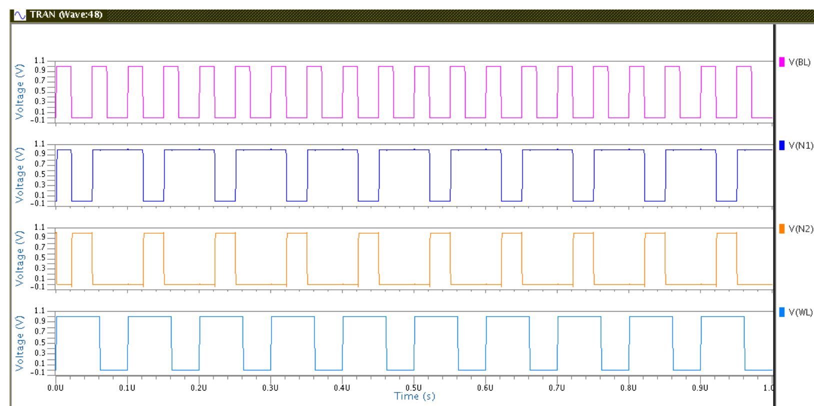

Figure 12: Transient output correct write operation.

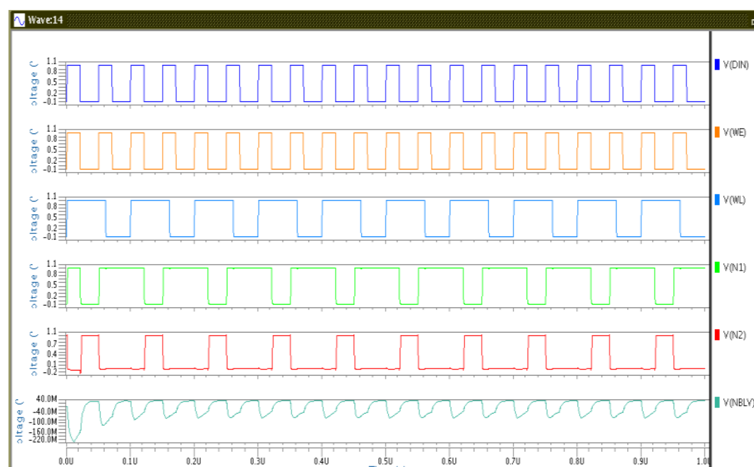

Figure 13: Write operation waveform of NBLV.

V. Conclusion

Implemented to obtain correct read and write operations compared to conventional 6T SRAM. To improve the stability SRAM using an inverter, to reduce power consumption and 6T SRAM using transmission gates are proposed and to improve reliability SRAM with NBLV circuit is also implemented. From the results it is evident that the proposed 6T SRAM is more stable, reliable, dissipates less power and delay is also reduced. The proposed circuit is very useful in system in chip applications.

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