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VLSI Implementation of Vedic Multiplier Using Urdhva–Tiryakbhyam Sutra in VHDL Environment: A Novelty

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Abstract: *This paper anticipated the design of a novel Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing system as well as in general processors. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. In this paper, we proposed an 8-bit multiplier using the new methodology of Vedic Mathematics called as Urdhva-Tiryagbhyam sutra which is used for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. This paper depicts the design of an efficient 8×8 binary arithmetic multiplier by using Vedic Mathematics. From various multiplication techniques, Urdhva-Tiryagbhyam sutra is being implemented because this sutra is applicable to all cases of algorithms for N×N bit numbers and the minimum delay is obtained. A 4×4 Vedic Multiplier is designed using 9 –full adder and a special 4-bit adder which is having reduced delay. Then 8-bit multiplier is designed using four 4-bit multiplier and 3-ripple carry adder. Then 8×8 Vedic Multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE8.2 Software. Finally the objective of this paper lies in design of an efficient vedic multiplier using Urdhva–Tiryakbhyam Sutra in VHDL Environment.*

Index Terms- *Vedic Mathematics, Vedic Multiplier, Urdhva Tiryagbhyam, Digital Signal Processing, VLSI Signal Processing,VHDL,*

I. Introduction

With the up-to-the-minute encroachment of VLSI technology the insist for portable and embedded digital signal processing (DSP) systems has increased efficiently.Multipliers are key components of many high performance systems such are FIR filters, Microprocessors, Digital Signal Processors etc.In order to perform multiplications,a large number of adders or components are used.The ancient system of mathematics named as Vedic mathematics was rediscovered from the Vedas.In contrast to conventional mathematics,Vedic mathematics is simpler and easy to understand.In 1884 Swami BharatiKrishna TirthajiMaharaj re-introduced the concept of ancient system of Vedic mathematics.The utterance 'Vedic' is consequential from the word 'Veda ‘which earnings the store-house of all knowledge.The Vedic mathematics includes sixteen-sutras or formulae and thirteen sub-sutras.The variety of applications of Vedic mathematics includes theory of numbers, compound multiplication, algebraic operation, calculus, squaring, cubing, cube root, simple quadratic, coordinate geometry and wonderful Vedic Numeric Code.So we can interpret as Vedic mathematics is a sphere of influence which presents various effective algorithms that can be applied in different twigs of engineering such as digital signal processing ,computing and especially VLSI Signal Processing applications.In the present world all the signal and data processing operations involves multiplication.Though speed is an important factor in the 3-dimensional VLSI problem and also a constraint in the multiplication operation ,So increase in speed can be achieved by sinking the number of steps in the computation process.Hence the efficiency of the system can be evaluated by the help of Speed and area consumed by the components. of multiplier determines the efficiency of a system.

II. Background & Related Works

Multipliers are important components in processor design. R.panda,M.pradhan[16] presents the concepts behind the "Urdhva Tiryagbhyam Sutra" and "Nikhilam Sutra" multiplication techniques.It then shows the architecture for a 16×16 Vedic multiplier module using Urdhva Tiryagbhyam Sutra.This paper then extends multiplication to 16×16 Vedic multiplier using "Nikhilam Sutra" technique. The 16×16 Vedic multiplier module

using Urdhva Tiryagbhyam Sutra uses four 8×8 Vedic multiplier modules; one 16 bit carry save adders, and two 17 bit full adder stages. The carry save adder in the multiplier architecture increases the speed of addition of partial products. The 16×16 Vedic multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE 10.1 software. This multiplier is implemented on Spartan 2 FPGA device XC2S30-5pq208. The performance evaluation results in terms of speed and device utilization are compared with earlier multiplier architecture.

A high speed squaring circuit for binary numbers [17] is proposed. High speed Vedic multiplier is used for design of the proposed squaring circuit. The key to our success is that only one Vedic multiplier is used instead of four multipliers reported in the literature. In addition, one squaring circuit is used twice. Our proposed Squaring Circuit seems to have better performance in terms of speed.

This paper bring out a 32X32 bit reversible Vedic multiplier [18]using "Urdhva Tiryakabhayam" sutra meaning Vertical and crosswise, is designed using reversible logic gates, which is the first of its kind. Also in this paper we propose a new reversible unsigned division circuit. This circuit is designed using reversible components like reversible parallel adder, reversible left-shift register, reversible multiplexer, reversible n-bit register with parallel load line.The reversible vedic multiplier and reversible divider modules have been written in Verilog HDL and then synthesized and simulated using Xilinx ISE 9.2i. This reversible vedic multiplier results shows less delay and less power consumption by comparing with array multiplier.

This paper describes [9] Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool"-A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool - XilinxISE12.1i.

Poornima M, Shivaraj Kumar Patil et.al explains the concept behind [2]"Implementation of multiplier using vedic algorithm"-Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic Mathematics has a unique technique of calculations based on 16 Sutras. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. Further, the Verilog HDL coding of Urdhvatiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3 kit have been done and output has been displayed on LED's of Spartan 3 kit.

Anju& V.K. Agrawal presents [4]"Implementation of Low Power and High Speed Vedic Multiplier using Vedic Mathematics"-High-speed parallel multipliers are one of the keys in RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), and graphics accelerators and so on. Array multiplier, Booth Multiplier and Wallace Tree multipliers are some of the standard approaches used in implementation of binary multiplier which are suitable for VLSI implementation. A simple digital multiplier (henceforth referred to as Vedic Multiplier in short VM) architecture based on the UrdhvaTiryakbhyam (Vertically and Cross wise) Sutra of Vedic Mathematics is presented. An improved technique for low power and high speed multiplier of two binary numbers (16 bit each) is developed. An algorithm is proposed and implemented on 16nm CMOS technology. The designed 16x16 bit multiplier dissipates a power of 0.17 mW. The propagation delay time of the proposed architecture is 27.15ns. These results are many improvements over power dissipations and delays reported in literature for Vedic and Booth Multiplier.

"Design and Implementation of Vedic Multiplier" this paper explains about a novel multiplier architecture based on ROM approach using Vedic Mathematics is proposed. This multiplier's architecture is similar to that of a Constant Coefficient Multiplier (KCM). However, for KCM one input is to be fixed, while the proposed multiplier can multiply two variables. The proposed multiplier is implemented on a Cyclone III FPGA, compared with Array Multiplier and Urdhava Multiplier for both 8 bit and 16 bit cases and the results are presented. The proposed multiplier is 1.5 times faster than the other multipliers for 16x16 case and consumes only 76% area for 8x8 multiplier and 42% area for 16x16 multiplier.

"Design of High Speed, Area Efficient, Low Power Vedic Multiplier using Reversible Logic Gate"-A systems performance is generally determined by the speed of the multiplier since multiplier is one of the key hardware component in high performance systems such as FIR filters, digital signal processors and

microprocessors etc. Multipliers have large area, long latency and consume considerable power. Hence good multiplier architecture increases the efficiency and performance of a system. Vedic multiplier is one such high speed, low area multiplier architecture. Further implementing this in reversible logic reduces power. In this paper a 4 X 4 Vedic multiplier is designed using a reversible logic gate which is efficient in terms of constant inputs, garbage outputs, quantum cost, area, speed and power. The design is simulated using Verilog.

III. Urdhva-Tiryakbhyam:A Novel Vedic Sutra

The word "Urdhva-Tiryakbhyam" resources vertical and crosswise multiplication.This multiplication formula is pertinent to all cases of algorithm for N bit numbers .Conventionally this sutra is used for the multiplication of two numbers in decimal number system. The same concept can be applicable to binary number system which is being discussed in this paper. Advantage of using this type of multiplier is that as the number of bits increases, delay and area increases very slowly as compared to other multipliers.

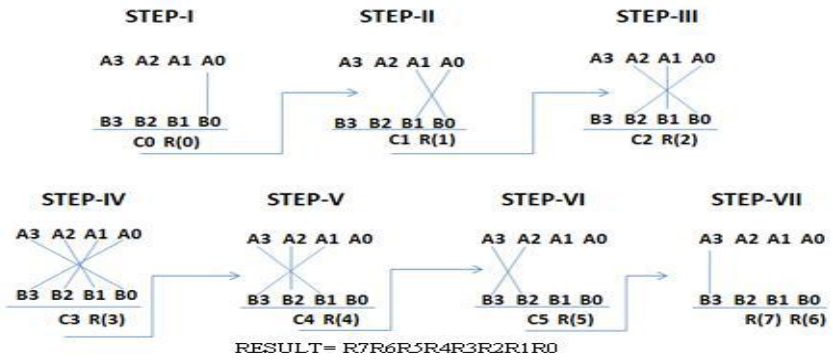


Figure.1 Multiplication method of Urdhva-Tiryakbhyam.

In the above figure-1, 4-bit binary numbers A0A1A2A3 and B0B1B2B3 are considered. The result obtained is stored R0R1R2R3R4R5R6R7.In the first step [A0, B0] is multiplied and the result obtained is stored in R0. Similarly in second step [A0, B1] and [A1, B0] are multiplied using a full adder and the sum is stored in R1 and carry is transferred to next step. Likewise the process continues till we get the result.

IV. Proposed Design Scheme Of Multipliers

(i) 4-Bit Multipliers

The 4×4 Vedic multiplier in binary is implemented by using VHDL code.In order to reduce the delay of 4×4 multiplier, it is designed by using nine full adders and a 4-bit special adder.

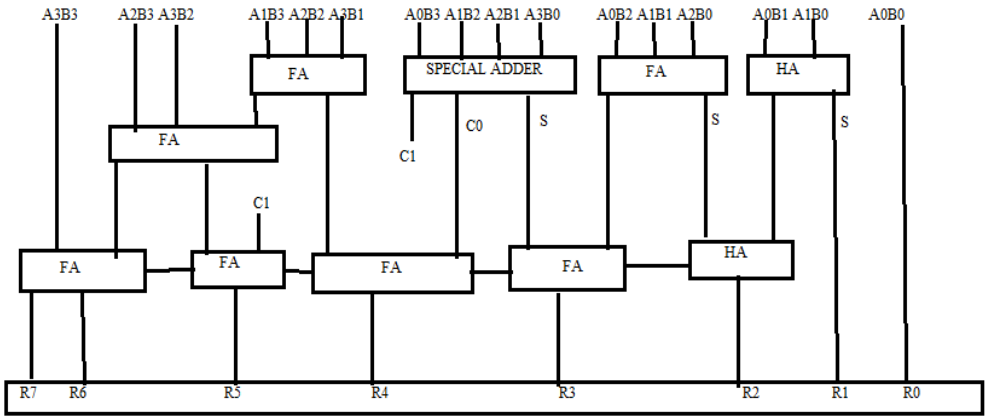


Figure.2 Architecture of 4×4 Vedic Multiplier

Special Adder in 4*4 multiplier

Figure.3 Architecture of 4-Bit special adder.

In the figure-3 A,B,C,D are four inputs.C0 and C1 are LSB and MSB of carry outputs respectively and Sum is the sum of four inputs. The Boolean expressions for the same are given below.

Sum<= p XOR q XOR r XOR s
c0<= ((NOT q) AND s)OR (r AND (NOT s))OR (q AND (NOT r))
c1<= p AND q AND r AND s

(ii) 8-Bit Multiplier

The 8×8 Vedic multiplier in binary is implemented using VHDL code. For reducing the delay of 8×8 multiplier, it is implemented using four Vedic 4*4 blocks and a ripple carry adder.

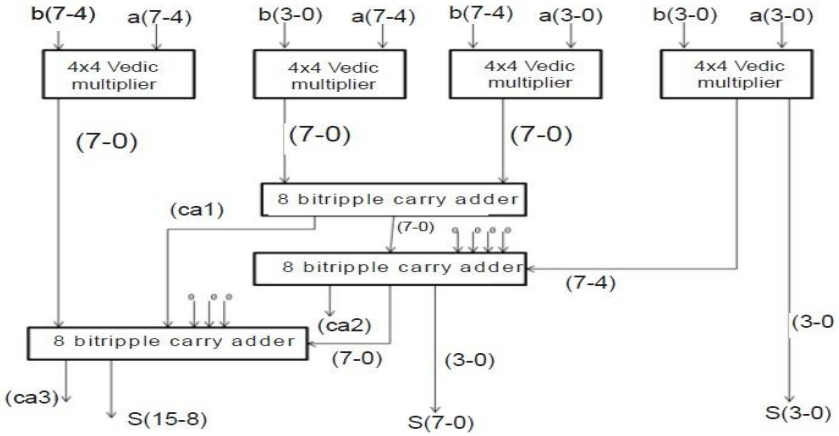


Figure.4 Architecture of 8×8 Vedic Multiplier.

P=AxB=(AH-AL)x(BH-BL)
=AHxBH+(AHxBL+ALxBH)+ALxBL

Special Adder in 8*8 multiplier: RCA

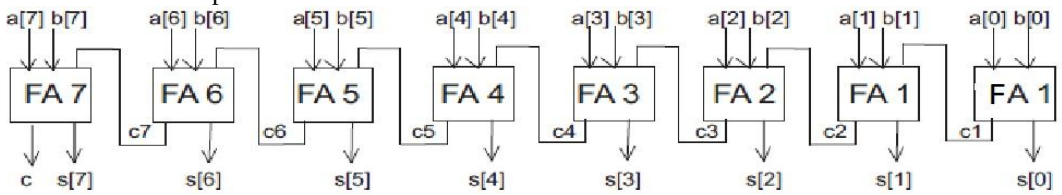


Figure.5 Architecture of Ripple carry adder.

The ADDER-1 in figure-5 adds the 8-bit outputs from the second and third multiplier blocks and uses eight full adders which are connected in ripple carry adder form.

V. Result And Discussion

The proposed 4 bit adder and 4X4 Vedic multiplier as well as 8x8 Multiplier using Urdhva–Tiryakbhyam Sutra in binary are implemented using VHDL language.. The entire code is completely synthesizable.The synthesis is done using Xilinx Synthesis Tool (XST) available with Xilinx ISE8.2.The below figure shows the simulated result with waveforms.

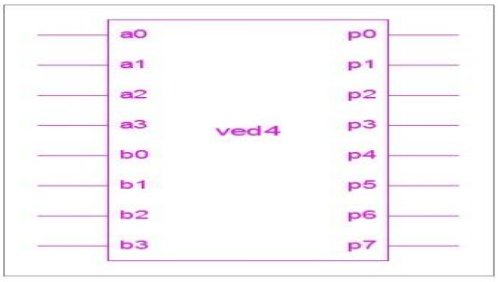


Figure.6 RTL block view of 4×4 Vedic Multiplier

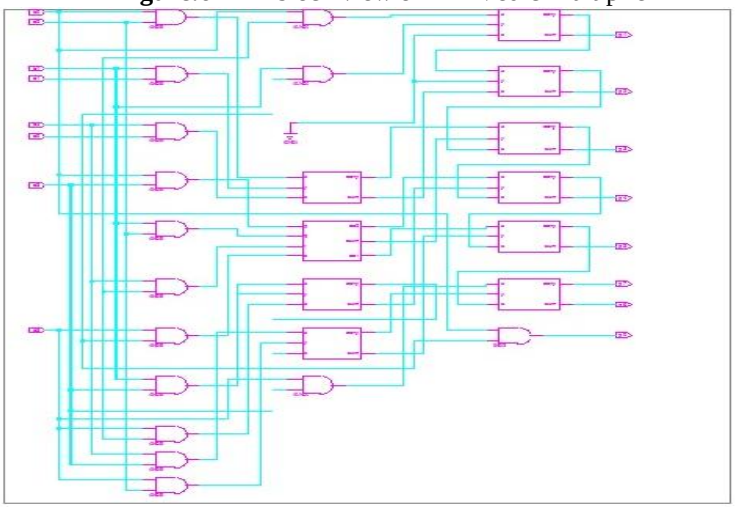


Figure.7 RTL circuit view of 4×4 Vedic Multiplier

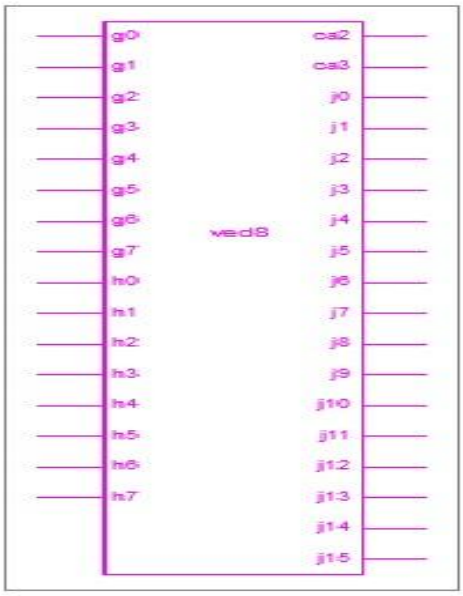


Figure.8 RTL block view of 8×8 Vedic Multiplier.

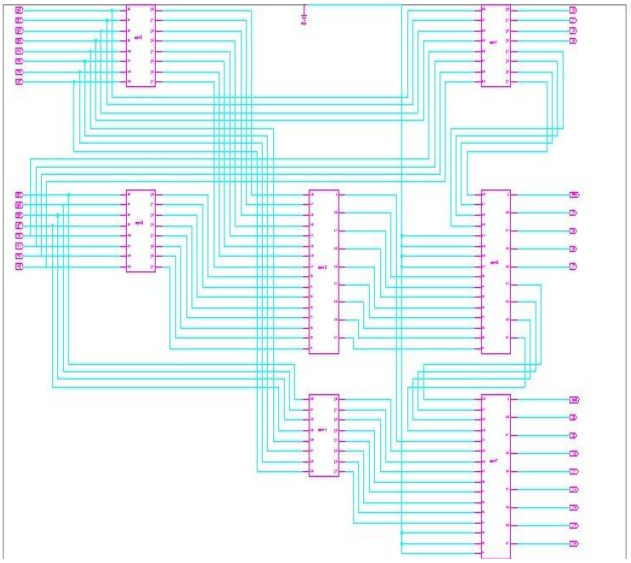


Figure.9 RTL circuit view of 8×8 Vedic Multiplier

Test Bench Waveform for 4x4 Vedic Multiplier

Example:

A= "1100" =12

B= "1111" =15

Result= 10110100 =180

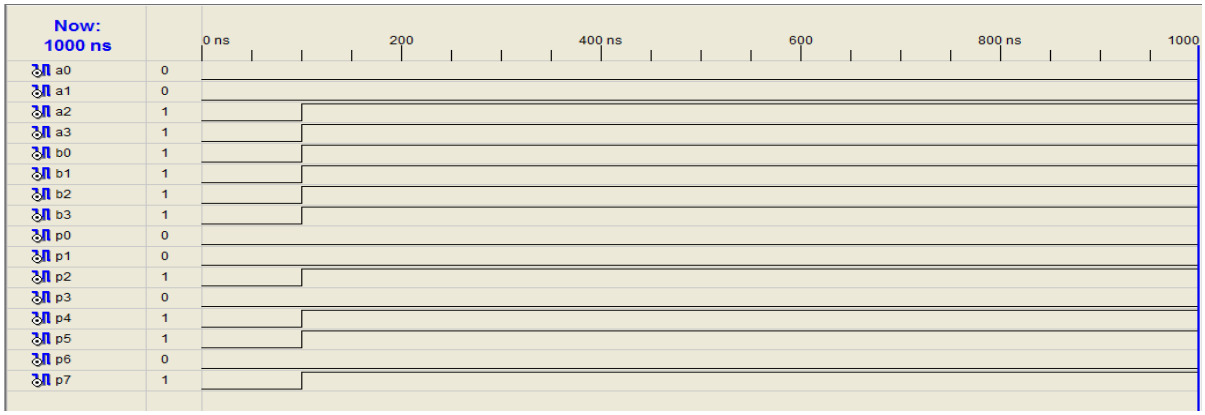


Figure.10 Test Bench Waveform of 4*4 Vedic Multiplier

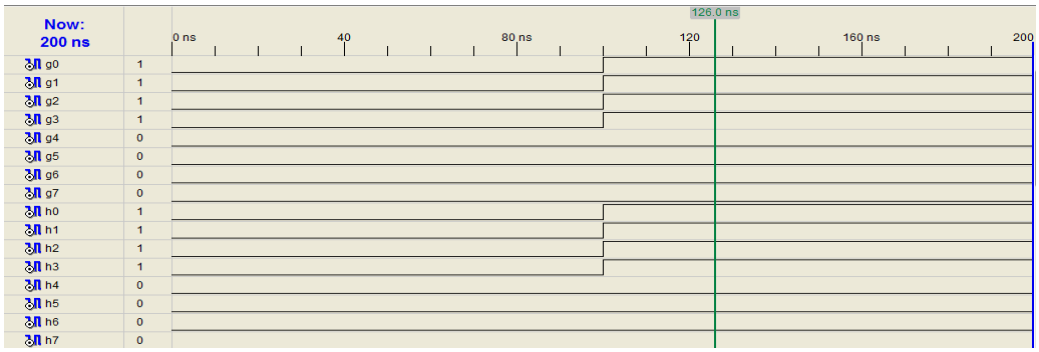
Test Bench Waveform for 4x4 Vedic Multiplier

Example:

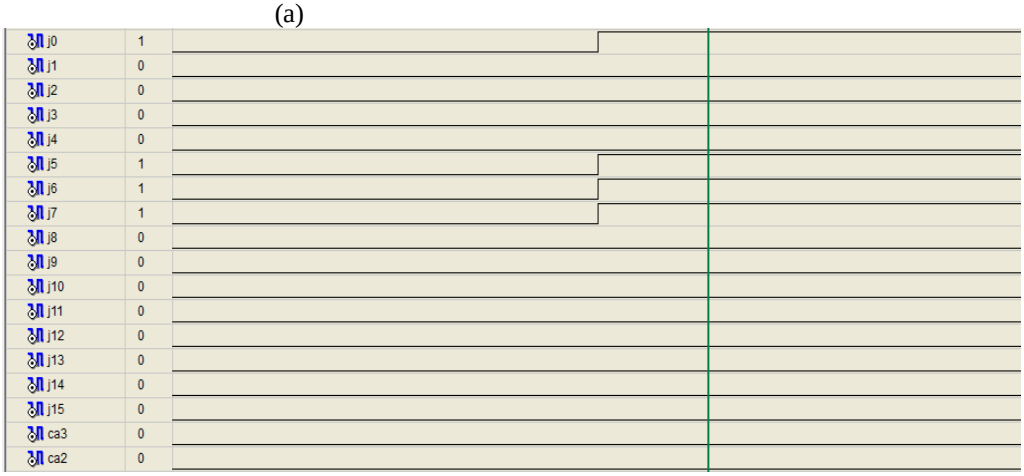
A="00001111" =15

B="00001111" =15

Result= 11100001 =225



(a)



(b)

Figure.11 Test Bench Waveform of 8*8 Vedic Multiplier(a) input(b)Output

SPECIFICATION/BITS	4*4 VEDIC MULTIPLIER	8*8 VEDIC MULTIPLIER
SPECIAL ADDER	4-BIT SPECIAL ADDER 4- I/P : 3- O/P I/P-(A,B,C,D) ; O/P- (SUM,C0,C1)	8-BIT RIPPLE CARRY ADDER 16 I/P : 16 O/P I/P- (a0- a7),(b0-b7) ; O/P – (S0-S15)
GATES USED	***SPECIAL ADDER*** • XOR : 3 nos • NOT : 3 nos • AND : 3 nos • OR : 2 nos ***FULL ADDER*** • XOR : 2 nos • AND : 3 nos	***RIPPLE CARRY ADDER*** ➢ HALF ADDER • XOR : 1 nos • AND : 1 nos ➢ FULL ADDER • XOR : 2 nos • AND : 3 nos ***VEDIC MULTIPLIER*** • XOR : 5 nos • AND : 9 nos • NOT : 3 nos • OR : 2 nos
BLOCKS	FULL ADDER : 9 nos SPECIAL ADDER : 1nos	4-BIT VEDIC MULTIPLIER : 4nos 8-BIT RIPPLE CARRY ADDER : 3 nos

Table.1 Device Utilizations in design of Vedic Multiplier using Urdhva–Tiryakbhyam Sutra

VI. Conclusion

The proposed Vedic Multiplier circuit using Urdhva-Tiryakbhyam Sutra can be implemented in arithmetic and logical units of a DSP processor replacing the traditional circuits. Generally the Vedic multipliers are much faster than the conventional multipliers. This gives us scheme for hierarchical multiplier design. So the design density gets condensed for inputs of large no of bits and modularity gets augmented .In summary, embodiments of the investigation provided in this work have led to the design of vedic multiplier for binary numbers using Urdhva-Tiryakbhyam Sutra.Urdhva tiryakbhyam, Nikhilam and Anurupye sutras are such vedic Sutras which can reduce the delay, power and hardware requirements for multiplication of numbers.Hence the designed multiplier can be used in various applications like digital signal processing,VLSI Signal Processing,encryption and decryption algorithms in cryptography etc.The proposed design can further be implemented for16x16,32x32 multipliers and their performance comparision with the help of FPGA.

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