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Performance Analysis Comparison of a Conventional Wallace Multiplier and a Reduced Complexity Wallace multiplier

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Abstract : *In this paper performance analysis comparison of a conventional wallace multiplier and a reduced complexity wallace multiplier is presented. Performance comparison is done in terms of power, delay, power delay product and complexity in terms of number of MOS transistors. The multipliers are designed by using Cadence virtuoso in 180nm CMOS technology and their performance characteristics are analysed. Performance improvement of the designed 4x4 bit reduced complexity wallace multiplier with respect to the designed 4x4 bit conventional wallace multiplier in terms of number of transistors, delay and power delay product are found to be 12.05%, 9.42% and 4.98% respectively.*

Keywords: *Power, Delay, Power delay product, Reduced complexity, Conventional wallace multiplier, Reduced complexity wallace multiplier.*

I. Introduction

A multiplier plays a vital role in any digital signal processors. There are different methods and architectures for designing a multiplier. Designing a multiplier by using wallace tree architecture is superior over other architectures in terms of performance characteristics [1-3]. A multiplier designed by using wallace tree architecture is known as a wallace multiplier [4]. Wallace multiplier consumes less power and its switching speed is faster as compared to other multiplier architectures. Researchers have shown interest on wallace multiplier, as result of which, different architectures are introduced to design a better wallace multiplier architecture. A conventional wallace multiplier and a reduced complexity wallace multiplier are two architectures among them. In this paper design and performance analysis of a conventional wallace multiplier and a reduced complexity wallace multiplier are discussed. Performance analysis is carried out by using Cadence Virtuoso in 180nm CMOS technology.

Fig. 1 shows the block diagram of a wallace multiplier. In this multiplier architecture, after generating the partial product, accumulation of partial product and final addition are done in different stages. When the final stage obtains only two rows, then final addition is done.

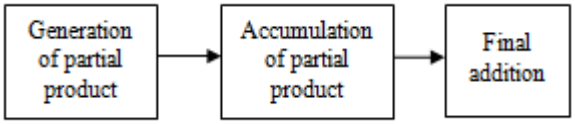

Fig. 1 Block diagram of a wallace multiplier

The number of rows of partial product in a particular stage can be expressed as [5]

$$R_{i+1} = 2(R_i/3) + R_i \bmod 3 \quad (1)$$

where, R_i gives the groups or stages and R_0 = N= number of bits.

II. Design of a conventional wallace multiplier

In a conventional wallace multiplier, partial products are generated first. Then these are accumulated in different stages by using eqn. (1). The procedure is repeated until last stage contains only two rows. A 4x4 bit conventional wallace multiplier is designed by using Cadence virtuoso in 180nm CMOS technology. The flowchart for designing a conventional wallace multiplier is shown in Fig. 2. The designed 4x4 bit conventional wallace multiplier is shown in Fig. 3. Design of the conventional Wallace multiplier is done in three steps:

i) Partial product generation
ii) Accumulation of partial product
iii) Final addition

For generating partial products, AND gates are used. The number of partial product in a 4x4 bit multiplier is 16. Hence total number of AND gates used are 16. After generating the partial product, these are accumulated in different stages by using eqn. (1). Both full adders and half adders are used for addition. When the last stage contains only two rows of partial products, then accumulation of partial product is stopped and final addition is done. In final stage, only full adders are used for addition.

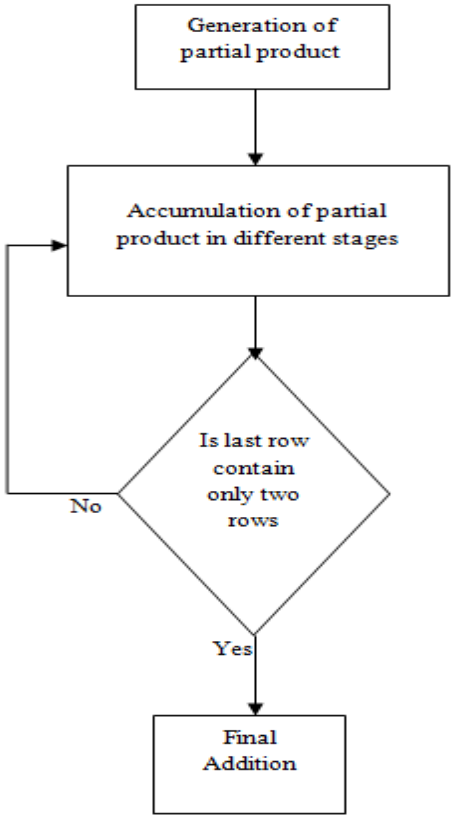

Fig. 2 Flowchart for designing a conventional wallace multiplier

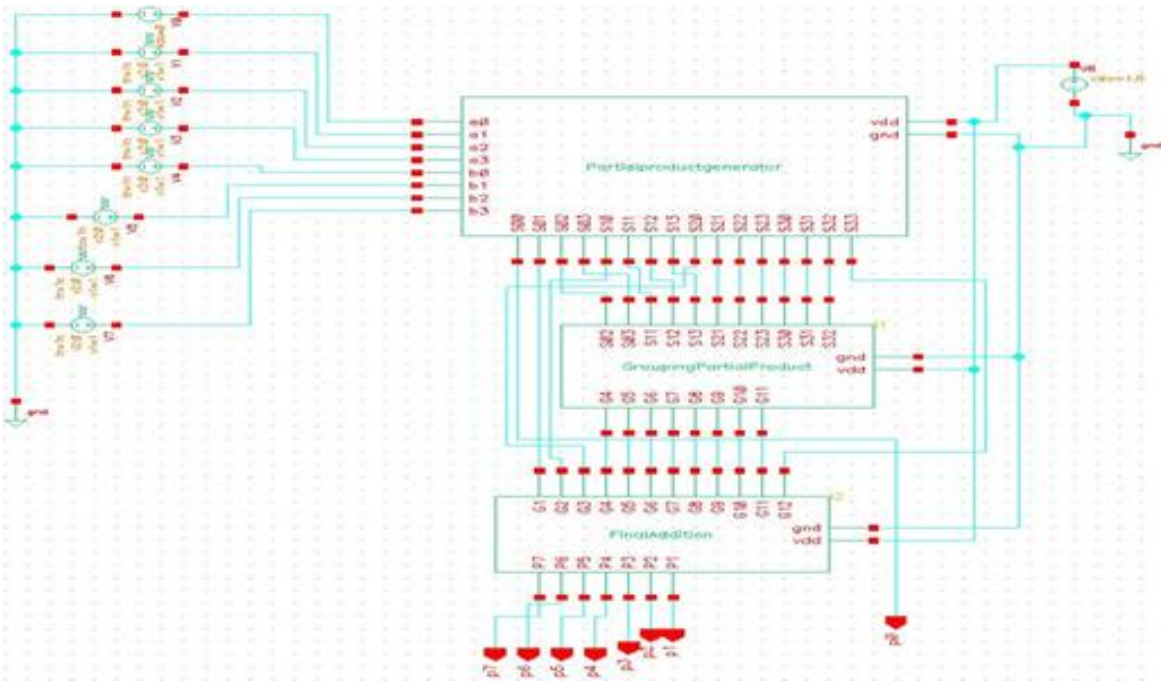

Fig. 3 A 4x4 bit conventional wallace multiplier

III. Design Of A Reduced Complexity Wallace Multiplier

In a reduced complexity wallace multiplier [5-6], partial product is generated first. Partial product of a 4x4 bit multiplication is shown in Fig. 4. The arrays of partial products are converted to inverted pyramid. The inverted pyramid is obtained by shifting the bits of left half of partial product in upward direction. The inverted pyramid of the partial product of a 4x4 bit multiplication is shown in Fig. 5. By using eqn. (1), partial products are accumulated in different stages. When the last stage contains only two rows of partial product, then final addition is computed. Reduced complexity Wallace multiplier reduces the number of half adders in the multiplier [7].

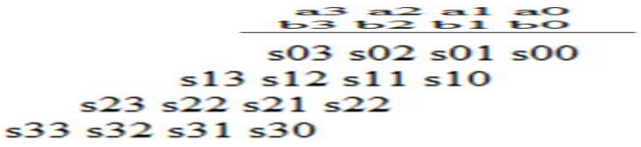

Fig. 4 Partial product of 4x4 bit multiplication

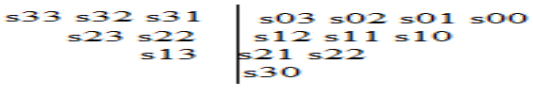

Fig. 5 Inverted pyramid of partial product

A 4x4 bit reduced complexity wallace multiplier is designed by using Cadence virtuoso in 180nm CMOS technology. The flowchart for designing a reduced complexity wallace multiplier is shown in Fig. 6. The designed 4x4 bit reduced complexity wallace multiplier is shown in Fig. 7. The design of a reduced complexity wallace multiplier is done in three steps:

i) Partial product generation
ii) Accumulation of partial product
iii) Final addition

The partial product generator is designed in the same way as the partial product generator for conventional wallace multiplier. Partial products are converted into inverted pyramid form. Now these are accumulated in different stages by using eqn. (1). Here generally full adders are used. Half adders are used only when number of stages exceeds the number of stages present in a conventional wallace multiplier. Hence it reduces number of half adders. When last stage contains only two rows, then final addition is computed by using full adders.

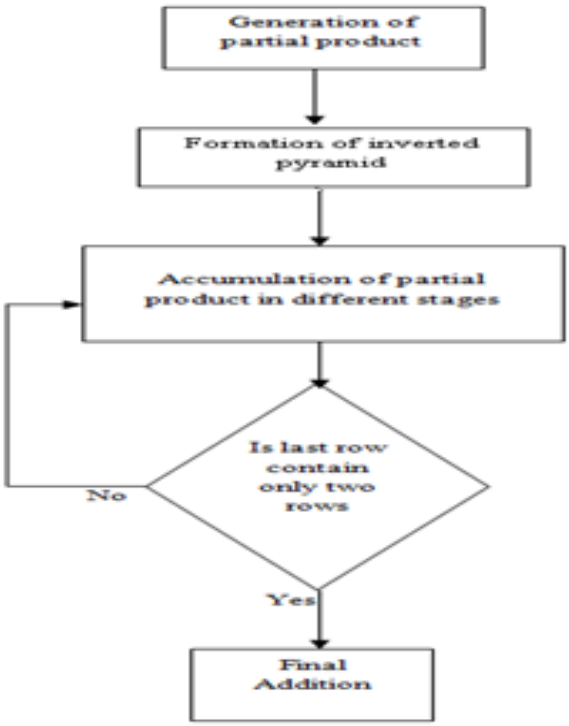

Fig. 6 Flowchart for designing a reduced complexity wallace multiplier

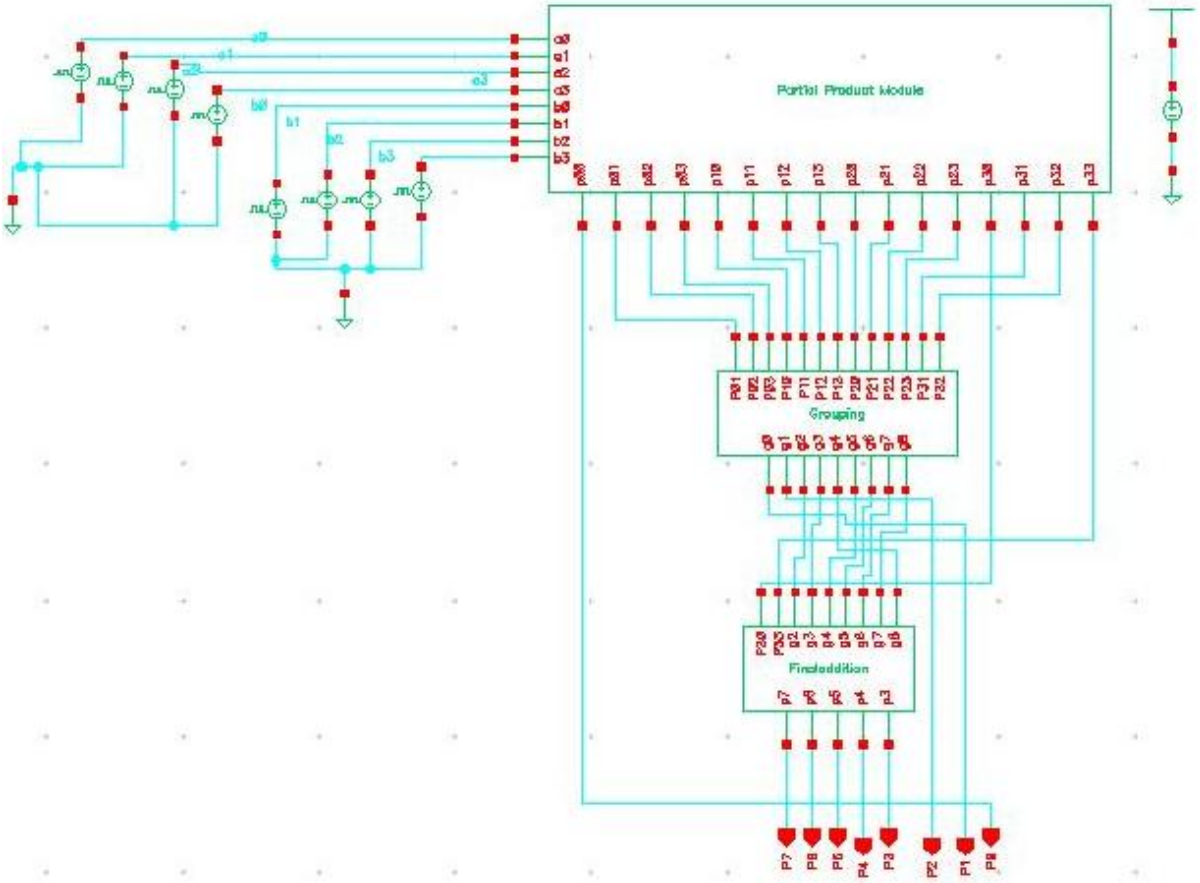

Fig. 7 A 4x4 bit reduced complexity wallace multiplier

IV. Performance Comparison Analysis

Performance characteristics analysis of a 4x4 bit conventional Wallace multiplier and a reduced complexity wallace multiplier are done by using Cadence virtuoso in 180nm CMOS technology. Power, delay, and power delay product are calculated by using calculator tool of Cadence virtuoso EDA tool. Tables 1-2 show the number of nMOS and pMOS transistors used in designing a 4x4 bit conventional Wallace multiplier and a reduced complexity Wallace multiplier. Performance characteristics of both multipliers are shown in tables 3-4. Table 5 shows the performance characteristics improvement of the designed 4x4 bit reduced Wallace complexity Wallace multiplier in comparison with the designed 4x4 bit conventional Wallace multiplier.

Table 1: Number of MOS transistors used in a 4x4 bit conventional wallace multiplier

Total number of pMOS transistors	249
Total number of nMOS transistors	249
Total number of MOS transistors	498

Table 2: Number of MOS transistors used in a 4x4 bit reduced complexity wallace multiplier

Total number of PMOS used	219
Total number of NMOS used	219
Total components used	438

Table 3: Performance characteristics of the designed 4x4 bit conventional wallace multiplier

Power	689.3µW
Delay	50µs
Power delay product	34.465 nJ

Table 4: Performance characteristics of the designed 4x4 bit reduced complexity wallace multiplier

Power	723.12µW
Delay	45.29µs
Power delay product	32.750 nJ

Table 5: Performance improvement of the designed 4x4 bit reduced complexity wallace multiplier

Performance characteristics parameters	Performance improvement
Number of MOS transistors	12.05%
Delay	9.42%
Power delay product	4.98%

From tables 1-5, it is observed that the designed 4x4 bit reduced complexity wallace multiplier is better than the designed 4x4 bit conventional wallace multiplier. The designed reduced complexity wallace multiplier shows some improvements in certain performance characteristics parameters such as number of MOS transistors used, delay, and power delay product in comparison with the designed 4x4 bit conventional wallace multiplier. However it consumes slightly more power as compared to the conventional wallace multiplier.

V. Conclusion

Performance analysis comparison of a 4x4 bit conventional wallace multiplier and a 4x4 bit reduced complexity wallace multiplier are done in terms of power, delay, power delay product and the number of MOS transistors. Less number of MOS transistors is required in designing a reduced complexity wallace multiplier as compared to a conventional wallace multiplier. Its performance characteristics in terms of delay and power delay product are better in comparison with the conventional wallace multiplier, while power dissipation is slightly increased. Hence overall performance of the reduced wallace multiplier is better than the conventional wallace multiplier.

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