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The High performance Multiplexer based Adder Circuits

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Abstract: *The need for extending low power circuits increased with the advent of use of large number of portable devices like cell phones, calculators, miniature computers etc. In all these devices, a long battery life is desired. An increase in battery life can be achieved by reducing power consumption of individual circuits. One of the methods to reduce the power consumption is by operating the devices at low current and low voltages. Operating the devices below threshold voltages is called as sub-threshold operation and the region of operation is called sub-threshold region. In this region, leakage current is used as operating current and power consumption is reduced significantly. The paper mainly focuses on the operation of various High performance Multiplexer based digital 1-bit Adder circuits[1] in sub-threshold region. The reduction in average power when compared to their super-threshold operation is analyzed. The variation of performance parameters and limitation of frequency of operation with variation in supply voltage are investigated. By varying the supply voltage below the threshold voltage, power can be reduced considerably. All the investigations in the paper are carried out using H-spice simulation tool. The circuits used are of 65nm process technology.*
Keywords: *Sub-threshold , Propagation delay , Adder, power delay product, Power dissipation.*

I. Introduction

Trends in semiconductor scaling have increased the difficulty in designing the devices that are in demand. Due to shrinking of transistor sizes, there is an increase in the growth of higher density devices which are resulted in power dissipation per chip to increase significantly. Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2-3 years once a new technology node is introduced. For example, the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip. This doubling of transistor density was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law .

The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate more slowly at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling methods are now required for many integrated circuits including microprocessors. The power dissipation problem facing the semiconductor industry has become so challenging. Without significant low power research efforts, new technologies may be needed as a long term solution. Reduction in power dissipation hence, is an important objective in the design of digital circuits. Well-known methods of low-power design (such as voltage scaling, switching activity reduction, architectural techniques of pipelining and parallelism) may not be sufficient in many applications such as portable computing gadgets, medical electronics, where ultra low-power consumption with medium frequency of operation (of the order of few MHz) is the primary requirement. Digital logic circuits computation using sub-threshold leakage current has gained a wide interest in recent years to achieve ultra low-power consumptions in portable computing devices. Both logic and memory circuits have been extensively studied with design consideration at various levels of abstraction. Significant power savings can be achieved in applications requiring low to medium frequency of operation using sub-threshold technique. The paper mainly focuses on achieving low power consumption by operating various circuits in the sub-threshold region[2]. The circuits considered are different 1-bit adder circuits which are compared[3] based on the performance metrics.

1.0 Sub-threshold 1-Bit Adder Circuits using 65nm Process Technology

1.1 Introduction:

The 1-bit adder cell is one of the most critical components of a processor that determines its throughput, as it is used in the ALU, the floating point unit and for address generation in case of cache or memory access. Therefore, it is inherent that modifications made to the full adder cell affect the system as a

whole. In the paper, various 1-bit adders are implemented in the sub-threshold region[4] and their performance is analyzed.

1.2 The High Performance Multiplexer Based Adders (HPMBA)

With the explosive growth in laptops, portable personal communication systems (PCS's), and the evolution of the shrinking technology and flexible circuits, the research efforts to find high-performance digital systems[5] has been intensified. In the paper, four multiplexed based adders which give smaller delays (and thus higher performance) than the conventional adder and Symmetric Adder even in the sub-threshold region are implemented and the results are verified. The High performance Multiplexer based adder uses the pass-gate 2:1 multiplexer as shown in the Fig1. [6].

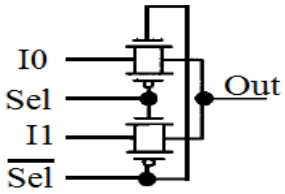

Fig 1 Pass-Gate CMOS MUX.

The usage of CMOS transmission gate in the multiplexer will improve the speed and without any degradation in the output voltage level.

1.2.1 High Performance Multiplexer Based Adder1 (HPMBA1)

The first architecture, shown in Fig.2(a), uses 6 multiplexer gates to accomplish the full adder function.

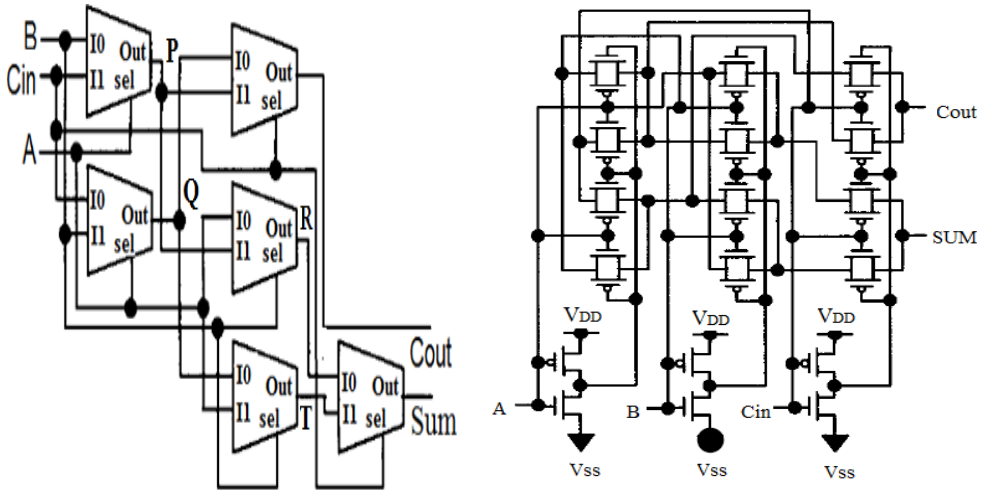

Fig 2.(a) High Performance Multiplexer Based Adder1 and Transistor level circuit diagram (HPMBA1)

The HPMBA1 has all its internal nodes connected to fresh input signals (A, B and C_{in}). Thus, the switching activity and the short circuit current of the nodes will be kept to a minimum. The SUM signal will have a critical delay equal to three times the critical delay of the used multiplexer gate, and equal to two in case of the C_{out} signal[7,8,9]. The HPMBA1 circuit implemented using the pass gate multiplexer has 30 Transistors (15 PMOS and 15 NMOS).

The HPMBA1 circuit has been simulated using H-SPICE software in the sub- threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 1

Table 1 Simulation results of HPMBA1

Parameter	Value
Carry rise time (s)	4.17E-08
Carry fall time (s)	4.19E-08
Sum rise time (s)	5.60E-08
Sum fall time (s)	2.7983E-08
Average Power (W)	2.6209E-09
Carry Delay (s)	1.8657E-08
Sum Delay (s)	2.5268E-08
PDP (J)	6.6224E-17

The Simulation Waveforms in Fig 3(a) shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 1.

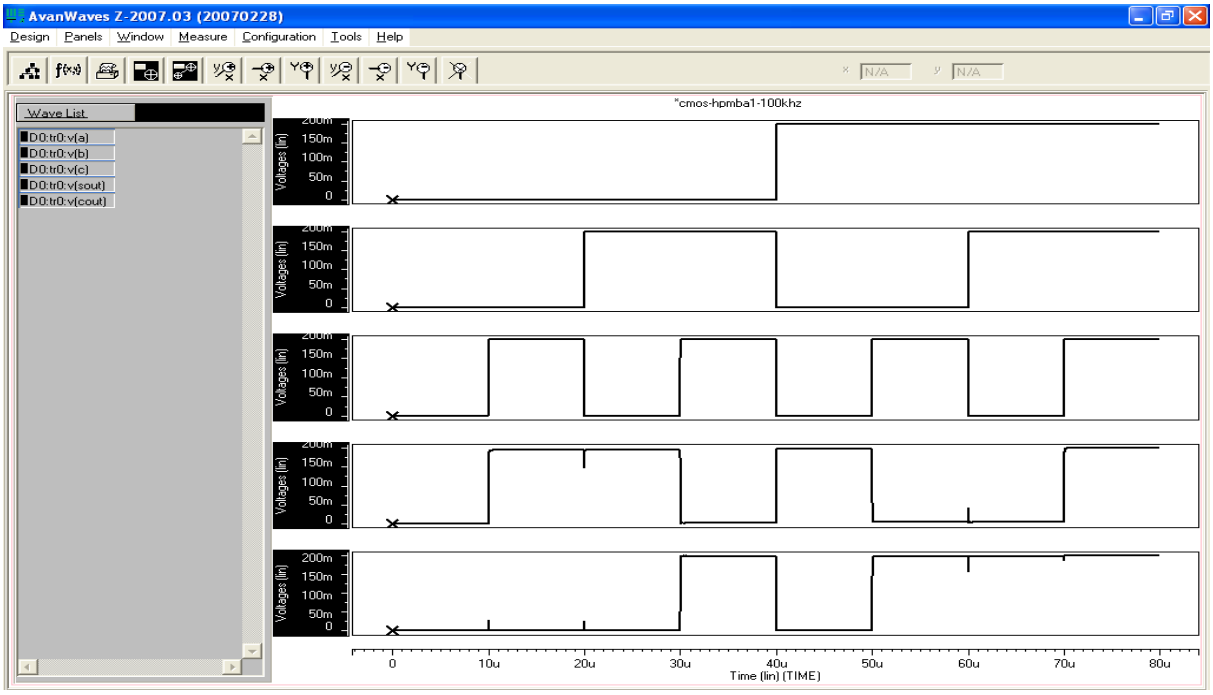

Fig 3(a) Simulation Waveforms for HPMBA1 at a frequency of 100KHz

The HPMBA1 has been simulated under various frequencies in the range 10KHz (0.01MHz) to 10MHz. From the results of the simulations, the rise time, fall time and delay are found to be constant while the average power increases with increase in frequency .The Simulation Waveforms of HPMBA1 at a frequency of 10MHz is as shown in the Fig 3(b) and it is observed that the output waveforms are distorted.

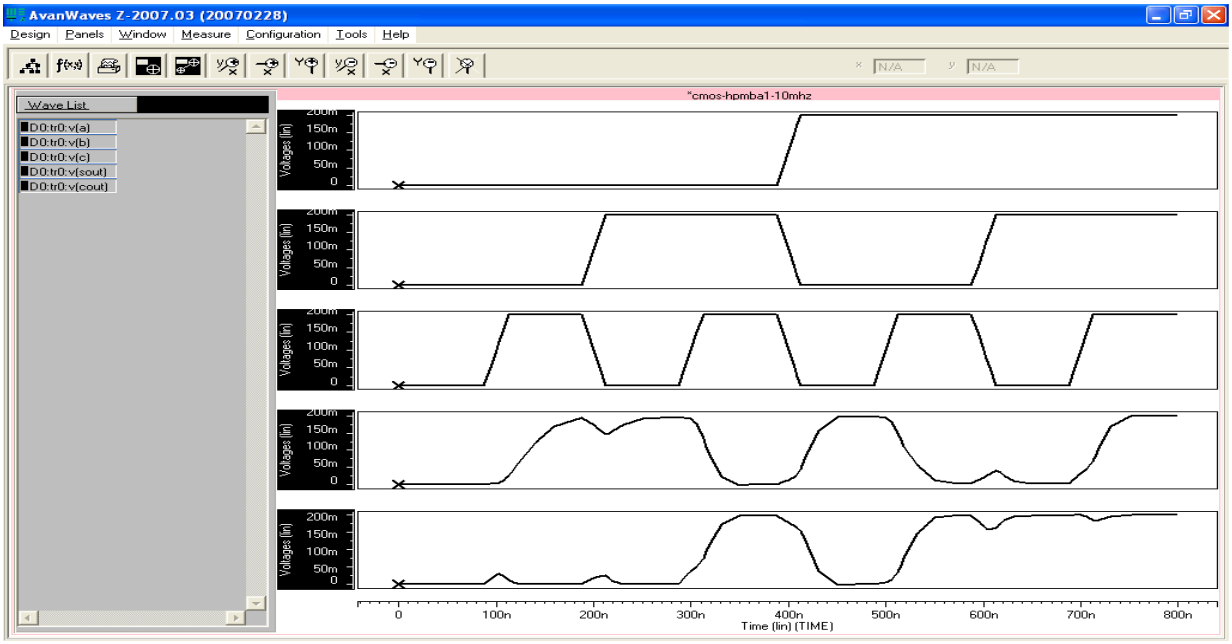

Fig 3(b) Simulation Waveforms for HPMBA1 at a frequency of 10MHz

1.2.2 High Performance Multiplexer Based Adder2 (HPMBA2)

The HPMUXA2 further improves C_{out} and SUM signal delay by employing five multiplexer gates and two inverters as shown in the Figure 3.16.

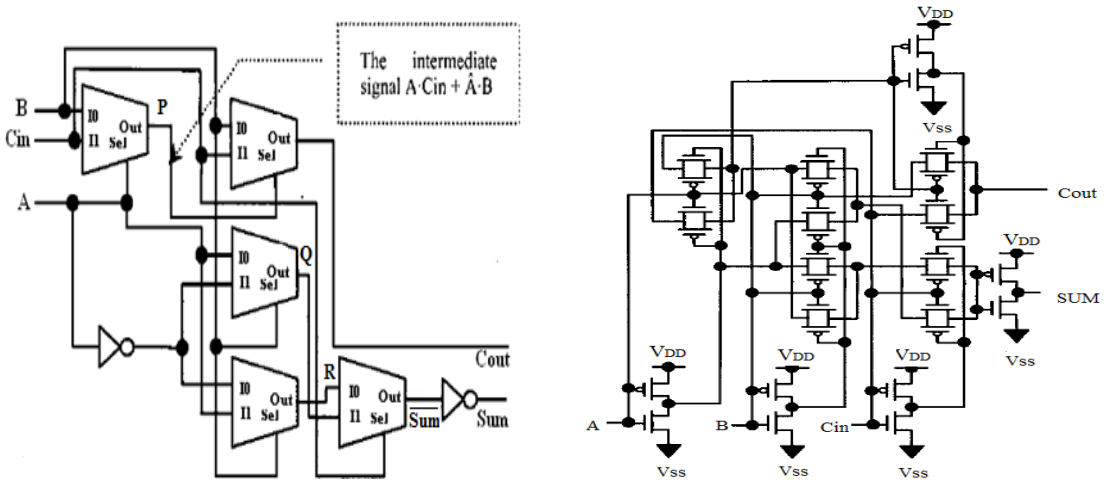

Fig 4 High Performance Multiplexer Based Adder2 (HPMBA2) andTransistor level circuit diagram of HPMBA2

The C_{out} signal of HPMBA2 is formed by using an immediately generated signal$\{(B \wedge \bar{A}) \vee (Cin \wedge A)\}$. Thus, the delay of C_{out} is equal to critical delay of one multiplexer gate plus the delay from sel port to out port. The SUM delay will be equal to two times the critical delay of the multiplexer and two times the critical delay of the inverter.

However, the power consumption of HPMBA2 will be higher than that of HPMBA1 because of the increase in the switching activity and the short circuit current of these nodes of those nodes supplied by the intermediately generated signals. Also, the presence of two inverters will add to the short circuit current of this architecture. The HPMBA2 circuit implemented using the pass gate multiplexer has 30 Transistors (15 PMOS and 15 NMOS). The HPMBA2 circuit and has been simulated using H-SPICE software in the sub-threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 2.

Table 2 Simulation results of HPMBA2

Parameter	Value
Carry rise time (s)	2.8133E-08
Carry fall time (s)	3.1139E-08
Sum rise time (s)	1.9713E-08
Sum fall time (s)	2.5879E-08
Average Power (W)	3.6255E-09
Carry Delay (s)	1.2049E-08
Sum Delay (s)	2.3096E-08
PDP (J)	8.3665E-17

The Simulation Waveforms in Figure 3.18 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 2.

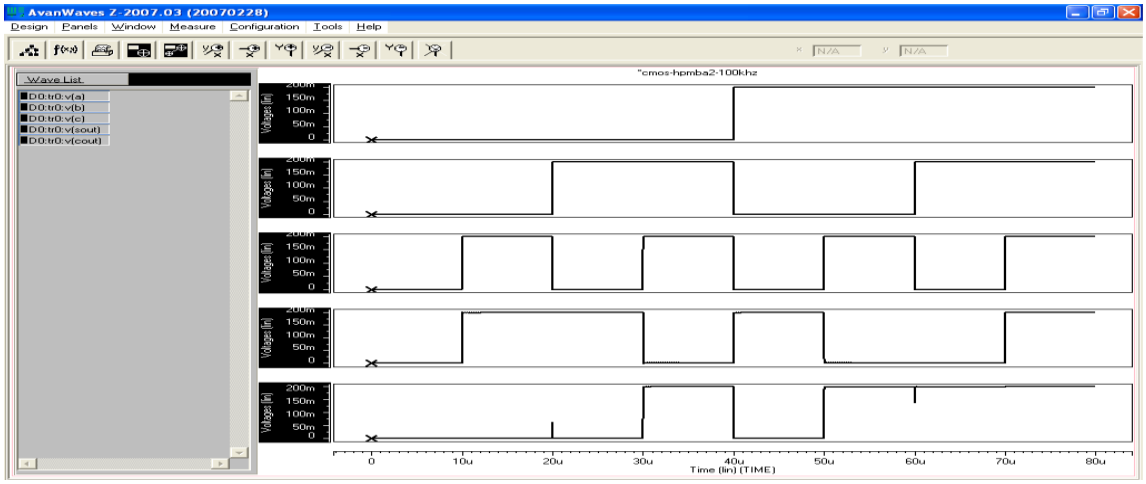

Fig 5 Simulation Waveforms for HPMBA2 at a frequency of 100KHz

The HPMBA2 has been simulated under various frequencies in the range 10KHz (0.01MHz) to 10MHz. The Simulation Waveforms of HPMBA2 at a frequency of 10MHz is as shown in the Fig6 and it is observed that the output waveforms are distorted.

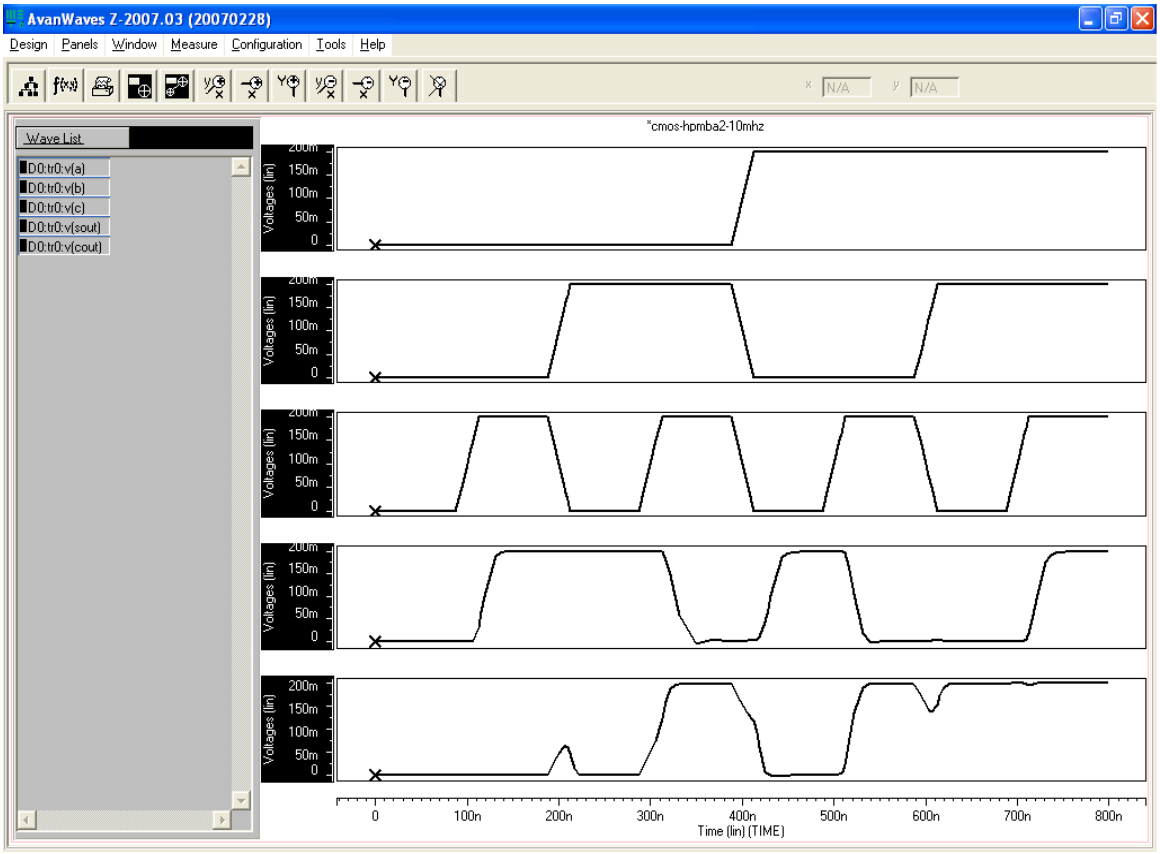

Fig 6 Simulation Waveforms for HPMBA2 at a frequency of 10MHz

1.2.3 High Performance Multiplexer Based Adder3 (HPMBA3)

This architecture is an improvement of HPMBA2. It has four multiplexer gates and two inverters as shown in Fig 7.

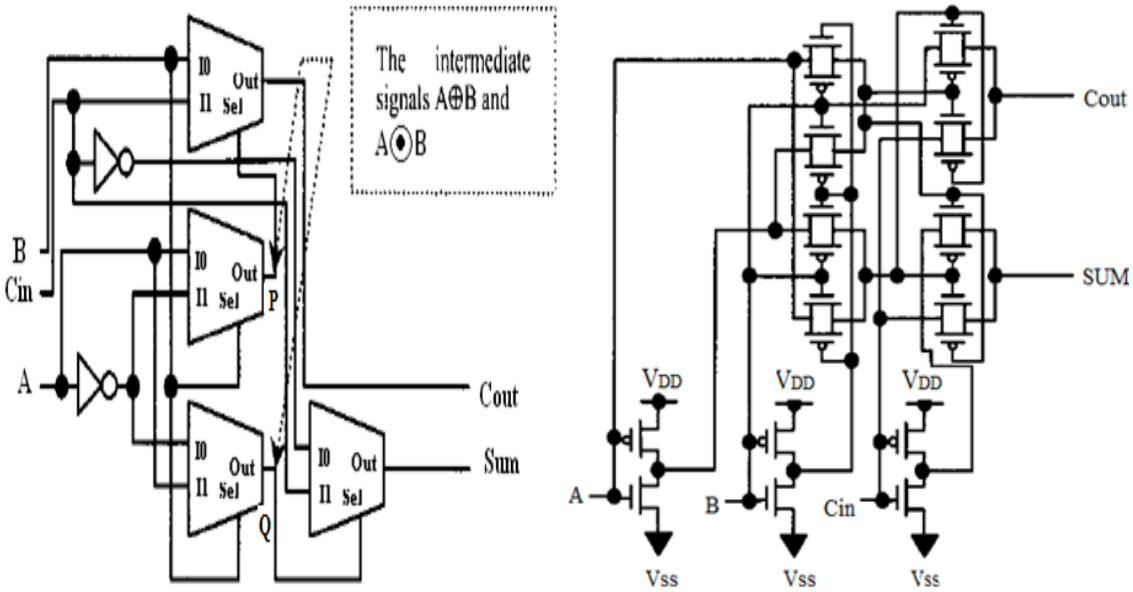

Fig 7 High Performance Multiplexer Based Adder3 (HPMBA3) and Transistor level circuit diagram of HPMBA3

The C_{out} delay will be higher as it is now equal to the sum of the critical delay of one multiplexer gate, the critical delay one inverter and the delay from Sel port to Out port. The SUM delay is less than HPMBA2 as it is equal to the critical delay of one inverter and one multiplexer plus the delay from Sel port to Out port.

The power consumption is less when compared to HPMBA2 as it uses lesser number of components. Comparing HPMBA1 with HPMBA3, the latter will have better delay characteristics, but will retain will have higher power consumption due to the usage of intermediately generated signals to produce C_{out} and SUM.

The HPMBA3 circuit implemented using the pass gate multiplexer has 22 Transistors (11 PMOS and 11 NMOS). The HPMBA3 circuit has been simulated using H-SPICE software in the sub threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 3.

Table 3 Simulation results of HPMBA3

Parameter	Value
Carry rise time (s)	2.7567E-08
Carry fall time (s)	3.0141E-08
Sum rise time (s)	2.9476E-08
Sum fall time (s)	3.0918E-08
Average Power (W)	2.8168E-09
Carry Delay (s)	1.2815E-08
Sum Delay (s)	1.4648E-08
PDP (J)	4.1261E-17

The Simulation Waveforms in Figure 3.23 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 3.

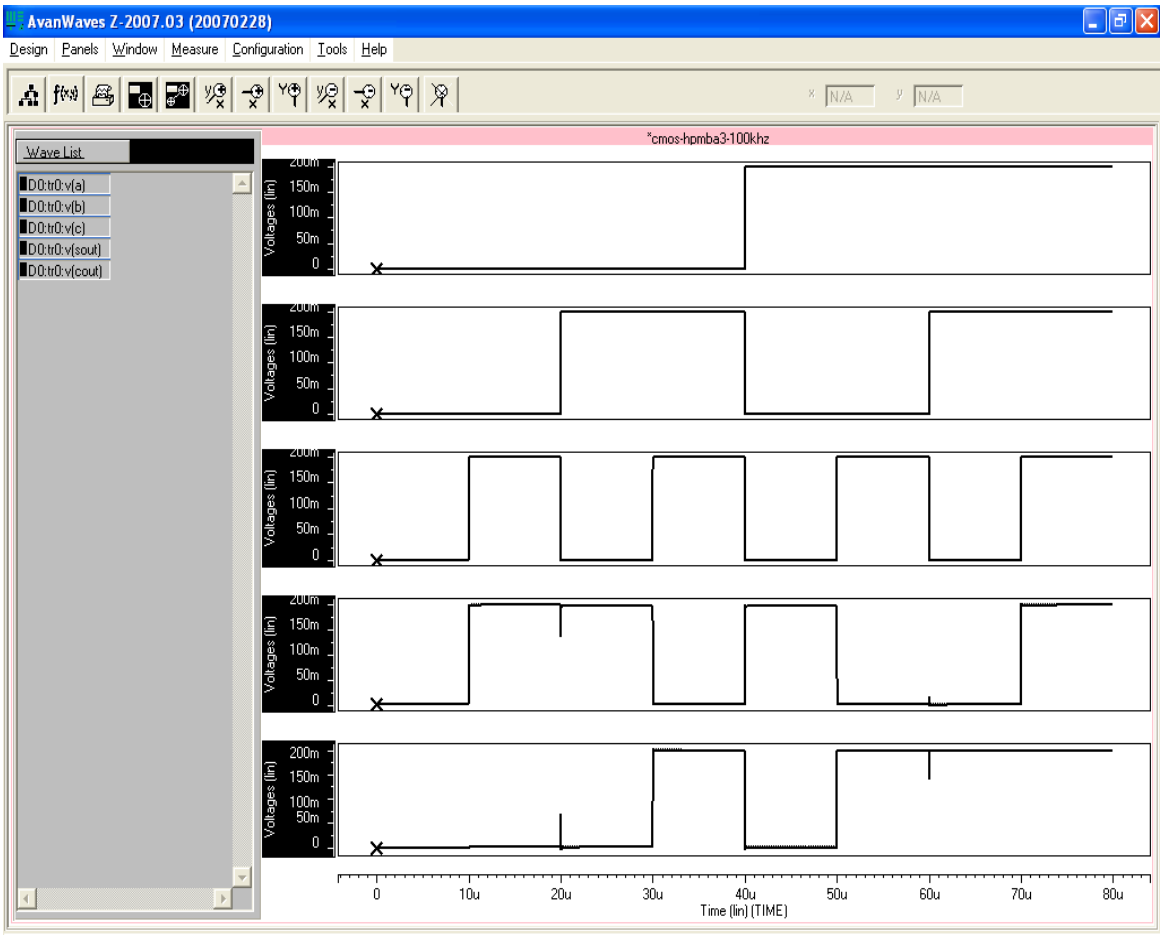

Fig 8 Simulation Waveforms for HPMBA3 at a frequency of 100KHz

The HPMBA3 has been simulated under various frequencies in the range 10KHz (0.01MHz) to 10MHz. The Simulation Waveforms of HPMBA3 at a frequency of 10MHz is as shown in the Fig 9 and it is observed that the output waveforms are distorted.

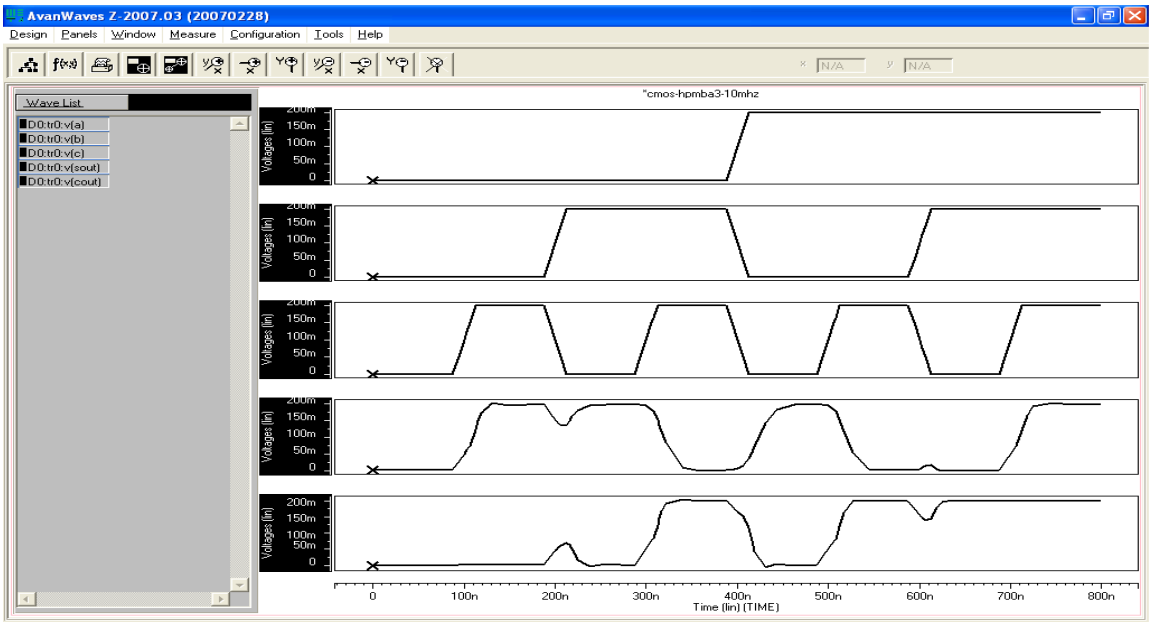

Fig 9 Simulation Waveforms for HPMBA3 at a frequency of 10MHz

1.2.4 High Performance Multiplexer Based Adder4 (HPMBA4)

The HPMBA4 is another modification of HPMBA2. One inverter in the HPMBA2 is replaced with two inverter-like structures to reduce the short circuit current power consumption. The first inverter-like structure is basically a CMOS inverter with its NMOS source connected to signal A instead of V_{DD} while the second one has its PMOS connected to A. Therefore the HPMBA4 uses five multiplexer gates, one inverter and two inverter-like structures as shown in the Fig 10.

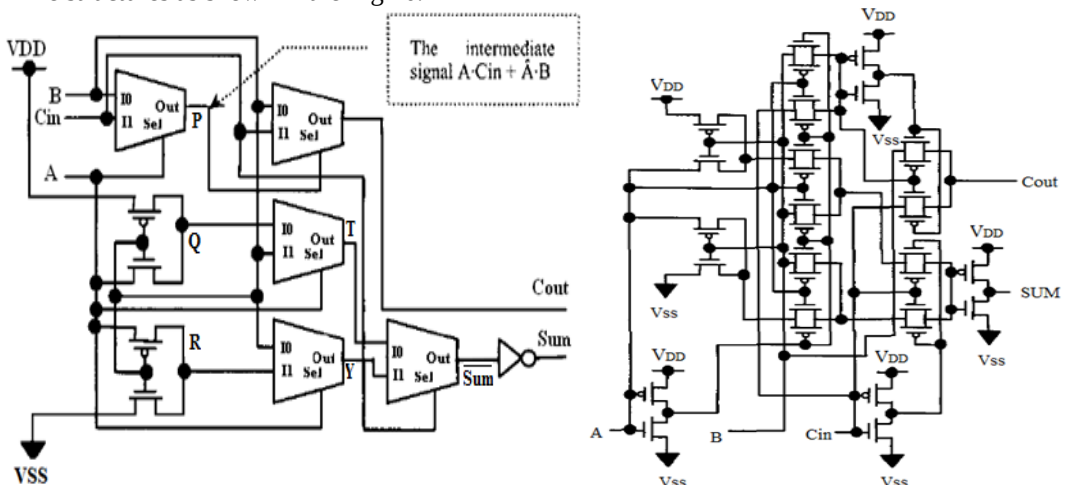

Fig 10 High Performance Multiplexer Based Adder4 andTransistor level circuit diagram of HPMBA4

The C_{out} delay of HPMBA4 is similar to that of HPMBA2 but the sum delay is found to be lesser. The HPMBA4 circuit implemented using the pass gate multiplexer (Fig 10) has 32 Transistors (16 PMOS and 16 NMOS). The HPMBA4 circuit and has been simulated using H-SPICE software in the sub threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 4.

Table 4 Simulation results of HPMBA4

Parameter	Value
Carry rise time (s)	2.8130E-08
Carry fall time (s)	3.2742E-08
Sum rise time (s)	1.9634E-08
Sum fall time (s)	1.7544E-08
Average Power (W)	3.3622E-09
Carry Delay (s)	1.2454E-08
Sum Delay (s)	2.1312E-08
PDP (J)	7.1655E-17

The Simulation Waveforms in Fig 11 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 4.

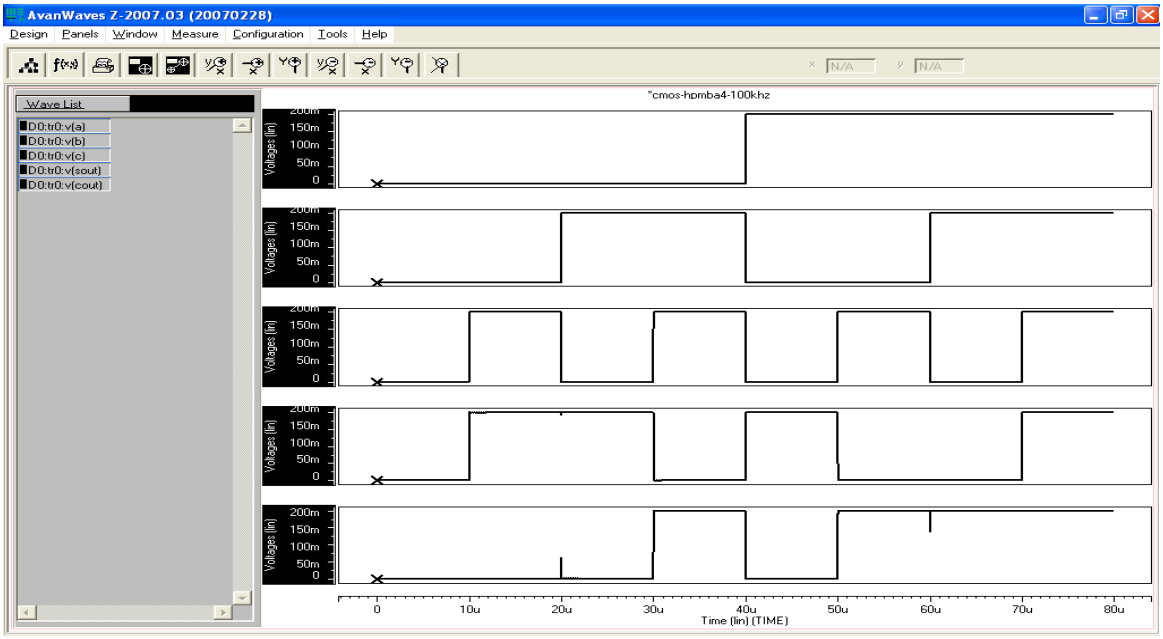

Fig 11 Simulation Waveforms for HPMBA4 at a frequency of 100KHz

The HPMBA4 has been simulated under various frequencies the range 10KHz (0.01MHz) to 10MHz.

The Simulation Waveforms of HPMBA4 at a frequency of 10MHz is as shown in the Fig 12 and it is observed that the output waveforms are distorted.

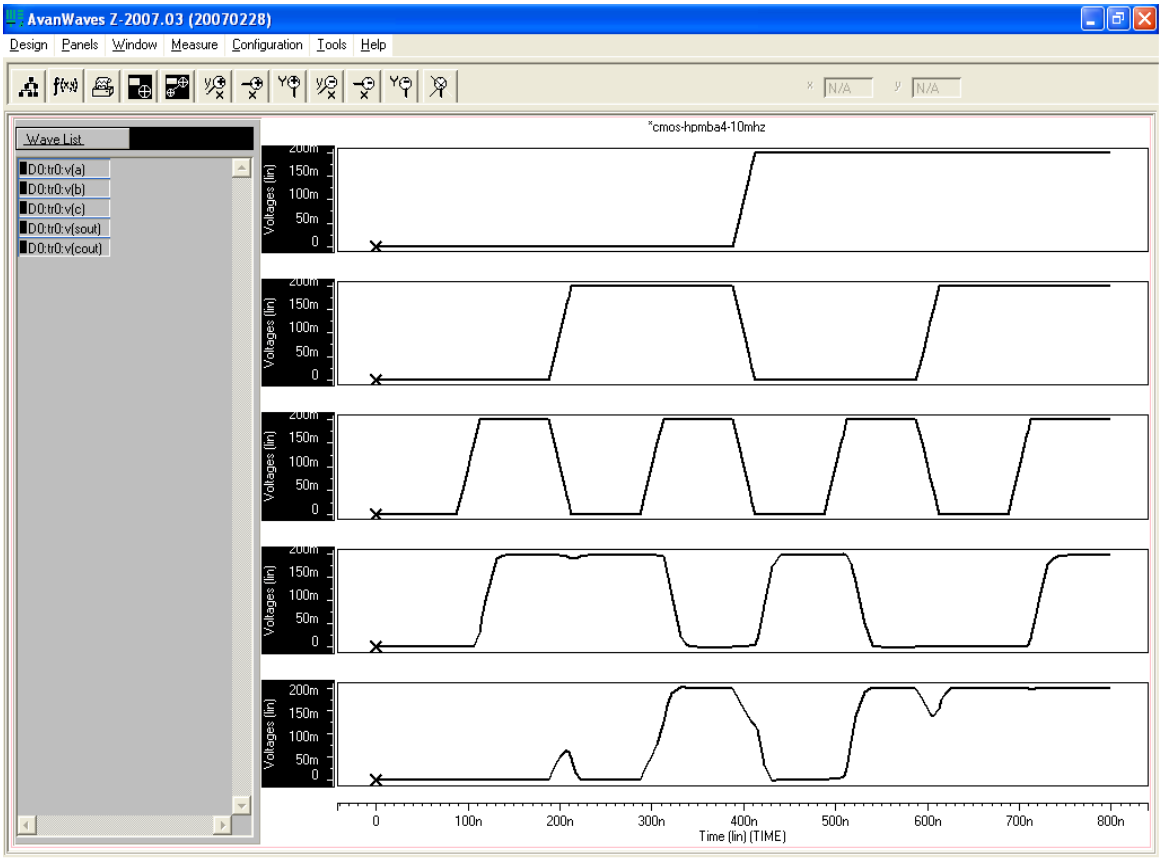

Fig 12 Simulation Waveforms for HPMBA4 at a frequency of 10MHz

The high performance multiplexer based adders can be used to improve performance in sub threshold region. However, we can further reduce the power of 1-bit adder cell in sub threshold region by using low power multiplexer based adders.

These employ less number of transistors and hence achieve lower power dissipation. The lowest number of transistors with which a 1-bit adder can be constructed is 10.

II. Discussion Of Results

In the paper, 4 1-bit High Performance Multiplexer Based Adders are implemented in sub-threshold region. The HPMBAs have smaller delays when compared to the conventional 1-bit adder. The HPMBA1, HPMBA2, HPMBA3 and HPMBA4 have 10%, 17.4%, 47.66% and 23.79% speed increment (decrement in delay) over conventional adders. The silicon chip area occupied by the any circuit will be proportional to the number of transistors required for implementing it. The HPMBAs occupy less area when compared to the conventional 1-bit adder. The decrements in area, taking the conventional 1-bit adder as reference for HPMBA1, HPMBA2, HPMBA3, HPMBA4 are 34.78%, 34.78%, 52.17%, and 30.43%, respectively.

2.1 Comparison of all 1-bit adders

All the 1-bit adder circuits have been simulated at 100KHz (pulse duration is 10μs) frequency under both sub threshold (V_{DD}=0.2V) and super threshold region (V_{DD}=0.8V) and the results have been tabulated in the Table5.

Table 5 Simulation results of all 1-bit adders

Parameter/Adder	Average power (W)		Propagation Delay (s)		Power Delay Product (J)	
	V_{DD}=0.2V	V_{DD}=0.8V	V_{DD}=0.2V	V_{DD}=0.8V	V_{DD}=0.2V	V_{DD}=0.8V
HP MBA1	2.6209E-09	2.7824E-08	2.5268E-08	1.4864E-09	6.6224E-17	4.1359E-17
HP MBA2	3.6255E-09	3.9876E-08	2.3096E-08	1.0072E-09	8.3665E-17	4.0165E-17
HP MBA3	2.8168E-09	2.9283E-08	1.4648E-08	8.5658E-10	4.1261E-17	2.5084E-17
HP MBA4	3.3622E-09	3.6885E-08	2.1312E-08	8.1058E-10	7.1655E-17	2.9898E-17

From Table 5, it can be observed that the adders when operated in sub-threshold region have lower power consumption (nearly 0.1 times of that in super- threshold region) and higher propagation delay (greater than ten times of that in super-threshold region).

III. Conclusions

From the various 1-bit adders that are implemented using 65nm technology, it is observed that HPMBA2 has the highest average power ,the HPMBA3 has the least propagation delay and it does not produce any degradation in the output voltage levels.

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