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Simulation of Propagation Delay of Multi and Single Conductor MLGNR in Nano Scale Region

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Abstract: *The paper deals with the analysis of propagation delay of multi-layer graphene nano-ribbon (MLGNR) using single and multi conductor equivalent models at 16 nm for driver-interconnect-load (DIL) system. The length of MLGNR varies from 100 µm to 1000 µm has been used for GNR at different layers 3, 10 and 20. Three threshold voltages 0.5V (super threshold region), 0.3V (near threshold region), and 0.2V (sub threshold region) have been used for different number of devices connected in parallel.*

Keywords: *CMOS, Driver-Interconnect-Load (DIL), FinFET, Multi conductor equivalent model, Single conductor equivalent model.*

I. Introduction

In recent years as the demand of better VLSI interconnects increases graphene nano-ribbon is playing an important role in the area of interconnection because of its outstanding properties. Graphene nano-ribbon is a flat two dimensional sheet. Like carbon nanotube graphene can be conducting and semi conducting [1][2]. There are two variants of graphene sheet namely arm-chair GNR and zig-zag GNR [3].

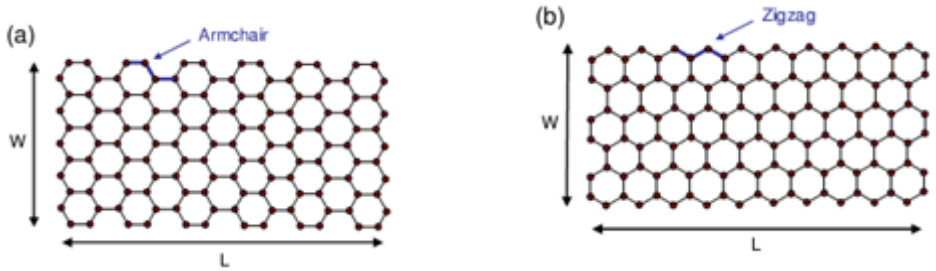

Fig.1 (a) armchair GNR and (b) zigzag GNR [4]

In this paper the effect of equivalent circuits of MLGNR along with DIL system have been studied in terms of propagation delay using TSPICE. The multi conductor equivalent circuit [5] carries mutual inductances and mutual capacitances along with quantum resistance, quantum capacitance, electrostatic capacitance, kinetic inductance and electrostatic inductance. For this work contact resistance of 3.2kΩ has been considered. The type of MLGNR which has been used in this work is neutral MLGNR means with no doping and with E_F = 0.1eV. The inter layer distance of 0.34 nm has been considered for the MLGNR. Mean free path equal to 419 nm has been taken in this work [6].

II. Interconnect Model

Two equivalent models of MLGNR shown in Fig. 3 have been used along with DIL system for the simulation.

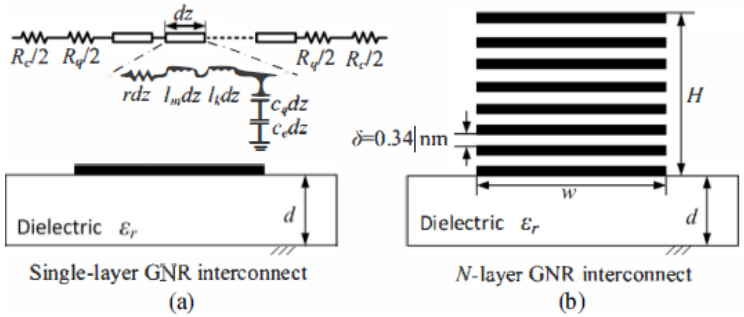

Fig. 2 Geometries of (a) single- and (b) N-Iayer GNR interconnects, together [5]

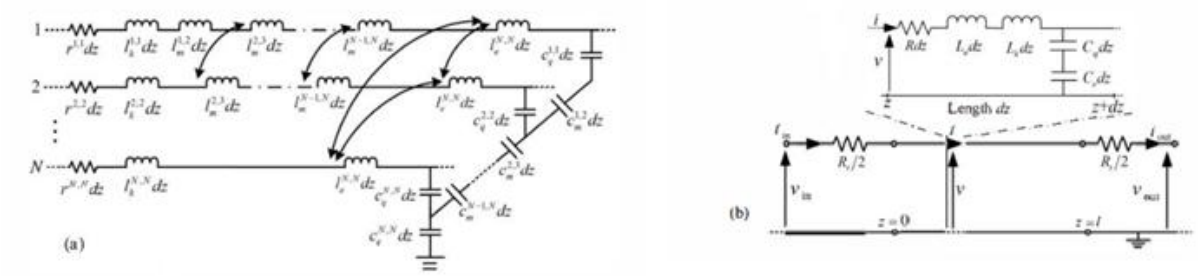

Fig. 3 (a) Multi-conductor circuit model (b) ESC model of the MLGNR interconnect [5]

The components of multi conductor circuit expressed by the authors in [7][8][3] have been used in this work to calculate the values for quantum capacitance, electrostatic capacitance, kinetic inductance, electrostatic inductance and quantum resistance.

$R_Q = (h/2q^2)/N_{ch}N_{layer} = 12.94\ K\Omega/\ N_{ch}N_{layer}$ (1)

$C_Q = N_{ch}N_{layer}\ 4q^2/hv_f = N_{ch}N_{layer} * 193.18\ aF/\mu m$ (2)

$C_E = \varepsilon_0 * w/d\ aF/\mu m$ (3)

$L_K = (h/4q^2v_f)/\ N_{ch}N_{layer} = 8.0884/\ N_{ch}N_{layer}\ nH/\mu m$ (4)

$L_E = \mu_0 * (d/w)\ nH/\mu m$ (5)

where, $N_{ch} = N_{ch,electron} + N_{ch,hole}$

$N_{ch} = \Sigma\ [1 + \exp((E_{n,electron} - E_F)/k_BT)]^{-1} + \Sigma\ [1 + \exp((E_F - E_{n,hole})/k_BT)]^{-1}$ (6)

N_{ch}= number of conducting channels in one layer,

N_{layer}= number of GNR layers,

h = Plank's constant $=6.626*10^{-34}$ J.s, and q = electronic charge $=1.6*10^{-19}$ C, v_f= Fermi velocity = $8*10^5$ m/s for GNR, $E_{n,electron}$ ($E_{n,hole}$) = minimum (maximum) energy of the nth conduction (valence) sub-band.

The expressions for mutual inductance and mutual capacitance is given by Areshkin in [9] have been used which are given as,

$l_{m,layer}^{(j-1,j)} = \mu_0 * (\partial / w)\ nH/\mu m$ (7)

$C_{m,layer}^{(j-1,\ j)} = \varepsilon_0 * (w/\partial)\ aF/\mu m$ (8)

Where ∂ is distance between two adjacent layers, μ_0 and ε_0 are the magnetic permeability and electrostatic permittivity of free space respectively.

Also the components of single conductor circuit which has been given by Cui in [10] used in this work which are given as,

$R_{ESC} = 12.94\ K\Omega/\ \lambda\ N_{ch}N_{layer}$

Where λ is mean free path.

$L_{ESC} = L_K + L_E$

$C_{ESC} = (C_Q + C_E)^{-1}$

Where, $C_E = C_e^{(N,N)}$

$C_Q = C_p^{(N)}$

and $C_p = C_Q^{(j,j)} + C_S^{(j-1)}$, for $j \in [2,N]$

$C_S^{(j-1)} = (1/\ C_Q^{(j-1)} + 1/\ C_m^{(j-1,\ j)})^{-1}$, for $j \in [2,N]$

$C_p^{(1)} = C_Q^{(1,1)}$

Similarly, $L_E = L_e^{(N,N)}$

$L_K = L_p^{(N)}$

$L_p^{(j)} = (1/\ L_K^{(j.j)} + 1/\ L_e^{(j-1)})^{-1}$, for $j \in [2,N]$

$L_e^{(j-1)} = L_p^{(j-1)} + l_{m,}^{(j-1,j)}$, for $j \in [2,N]$

$L_p^{(1)} = L_K^{(1,1)}$

III. Simulation And Results

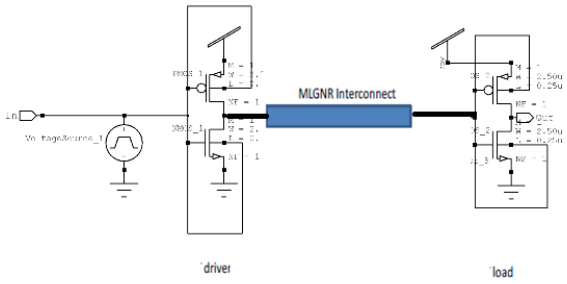

Fig. 4 Driver- interconnect-load system (DIL) using SG FinFET driver-load stage.

The simulation set up comprises of MLGNR interconnect with driver and load with different number of layers like 3, 10, and 20. The driver and load circuits which have been used for analysis are CMOS, short-gate (SG) FinFET, low-power (LP) FinFET, and independent-gate (IG) FinFET at 16 nm. By using these four set ups delay performance is calculated for multi conductor and single conductor equivalent circuits of MLGNR. The Fig. 4 shows a DIL system with SG FinFET driver-load stage, other DIL systems have been obtained by simply connecting the CMOS and other two forms of FinFETs in the above driver-load stages.

TSPICE version 14.0 has been used for simulation work. The different number of devices which are connected in parallel have been shown by using the symbol M. Results from Fig. 5 to Fig.8 shows delay variation at Vin = 0.5V for four test circuits for different values of M. Results from Fig 9 to Fig.15 show the same effect as above but for sub threshold region and near sub threshold region.

Fig. 16 shows the comparative effect of single and multi conductor model of MLGNR with respect to delay at 100 um interconnect length and for GNR layers = 3, 10 and 20 which clearly shows the difference in the values of multi and single conductor equivalent circuit.

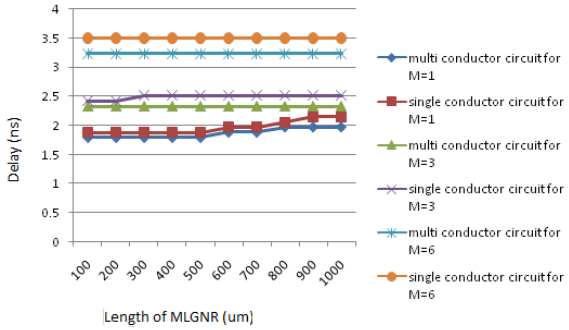

Fig. 5 Effect of length on delay for CMOS DIL in super threshold region

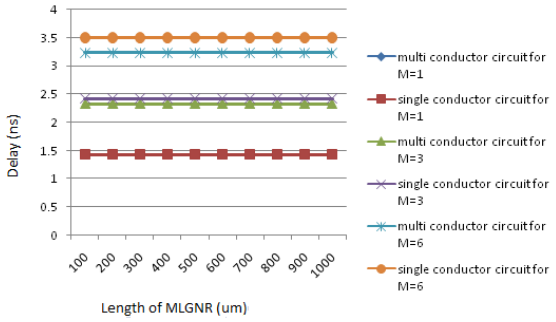

Fig. 6 Effect of length on delay for SG FinFET DIL in super threshold region

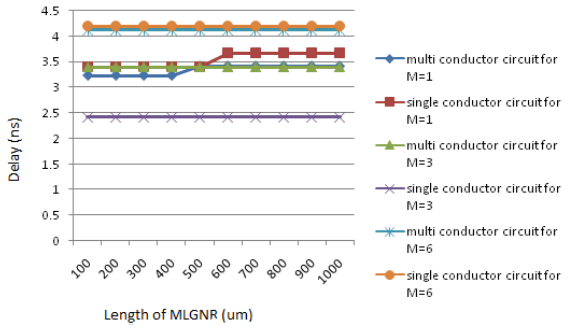

Fig. 7 Effect of length on delay for LP FinFET DIL in super threshold region

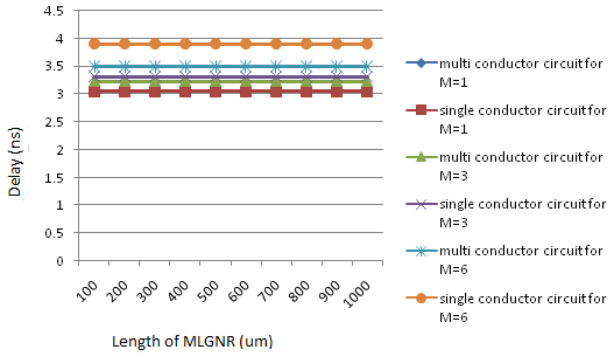

Fig. 8 Effect of length on delay for IG FinFET DIL in super threshold region

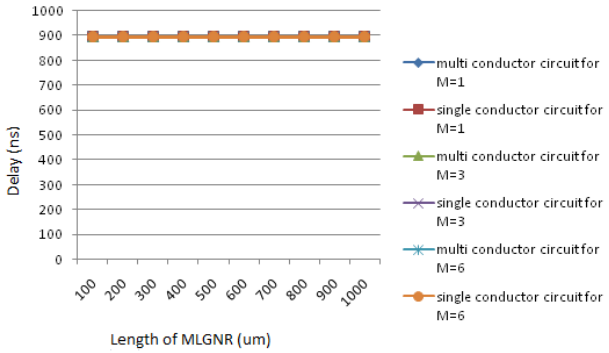

Fig. 9 Effect of length on delay for CMOS and SG FinFET DIL in near threshold region

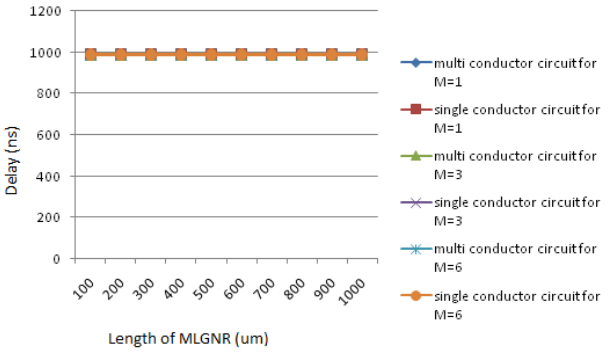

Fig. 10 Effect of length on delay for IG FinFET DIL in near threshold region

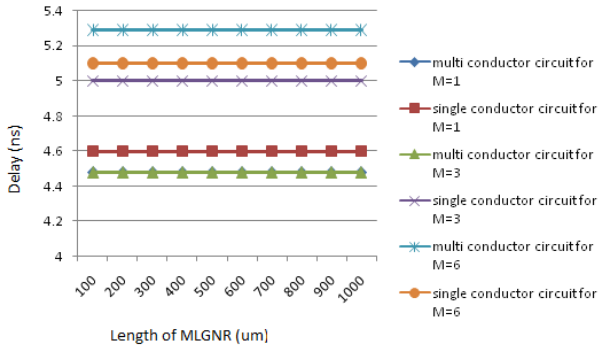

Fig. 11 Effect of length on delay for LP FinFET DIL in near threshold region

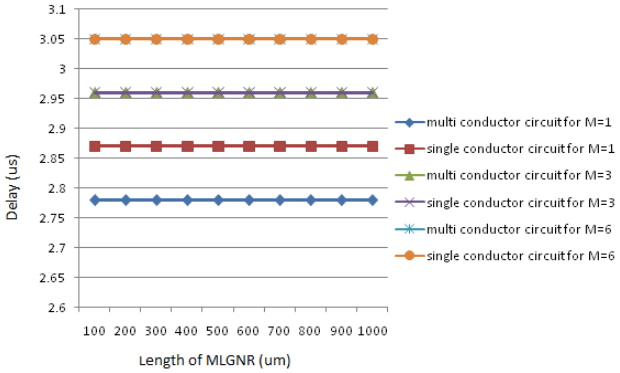

Fig. 12 Effect of length on delay for CMOS DIL in sub threshold region

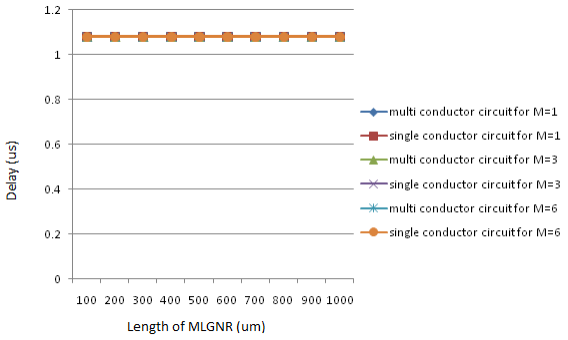

Fig. 13 Effect of length on delay for SG FinFET DIL in sub threshold region

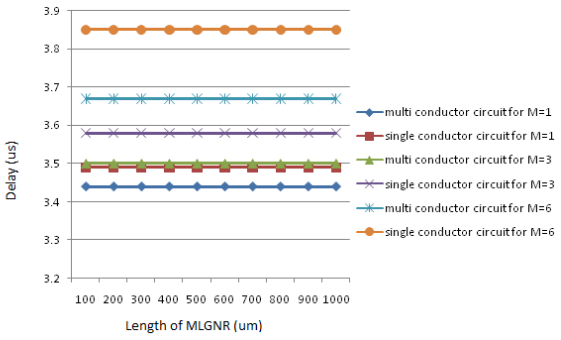

Fig. 14 Effect of length on delay for IG FinFET DIL in sub threshold region

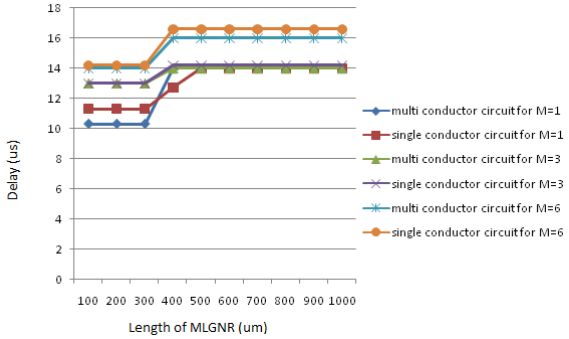

Fig. 15 Effect of length on delay for LP FinFET DIL in sub threshold region

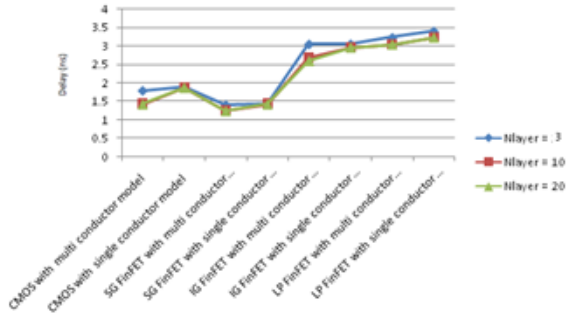

Fig. 16 Comparison of multi and single conductor model for different GNR layers

IV. Conclusion

The paper has shown the comparative analysis of propagation delay of multi and single conductor equivalent circuits of MLGNR along with DIL system. From the results which have been simulated in the paper it is clear that the multi conductor model gives better values than that of single conductor and this effect is significant for all four test circuits in super threshold, but in near threshold region the effect is clear only for LP FinFET DIL system and also the comparative effect is less for CMOS and SG FinFET DIL systems in sub threshold region.

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