# Impact of Quaternary Logic on Performance of Look-Up Tables

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***Abstract:*** *The explosive growth of the semiconductor industry over the past decade has been driven by the rapid scaling of complementary metal-oxide-semiconductor (CMOS) technology. Interconnects still is the major area which continues to gain attention of designers as they play crucial role in Power, Delay and area of any chip. With use of Multiple-valued logic it is possible to reduce the number of bits used to represent information in the circuit, so can be used to reduce the impact of interconnections. In addition to the reduction in number of bits, multiple-valued logic can show increase in functional complexity, implementing circuits that can perform comparable to the binary circuits. Proposed here a quaternary lookup table (LUT) structure, and compared with binary LUTs for performance optimization. The circuit is designed with standard CMOS processes, employing single voltage supply designed using voltage-mode structures. Presented in this work is quaternary lookup table (QLUT) able to work at 1MHz consuming 36.48 µW. The experimental results demonstrate the correct quaternary operation estimate the power efficiency of the proposed design.*

***Keywords:*** *Quaternary, Look-up Table, Power dissipation, Noise margin, Propagation Delay*.

## I.    Introduction

### 1.1  Quaternary logic

Multi-valued systems are usually proposed to provide advantages by decreasing the number of data interconnect lines and processing components. Such logic circuits can represent numbers with fewer bits than binary, e.g. the decimal number 255 is represented as 11111111 in binary and 3333 in quaternary. Multiple-valued logic can provide improved circuit interconnections, reduced chip area and increased bus efficiency, since more logic levels are used per line" as compared to conventional binary logic.

An important aspect of multi-valued logic systems is of choosing the radix value and the choice of radix is available in actual or conceptual domains. Actual and conceptual domains may be different. The choice mainly depends on the ease of manipulations of variables in conceptual domain and manipulations of voltage, current, charge etc. in actual circuits.

Quaternary logic is quite feasible since the implementations can be designed using available circuitry, and no additional special components are required. Hence quaternary radix is selected to realize the logic circuits. In Quaternary logic level 0, level 1, level 2, level 3 can be represented by Gnd (ground), Vdd/3, 2Vdd/3, and Vdd respectively. In addition to the reduction in interconnections, Quaternary logic also offers a possibility of increasing the functional complexity per unit silicon area, producing circuits that have performance comparable to the equivalent binary circuits.

### 1.2 Look up Tables (LUT)

General Look-Up Tables (LUTs) are fast memories, which implement a logic function according to their selection mode. LUT contains Memory Cells to implement small logic functions. Look up Tables are the kind of logic that are used in SRAM based FPGAs. Each LUT is a bunch of single bit memory cells storing individual bit values in each of the cells. Configuration values are initially stored in the look-up table structure, and once inputs are applied to it, the logic value in the SRAM associated is assigned to the output.

The capacity of a LUT |C| is given by

$$|C| = n \times b^k \qquad (1)$$

Where n is the number of outputs, k is the number of inputs and b is the number of logic values. 4-input binary look-up table with one output is able to store $1 \times 2^4 = 16$ Boolean values. The total number of functions |F | that can be implemented in a BLUT with k input variables is given as

$$|F| = b^{|C|} \qquad (2)$$

Use of quaternary logic in design of Look up table and calculation for capacity and possible function

implemented and its comparison with binary look-up table is shown in table below. It shows LUT capacity to hold Boolean values and possible function can be implemented using them.

**Table I Comparison of Binary and Quaternary LUTs**

| Parameter | BLUT ( 2 variable , 1 output) | QLUT ( 2 variable , 1 output) |
|---|---|---|
| Capacity :<br>$\|c\| = n \times b^k$ | $\|C\| = 1 \times 2^2 = 4$<br><br>2i/p BLUT: holds 4logic value | $\|C\| = 1 \times 4^2 = 16$<br><br>2i/p QLUT : holds16 logic value |
| Functions:<br>$\|F\| = b^{\|c\|}$ | $\|F\| = 2^{\|4\|} = 16$ | $\|F\| = 4^{\|16\|} = 4294967296$ |

Considering any four variable function the below table shows details comparison of design using Quaternary and binary LUT.

**Table II BLUT & QLUT comparison for implementation of 4 variable FUNCTIONS**

| Parameter | 4 variable function i.e. 4 i/p BLUT | 2 variable function i.e. 2 i/p QLUT |
|---|---|---|
| Capacity | Stores16 Logic values | Stores 16 logic values |
| Select lines i.e. Inputs | 4 | 2 |
| Transistor count with Transmission Gates | 34 NMOS, 34 PMOS | 42 NMOS,42 PMOS |
| Total nodes formed | 15 | 5 |
| Multiplexer Stages | 4 | 2 |

## II.    Circuit Implementation

### 2.1 Quaternary Inverter

Fig.1. Shows Quaternary SRAM and Inverter consists of five enhancement mode n MOS and p MOS each. Threshold voltages of the transistors T1, T2, T3 to which input is applied are 0.5, 1.5, and 2.5 and act as switches. There is a correspondence between magnitude of logic level and of voltage value i.e., with voltages 1.5 and 2.5. Transistors T4 and T5 forms voltage divider network. When input is provided as four levels output is calculated as per the following equation.

$$\text{Output} = \text{radix} - \text{input} - 1 \qquad\qquad (3)$$

Radix selected here is 4 for quaternary logic and four inputs are 0v for logic '1' , 1v for logic'2', 2v for logic '2' , 3v for logic'3'. For stable state are obtained after simulation. Complexity of circuit is reduced by employing three values of enhancement mode threshold voltage this uses a priority rule in establishing the output voltage i.e. the priority is given to lowest level at all times when many transistors are in the ON state.
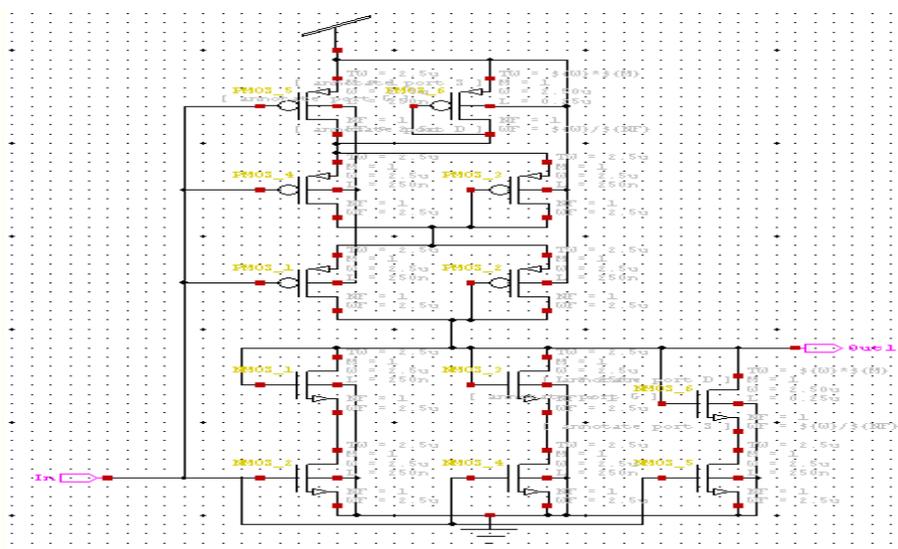


**Fig. 1 Quaternary Inverter**

## 2.2 Quaternary SRAM

Here for quaternary SRAM cell quaternary inverters are used instead of binary inverters. The data being held in the memory cell will be interpreted as a logic 0, logic 1 or logic 2 or logic 3. Fig.2. shows the structure of the MOS static RAM cell for quaternary logic, consisting of 2 cross-coupled quaternary inverters and 2 access transistors.
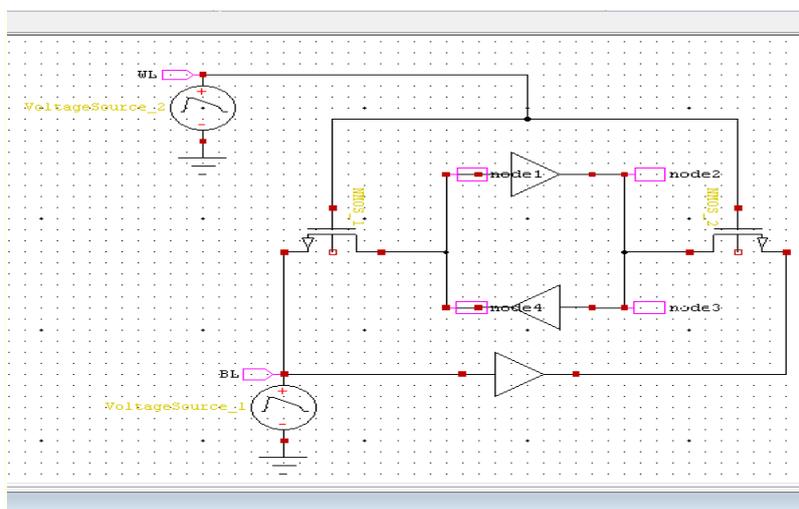


**Fig.2 Quaternary SRAM**

## 2.3 Quaternary transmission gate.

Designing low-power devices is done through techniques. The techniques used in this design, to reduce the power consumption are [11] [5] [4]:

a.  Use of static design over dynamic.
b.  Circuit complexity has been reduced by using three values of enhancement mode threshold voltage and by utilizing a priority rule in establishing the output voltage i.e. the priority is given to lowest level at all times when several transistors are in the ON state. This principle of operation leads to the marked decrease in the in the transistor number and exact transient response.
c.  Minimizing capacitances, and total area.

Design style is static through the use of static CMOS and static TG gates. TG can have are able to lower down power supply VDD from the nominal value because PMOS and NMOS devices are both used, hence there is full-logic swing [9]. Minimization of area is possible with TG gates because they can be mostly made to be minimum sized.

Literals used in the representation are to provide controlling action. Respective inputs must be selected with appropriate control input. Complete gate level schematic of T-gate is as shown below in fig.3. Simple transmission gate is required to transmit the external input to the output, depending upon the content control input. Simple inverter is required to get desired bias condition for PMOS of Transmission gate as given below
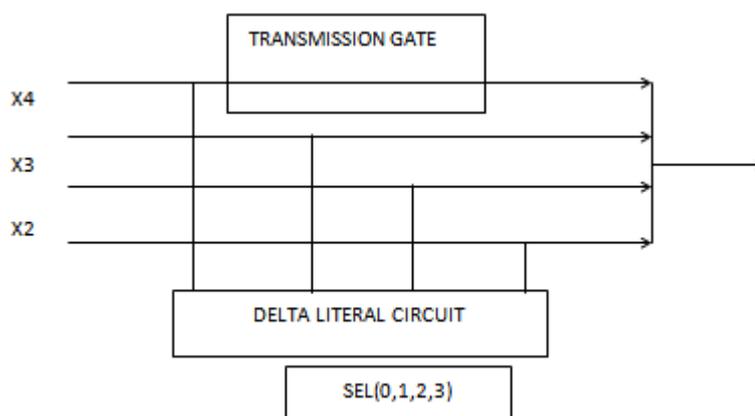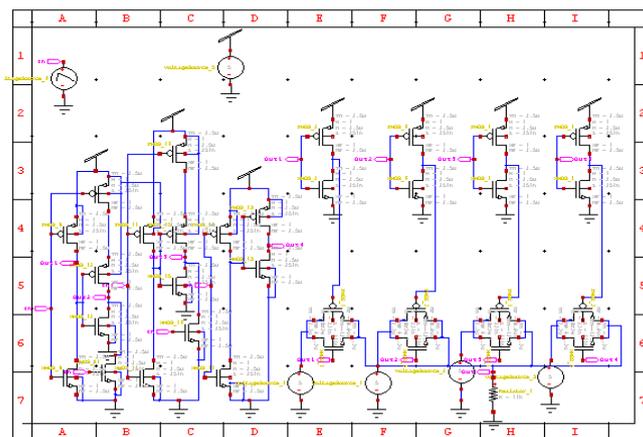


**Fig.3 Basic Delta Literal Circuit used in Design**

**Fig.4 Schematic for Quaternary Transmission Gate**

### 2.4 Binary LUT using SRAM for data writing and retrieval.

Circuit shown in fig.5 has 16 quaternary inputs (in1, in2, in16) one quaternary output (Out) and 2 quaternary control signal (sel1, sel2) to select appropriate input. Fig.5. Shows the binary LUT implemented using binary SRAM. This design is made up of 1 binary 16 to1 MUX and 16 binary SRAM. Here 16 inputs are given to the input node of SRAM to store the particular value in the SRAM, and 4 select lines are used to select the input.



**Fig.5 Binary LUT with SRAM**

### 2.5 Quaternary LUT using SRAM for data writing and retrieval.

The quaternary 16:1 multiplexer Shown in fig.6 is designed using 5 quaternary 4:1 MUX. It contains 6 (delta literal circuit) DLCs, 6 binary inverters and 84 transistors and its schematic is presented in figure. This circuit has 16 quaternary inputs (in1, in2,...,in16)one quaternary output (Out) and 2 quaternary control signal (sel1, sel2) that sets the output to one of the 16 inputs. For the select line sel1=0 and sel2=0. Input in1 is transferred to the output.
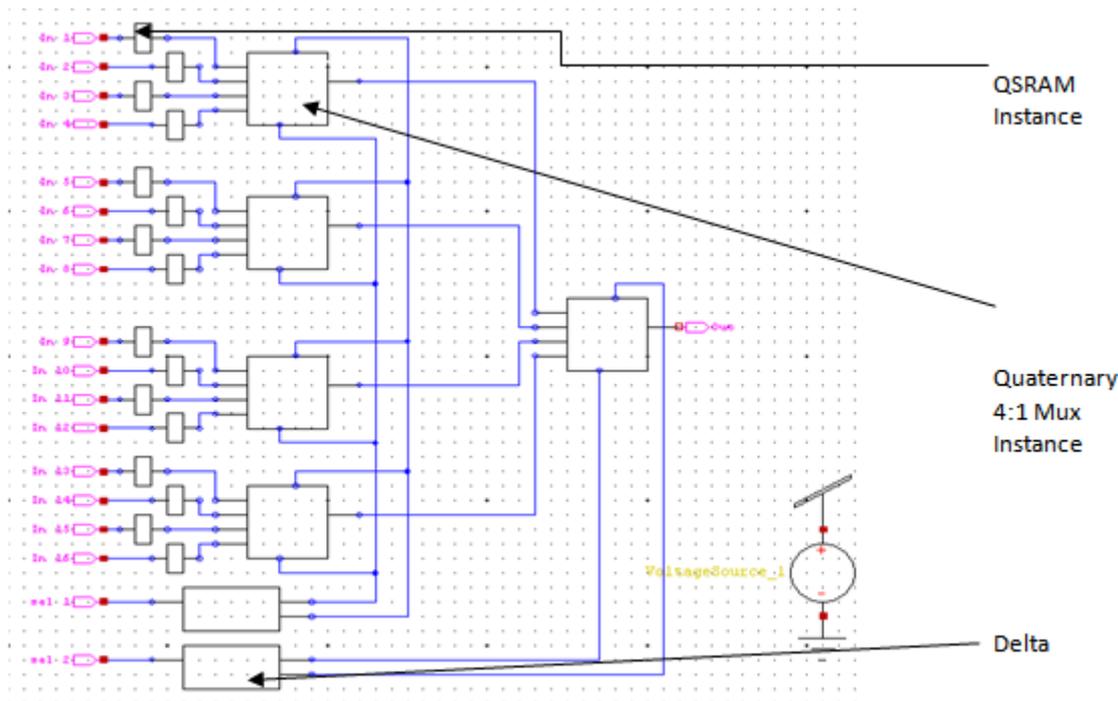
**Fig.6 Quaternary LUT with QSRAM**

Fig.6 shows the quaternary LUT with quaternary SRAM. This design is made up of 1 quaternary 16 to1 MUX and 16 number of quaternary SRAM. Here 16 inputs are given to the input node of SRAM to store the particular value in the SRAM. All inputs are previously stored in particular SRAM. Two select lines are used to select the particular input.

**2.5 Comparison of Propagation Delay**

Propagation delay time determine the input to output signal delay. Propagation delay is calculated for QLUT and it is compared with BLUT. The simulation result of the propagation delay is given by the tanner tool. Table III. Shows the comparison of the propagation delay of BLUT and QLUT. Here for load capacitance of 100fF, 400fF and 500fF propagation delay of quaternary LUT is reduced about 14.33%, 22.08% and 23.53% respectively. For 1000fF load capacitance, propagation delay of quaternary LUT is reduced by 29.71%.

**Table III. Propagation delay of BLUT and QLUT**

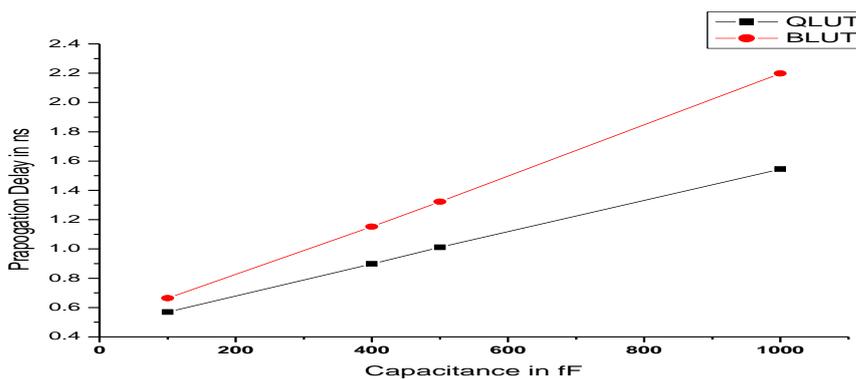| Capacitance (fF) | Device | Propagation delay (ns) | Rise time(ns) | Fall time (ns) |
|---|---|---|---|---|
| 100 | BLUT | 0.6641 | 2.2142 | 1.1430 |
|  | QLUT | 0.5689 | 156.8275 | 1.1585 |
| 400 | BLUT | 1.1522 | 4.0815 | 2.1785 |
|  | QLUT | 0.8977 | 158.8292 | 1.8555 |
| 500 | BLUT | 1.3223 | 4.7321 | 2.5297 |
|  | QLUT | 1.0112 | 159.5484 | 2.0913 |
| 1000 | BLUT | 2.1979 | 8.0663 | 4.4418 |
|  | QLUT | 1.5449 | 163.4007 | 3.3762 |

**Fig.7 Propagation delay for load capacitance variation**

## III. Power Consumption

### 3.1 Static power consumption

Static current in CMOS is negligible as long as VIN < VTN or Vin > VDD+VTP. Leakage current is determined by "off" transistor which is influenced by width of transistor, voltage supply, and threshold voltages. 2.72% static power reduced in QLUT as per this design.

**Table IV. Static power consumption of BLUT and QLUT**

| Parameter Considered : Power dissipation | BLUT | QLUT |
|---|---|---|
| Leakage current due to NMOS when Vin < VTN | 3.6051x 10 -10 W | 3.5097x 10 -10 W |
| Leakage current due to PMOS | 2.42nW | 1.78nW |

### 3.2 Dynamic power consumption

The Dynamic power consumption equation is as below,

$$P_{dyn} = CL\ Vdd^2\ Freq. \tag{4}$$

Cl is load capacitance, Freq is frequency of operation and Vdd is Supply voltage.

### 3.2.1. Input Capacitance of BLUT

The input capacitance of any circuit can be calculated by taking the sum of all the gate capacitances which are attached to an input of LUTs [11].

$$Cgate = Cox \sum_{i=0}^{n} (WL)\,i \tag{5}$$

Cox is a process parameter, and it is the capacitance (in Farads) per unit of square area calculated as,

$$Cox = \varepsilon ox\ /\ tox \tag{6}$$

Where tox is the oxide thickness= 5.6 x 10-9 for 250nm technology, the dielectric constant for silicon dioxide is $\varepsilon ox = 3.85 \times 8.85 \times 10 -12$. Using these values we calculate as follows.
Cox = 6.08 x 10-3  fF/$\mu m^2$ ,

$$cgate = \text{cox} \sum_{n=1}^{8} ((W.L)n)n + ((W.L)p)n\ \ = 61.71\ \text{Ff}$$

### 3.2.2. Output capacitance BLUT

Output parasitic capacitances consist of the gate to drain overlap capacitance Cov, drain junction capacitance made up of the junction-to-body capacitance Cjb, drain sidewall capacitance, Cjsw. For a transmission gate, the junction capacitance of the source and the drain, and overlap capacitance of the source and drain are considered [10] [5].

a.   Cov- Gate to Drain overlap capacitance:

The overlap capacitance will be equal for the drain overlap and source overlap capacitances [10]. Cov=CGD0 x W, where CGDO is a SPICE parameter. For an NMOS transistor, CGDO = 4.65 ×10 −10 F/m and for a PMOS transistor, CGD0 = 5.59 × 10 −10 F/m.

(Cov) n = 4.65x10e-10 x 2. 5x 10e-6   = 1.1625 fF,

(Cov) p = 5.59x10e-10 x 7.65 x 10e-6  = 4.27625 fF,
Hence avg cov = 2.7194 fF For 4 switching elements: 4 x cov  = 10.8776 fF

b.    Cjb-junction to body capacitance
The junction to body capacitance is made up of Cjb- junction-to-body capacitance, and Cjsw- side-wall capacitance.

$$Cjb= (W.D/VDD) \int_0^{VDD}\{CJ0/[1+Vj/Vb]^{\wedge}mj\} \, dVj \tag{7}$$

CJ0 is a SPICE parameter and is equal to CJ0 = 1.6989 × 10 −3 F/m2 for NMOS and 1.8579 × 10 −3 F/m2 for PMOS. V j is the voltage on the drain or source to body junction, and Vb is the built-in voltage across the said junction (0.69 V for NMOS and 0.90 V for PMOS), and VDD is the supply voltage [10]. mj is the grading coefficient and is equal to 0.4503 for NMOS and 0.4686 for PMOS. D is the length of the drain/source contact and it is 2.7 μm [10].
(Cjb) n = 1.2534 fF, (Cjb) p = 3.8172 fF,
Hence avg Cjb -= 2.5353 fF,
For 4 switching elements:  4 x cjb  =10.1412 fF
c.    Cjsw - sidewall capacitance

$$Cjsw= ((2D+W) /VDD) \int_0^{VDD}\{CJSW0/[1+Vj/Vb]^{\wedge}mjsw\} \, dVj \tag{8}$$

SPICE parameters CJ0 and MJ have been replaced with CJSW0 and MJSW respectively. CJSW0 = 3.8722 ×10 −10 F/m2 for NMOS and 3.8722 ×10 −10 F/m2 for PMOS, MJSW = 0.2881 for NMOS and MJSW = 0.3315 for PMOS [9].

(Cjsw) n= 2.1393 fF, (Cjsw) p= 3.1463 fF, Avg   Cjsw = 2.6428 fF
For 4 switching elements:  4 x Cjsw   =10.5712 fF

CL = Cin + Cov + Cjb +Cjsw   = 0.0933 pF.
Vdd = 3v at 1MHz freq.,

Pdyn = Cl Vdd2 Freq = 0.8397 μW
Pdyn = 0.8397 μW + 4 input inverters with 1pF cl
Pdyn = 0.8397 μW + 36 μW= 36.8397 μW

### 3.2.3    Input CAPACITANCE  for QLUT

$$cgate = cox \sum_{n=1}^{8}((W.L)n)n + ((W.L)p)n = 30.855\text{fF}$$

### 3.2.4    Output Capacitances for QLUT
a.    Cov- Gate to Drain overlap capacitance

$$Cov = Cgdo* \text{ x W} \tag{9}$$

(Cov) n = 4.65x10e-10 x 2. 5x 10e-6   = 1.1625 fF,
(Cov) p = 5.59x10e-10 x 7.65 x 10e-6 = 4.27625 fF,
Hence avg cov = 2.7194 fF,
For 2 switching elements:  2 x cov = 5.4388 fF
b.    Cjb-junction to body capacitance
(Cjb) n= 1.2534 fF, (Cjb) p = 3.8172 fF, Hence avg Cjb = 2.5353 fF,
For 2 switching elements: 2 x cjb= 5.0706 fF
c.    Cjsw - sidewall capacitance
(Cjsw) n= 2.1393 fF, (Cjsw) p= 3.1463 fF,

Pdyn =  p.d. of 4 transistors from DLC + P.d of TG
     = (4 x cl x vdd2 x fl) + cl x vdd2 x fl
     = 36μ + 0.4198 μ

Hence Avg Cjsw = 2.6428 fF
For 2 switching elements: 2x Cjsw= 5.2856 fF

Load capacitance: $CL = Cin + Cov + Cjb + Cjsw = 46.65$ fF
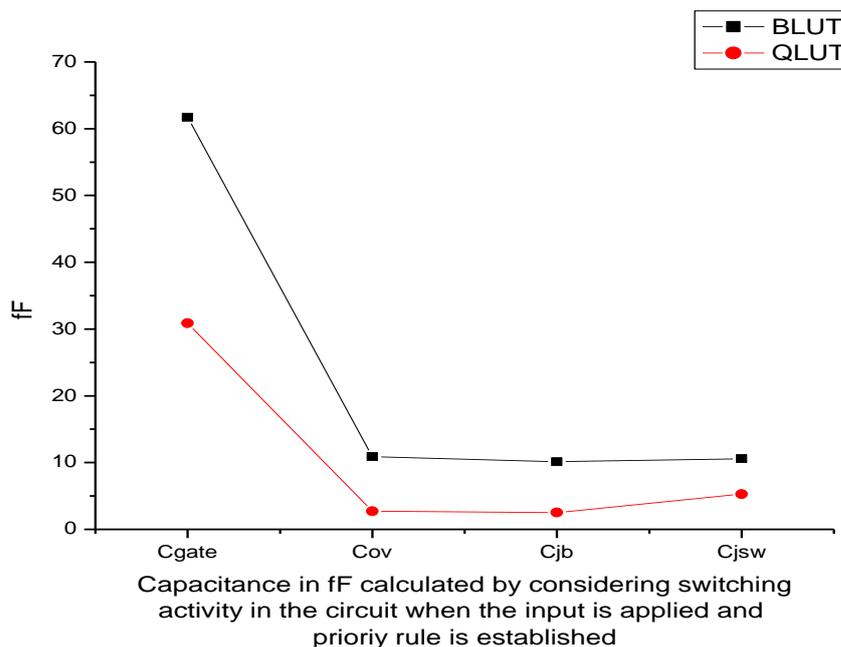Dynamic power dissipation is, $Pdyn = 36.4198$ µW



**Fig8. Parasitic Capacitances**

The Parasitics are less in Quaternary circuits as switching activity is less also data is represented in few number of bits as compared to binary.

**Table V  Propagation delay of BLUT and QLUT**

| Circuit | dynamic power dissipation(µW) |
|---|---|
| BLUT | 36.8397 |
| QLUT | 36.4198 |

### 3.3  Noise margin

In binary SRAM, for two logic values we get two storage nodes of SNM, so for quaternary logic there are four storage nodes of SNM [2].For quaternary SRAM inverter input/output characteristics can be shown as in figure 8.

Cell ratio (CR) is the ratio between sizes of the driver transistor to the load transistor during the read operation [1]. Pull up ratio (PR) is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation [5][1]. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage. Driver transistor is responsible for 70 % value of the SNM [5] [1].
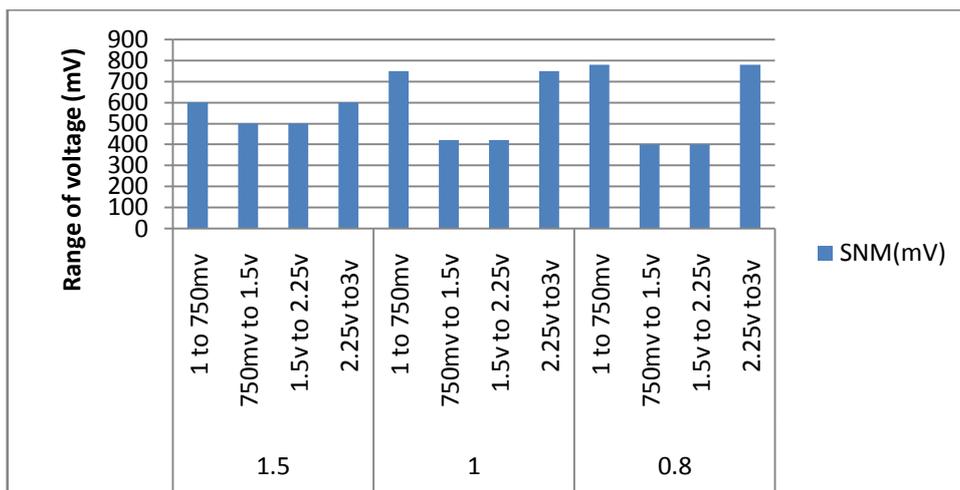
**Fig.9 SNM and Cell Ratio variation in quaternary SRAM.**

The Lower noise margin for this design is 400mV below which it will fail to recognize proper voltage level.
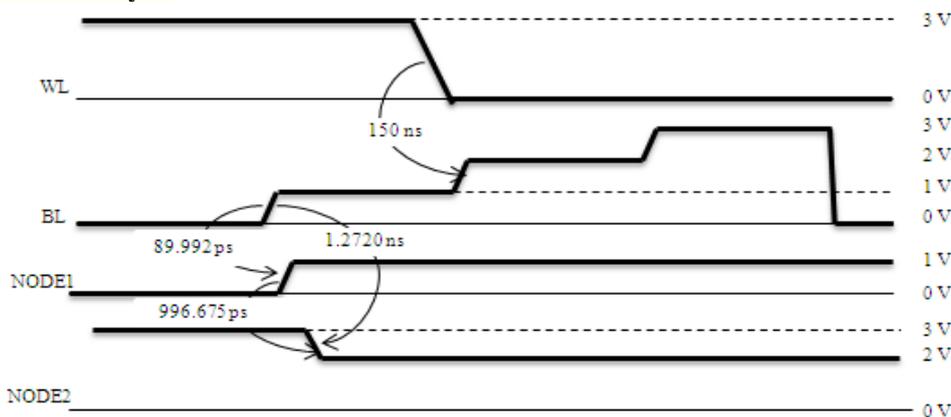
### 3.4 Access Time Analysis



**Fig.10 Data rate during read and write operation.**

The bit rate of the quaternary SRAM is calculate  $1/(26.6447 \text{ ps} * 10) = 3.7531 \times 10^{-3} \times 10^{12m}$    $= 3.7531 \times 10^9$ bps [5]

**Table VI  Bit RATE OF BLUT and QLUT**

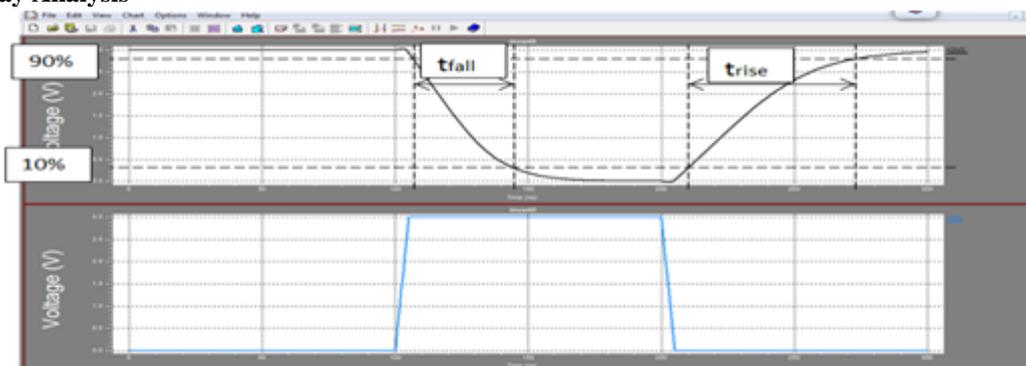| Bit rate of SRAM | Bits / sec |
|---|---|
| Binary SRAM | 1.9832 x106 bps |
| Quaternary SRAM | 111.12      107 bps |

### 3.5 Delay Analysis



**Fig. 11  Rise and fall time waveform.**

**Table VII Propagation DELAY OF BLUT and QLUT**

| Device | Binary inverter | Quaternary inverter |
|---|---|---|
| Propagation delay (ns) | 1.3598 | 0.6456 |
| Rise time (ns) | 4.00 | 2.1049 |
| Fall time (ns) | 4.00 | 150.4610 |

Reduction in propagation delay of Quaternary Inverter is 52.52%

Following are findings from this analysis.
• Bit rate is increased than binary SRAM.
• Changing the Cell Ratio, we got different speed of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, for hence current also increases.
• As current is an increase, the speed of the SRAM cell also increases.

## IV. Experimental Results

### 4.1 Quaternary Inverter

Simulation results of quaternary inverter shows that the input is given as 0v, 1v, 2v and 3v, and output is exactly invert of the input as 3v, 2v, 1v, and 0v.
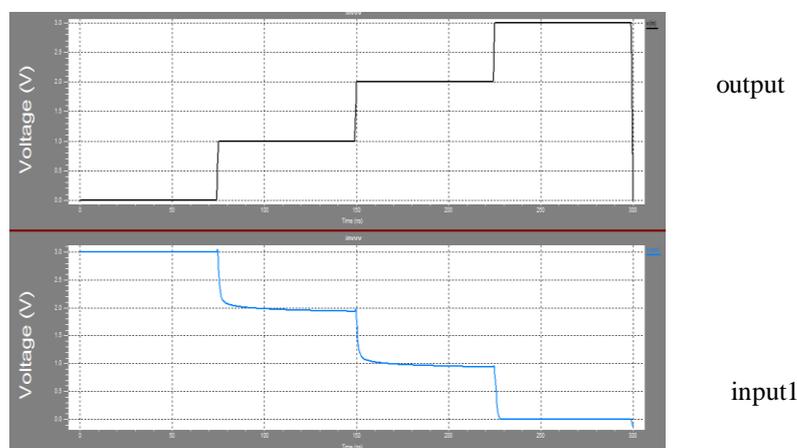


**Fig. 12 Input and Output waveform of Quaternary inverter**

### 4.2 Simulation result: BLUT

Fig.12. Shows the simulation result of the quaternary LUT. By selecting the select line as sel1=0 and sel2=0, I can get input 1(BL1) is as output of the LUT. WORD LINE (WL) is used to choose the mode of operation either read operation or write operation. Word line = 3v is used for the read operation and 0v is used for write operation.
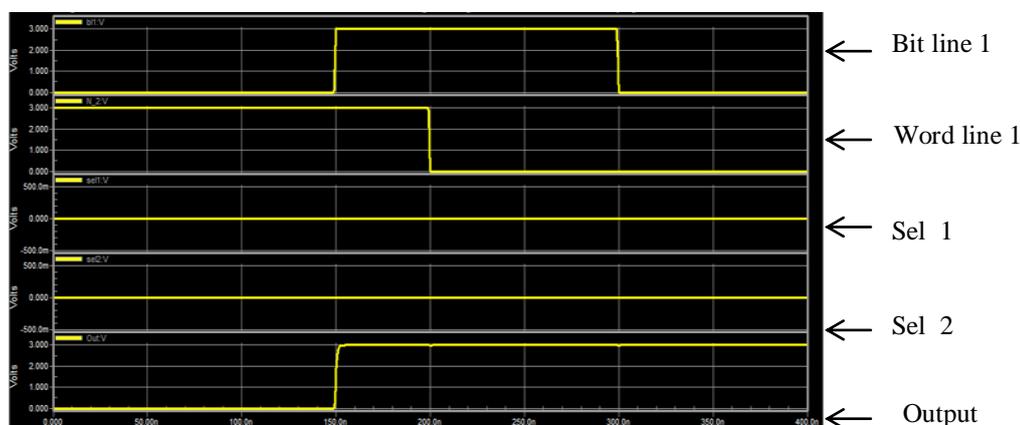


**Fig. 13 Simulation result BLUT**

During write operation word line is high and data is written in the binary SRAM through bit line 1. And during read operation word line become low and data is stored in the binary SRAM. In the simulation result

word line is at the state of 3v for write operation. Bit line at the input1 is given as 0v 3v 0v. But when the value of bit line is 3v the word line goes from 3v to 0v. 0v of word line indicate the read operation, so 3v can be read at the output at the time of read operation.

### 4.3  Simulation result: QLUT

Here For select line 1 and 2 as "0", bit line 1 is connected to the output.  During write operation word line is high and data is written in the quaternary SRAM through bit line 1. And during read operation word line become low and data is stored in the quaternary SRAM.
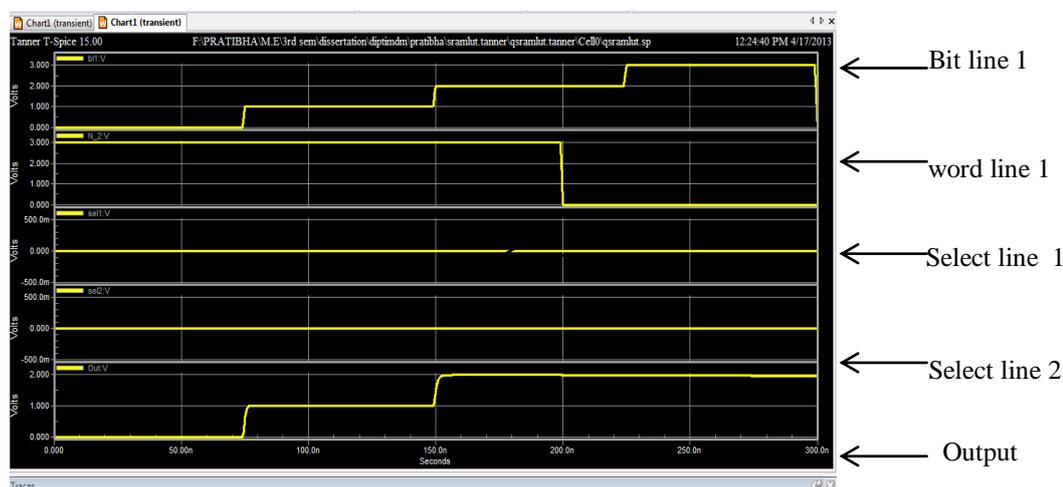


**Fig. 14 Simulation result QLUT**

In the simulation result word line is at the state of 3v for write operation. Bit line at the input1 is given as 0v 1v 2v 3v. But when the value of bit line is 2v the word line goes from 3v to 0v. 0v of word line indicate the read operation, so 2 V can be read at the output at the time of read operation.

### 4.4  Simulation result: Quaternary transmission gate

Depending upon four different logic levels present at the input of transmission gate input, corresponding levels present at pass input that logic is forwarded to output.
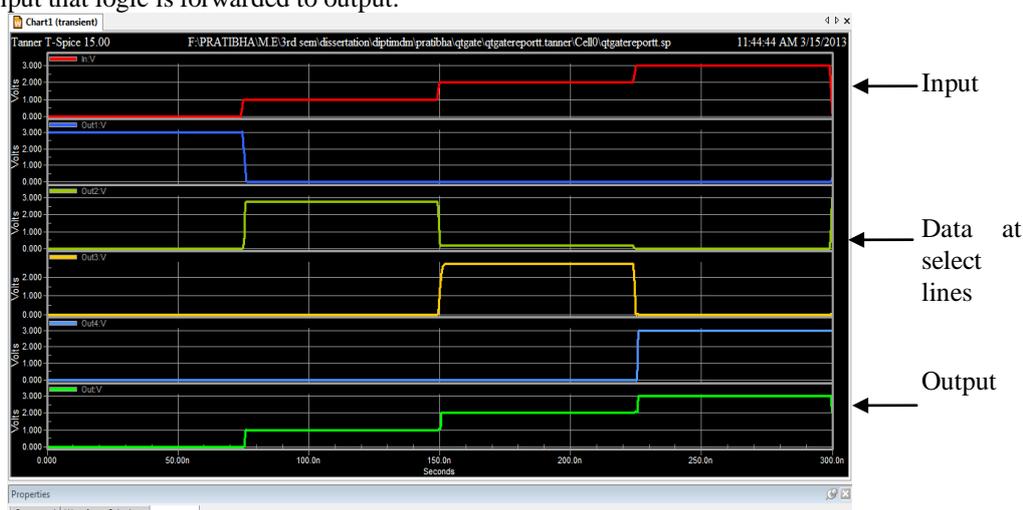


**Fig. 15 Simulation result Quaternary TG**

### 4.5 Simulation result: Quaternary SRAM

Here for quaternary SRAM cell quaternary inverters are used instead of binary inverters. The data being held in the memory cell will be interpreted as a logic"0" or logic"1" or logic"2" or logic"3". Fig.15 shows bit line can store four level of logic values as logic 0, logic 1, logic 2 and logic 3.When word line is at logic high state then SRAM cells writes in cell whatever data present at bit line , which can be seen from node1.Similarly when word line is logic low level then previous data available for reading.
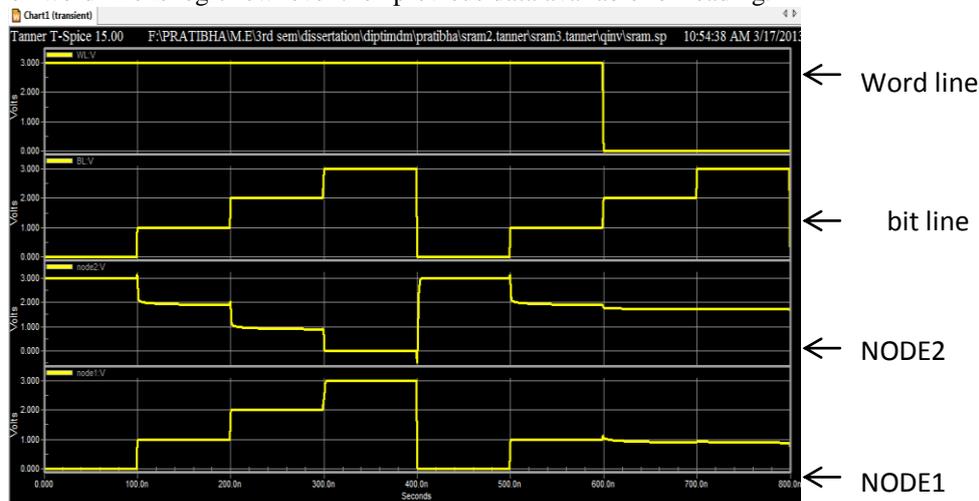


**Fig. 16 Simulation result Quaternary SRAM**

## V.  Conclusion

The continued scaling of the technology has meant that designs that were limited by the amount of functionality on a chip are now limited by the amount of constrained power This works explains implementation quaternary LUTs which are faster than conventional memories , adding a quaternary logic to LUTs increases its functionality , reduces interconnects by representing information in fewer possible bits. Propagation delay of quaternary SRAM is reduced up to 78.32%, and for the LUTs with SRAM, power dissipation is increased about 2.02% but static power dissipation is reduced by 43.11% and propagation delay of QLUT is reduced up to 29.71%. Technology variation is to be done for this design considering noise margin issues. From result and analysis it is evident that quaternary circuits may increase some circuit complexity but are able to process more information, also still these circuit relay on binary counterpart for basic implementation so basic ASIC for these circuits are made from MOS transistor used in binary logic design.

## Acknowledgements

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