IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 5, Issue 4, Ver. I (Jul - Aug. 2015), PP 43-48
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Performance Analysis of 10 T Full Adder Using SVL and Power Gating Technique for Reducing Leakage Current at 45 nm Technology

Vinod Agarawal[1], Ravi Shiravastav[2], Sourabh Khandelwal[3], Shyam Akashe[4]
[1](Research Scholars, ITM , Gwalior, India),[2](Department of ECE, ITM , Gwalior, India),
[3](Department of ECE, ITM , Gwalior, India), [4](Department of ECE, ITM University , Gwalior, India)

Abstract: *In microprocessor and digital signal processor, Full Adder performs addition and therefore it is used for arithmetic operation and is also used for comparison and access the address in memory. For highly efficient operation of low powered and battery operated portable devices, Full adder is implemented using different structures. There is a 1-bit full adder using10 transistors are proposed in this paper. There are two techniques 1) power gating technique and 2) SVL (switch controllable voltage level) technique are proposed for reducing leakage current. The results based on power gating technique and SVL technique show that leakage current of 10 transistors based1-bit Full Adder are reduced to a large extent. For ten transistors based 1-bit Full Adder, delay is also reduced as compare to conventional full adder. All simulation results for leakage current and delay are performed with 45nm CMOS technology, 20ns access time and 0.05GHZ frequency using cadence virtuoso tool.*

Keywords: *CMOS, Full Adder, leakage current, power gating technique, SVL*

I. Introduction

In VLSI, the whole research is on reducing the size of transistors and reducing the number of transistors for implementing any system. Today technology comes from micrometer to nanometer with reducing the length of gate (i.e. transistor's size) up to 45nm and now approximately 100 million transistors per cm^2 can be grown on a single chip. In this way transistor's density on chip increases and whole of the system can be fabricated on single chip. For the systems like microprocessors and digital signal processors, ALU (arithmetic and logic unit) perform arithmetic and logical operation. In ALU, Full Adder performs the addition bit by bit with carry input and provides output with carry output. The carry output becomes the carry input for next input combination.

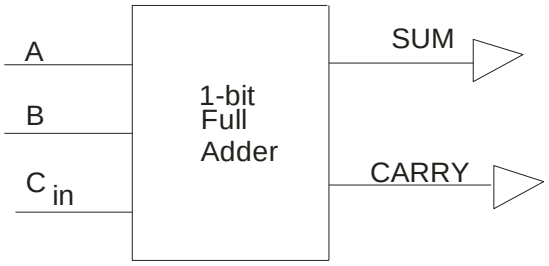

Fig.1 Symbol diagram of 1-bit full adder

There are three types of basic structure on which Full Adder is based static, dynamic and hybrid. Static Full Adder are less power consuming than dynamic and then more reliable. Dynamic Full Adder have faster switching speed, full swing voltage level and less number of transistors but suffer from charge sharing, clock load, high power dissipation due to high switching activity and complexity [1], [2]. Hybrid full adder is basically the combination of static and dynamic Full Adder [4], [1]. There are number of research papers focus on different type of structures of full adder based on different logic structure design and also based on the way of expression of logic function. For implementing the full adder in nanotechnology we have to focus on important parameter like delay, power dissipation and number of transistors. There are 42 transistors are used to implement the sum and carry function in full adder. In standard complementary CMOS logic, full adder is implemented using 28 transistors by implementing the sum output using carry output. In this paper, a 1-bit full adder is implemented using 10 transistors so that delay and power dissipation are reduced to a large extent [3]. Power consumption in nano-technology is basically due to leakage current power dissipation which is considered negligible as compare to dynamic dissipation in past technology. For reducing leakage current, two techniques 1) power gating technique and 2) SVL technique are presented in this paper.

II. Proposed 1-Bit 10T Full Adder

There are number of research papers focus on different types of full adder depend on the number of transistors. Here 1-bit SERF (static energy recovery Full adder) full adder named 10T13A using ten transistors is implemented. The modified logic equation for implementing proposed adder is

SUM = A ⊕ B ⊕ C & SUM = (A ⊕ B) ⊕ C

CARRY = AB + BC + CA & CARRY = A. (A ⊕ B)' + (A ⊕ B). C

The sum function can be implemented by using XOR or XNOR and multiplexer is used for implement the carry signal is shown in figure.

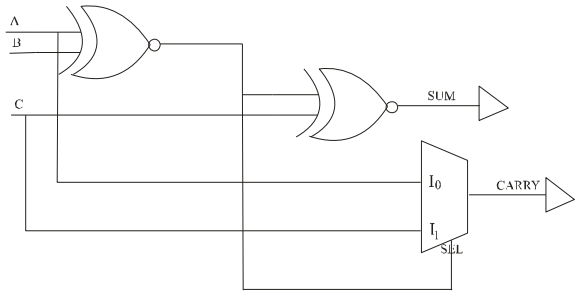

Fig.2 Gate Level Diagram of 10T13A Full Adder

The sum function is implemented by cascading of 4 transistor based ground less static energy recovery type XNOR circuit with inverter based XNOR circuit [2]. [5] The carry function is implemented by multiplexing of input A and C with intermediate signal (A ⊕ B)'as a select signal. Here the 2 x 1 multiplexer is implemented with 2 transistors using pass transistor logic. The transistor level schematic of 10T13A Full adder is shown in figure.

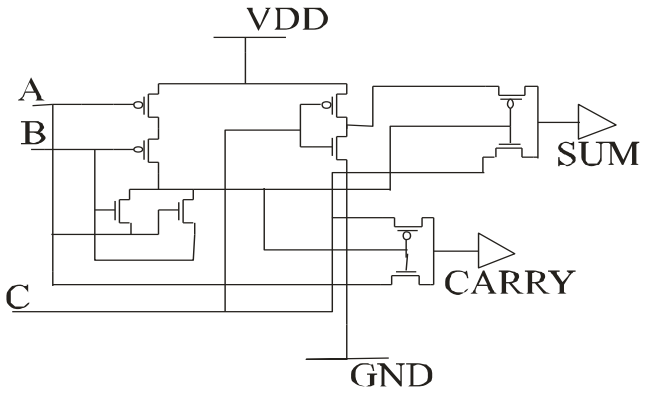

Fig.3 Transistor Level Schematic of 10T13A Full Adder

This SERF type full adder use energy recovery technique and then less power dissipation. The static energy recovery technique can be understood by the working of 4T groundless XNOR in which initially both inputs A and B equal to zero and capacitance at the output node are charged up to VDD. Now input B becomes high while input A is kept low then capacitor is discharged by input A and some charge stored by input A. Now when A becomes high then it is not required to charge fully because of some charge storage and energy is recovered as compare to conventional full adder [6],[7],[8]. In this way power consumption is reduced we can save chip area with reduction in number of transistors.

III. Problems in full adder

The pass transistor logic for implement the carry function is responsible for the problem of threshold voltage loss and also for degradation in voltage swing at output level. This degraded output voltage swing lead to slow switching for cascaded operation of circuits like Ripple carry Adder, Carry Select Adder etc. Therefore at low VDD cascading of 1-bit full adder is not possible [2], [3]. Operating speed mainly depends on propagation delay of transistors, number of inversion and intra-cell wiring capacitance. By reducing the number of transistors propagation delay is reduced as compare to conventional standard full adder but due to technology advancement interconnect delay become responsible for operating speed reduction. Power dissipation in CMOS circuits is mainly due to node capacitance, transistor size and switching activity of transistors. By the reduction of transistors power dissipation is reduced but due to advancement in technology power is dissipated due to leakage current. In CMOS devices leakage current are of many types. 1) Sub threshold leakage current is the current which sink from drain to source of transistors when gate source voltage VGS is less than VTH (i.e. transistors are

in cut off regions) [10]. When MOS device operating in weak inversion (sub threshold) region then sub threshold leakage current is the diffusion current of the minority carriers. The equation for sub threshold leakage current is

$$\mathrm{IDS} = \mathrm{K}\left(1 - \mathrm{e}^{\frac{\mathrm{VDS}}{\mathrm{VT}}}\right).\mathrm{e}^{(\mathrm{VGS} - \mathrm{VT} + \eta.\mathrm{VDS}/\mathrm{nVT})}$$

Where k and n are technology function, η is drain induced barrier lowering coefficient.sub threshold leakage current also depend on temperature supply voltage, device size, and threshold voltage etc [10].We can reduce sub threshold leakage current using higher threshold VTH in some part of design. 2) Another type of leakage current is called gate leakage current in which main current sink from gate to substrate of transistor within the sio2 layer beneath the gate [10]. We can use multiple thickness of oxide layer to decrease the gate leakage. 3) Junction tunneling leakage current can varied as an exponential function of reverse bias voltage and junction doping. It produces in reverse bias region due to generation of electron hole pair in the depletion region and due to diffusion of minority carriers near depletion region [10].

IV. Proposed work

Today CMOS technology is scaled down up to 45nm and consequently supply voltage and also threshold voltage has been decreased. Reduced threshold voltage exponentially increase sub threshold leakage current in such a way that more than 40% of total power is dissipated by leakage current while leakage current power dissipation was negligible in past CMOS technology. So it is a need to introduce leakage reduction techniques. Different techniques like MTCMOS technique, drain gating technique, voltage scaling technique, VTCMOS technique, stacking technique are used for reduce leakage current. In this paper two techniques 1) power gating technique and 2) SVL technique is proposed for reducing leakage current.

A. Power Gating Technique

Here power gating technique is applied on 10T13A full adder by using high threshold voltage PMOS and NMOS transistors switches for providing VDD voltage supply and ground voltage supply respectively for low threshold voltage PMOS and NMOS transistors based full adder load circuit [11]. The transistor level schematic of 10T13A full adder with power gating technique is shown in figure.

Different threshold voltages are used therefore power gating technique also known as multi threshold CMOS technique (MTCMOS) technique. There are two mode for application of power gating technique 1) active mode and 2) standby mode. In active mode PMOS and NMOS transistors switches are on and therefore provide virtual VDD voltage supply and ground voltage supply for load circuit and circuit starts to work [12]. In standby mode PMOS and NMOS transistors switches are off and therefore disconnect from VDD voltage supply and ground voltage supply for load circuit and circuit comes in standby mode. Here the sub threshold leakage current is reduced by increased body effect. Fast switching of lower threshold voltage transistors provide better critical delay path for 10T13A full adder load circuit but more static power dissipation. Using high threshold voltage transistors for non critical delay path, leakage current, power dissipation, and noise can be reduced. However, there is a need of additional fabrication processes for portioning and sizing of high threshold voltage PMOS and NMOS transistors provide restriction for use of power gating technique [13].

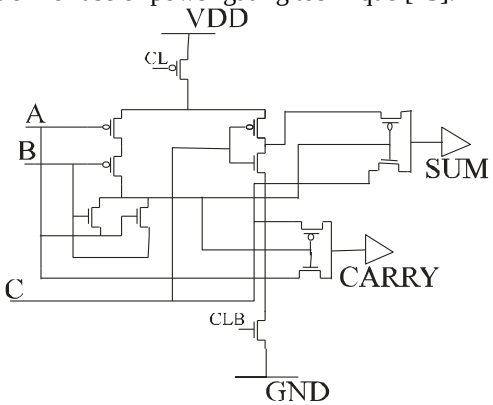

Fig.4 Transistor Level Schematic of 10T13A Full Adder with Power Gating Technique

B. SVL (self controllable voltage level) technique

Here SVL technique is applied on 10T13A full adder by using two approaches 1) USVL (upper self controllable voltage level) for providing VDD voltage supply and 2) LSVL (lower self controllable voltage level) for providing ground voltage supply for PMOS and NMOS transistors based full adder load circuit. The transistor level schematic of 10T13A full adder with SVL technique is shown in figure.

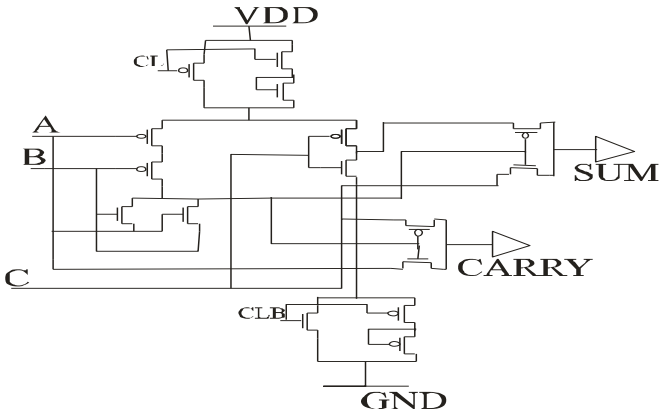

Fig.5 Transistor Level Schematic of 10T13A Full Adder with SVL Technique

USVL circuit consists a parallel combination of single PMOSFET switch (p-SW) and several NMOSFET resistors (n-RS) in series and LSVL circuit consists a parallel combination of single NMOSFET switch (n-SW) and several NMOSFET resistors (p-RS) in series. In active mode both p-SW and n-SW are 'on' while n-RS and p-RS are 'off'. Hence maximum supply voltage VD = VDD and minimum ground level voltage VS (= VSS = 0) are supplied to the active load circuit of full adder. In this way operating speed for full adder is also enhanced. In standby mode both p-SW and n-SW are 'off' while n-RS and p-RS are 'on' and therefore dc voltage supply for load circuit is decreased and ground voltage supply for load circuit is increased [14], [15]. Here DIBL (drain induced barrier lowering) effect is reduced due to application of both USVL and LSVL and Back gate bias (BGB) effect is also increased due to LSVL. Thus there is increase in threshold voltage VTHN and consequently reduction in total leakage current [16].

C. Simulation result

Here the 10T13A static energy recovery Full Adder (SERF) is simulated for input and output waveform. In this paper the simulations, for calculation of leakage current in standard 28 T full adder, proposed 10T13A Full Adder and 10T13A Full Adder with proposed power gating and SVL technique are performed and then results are compared. The simulation results show that the leakage current in conventional full adder is reduced by 54.6% using proposed 10T13A full adder and the leakage current in 10T13A Full adder is reduced by 69.4% and 48.6% using 10T13A Full Adder with proposed power gating and SVL technique respectively. All simulations are performed at 45nm technology using cadence virtuoso tool.

Table.1 Table for comparison of leakage current in different full Adder

Reduction scheme	Temperature in deg. Celsius	Voltage (mV)	Leak. current (pA)
Conv. Full Adder	27	700	2.932
10T13A Full Adder	27	700	1.329
10T13A with SVL	27	700	.6831
10T13A with power Gating	27	700	.1434

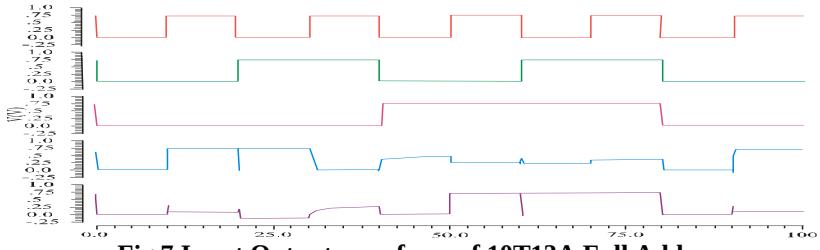

Fig.7 Input Output waveform of 10T13A Full Adder

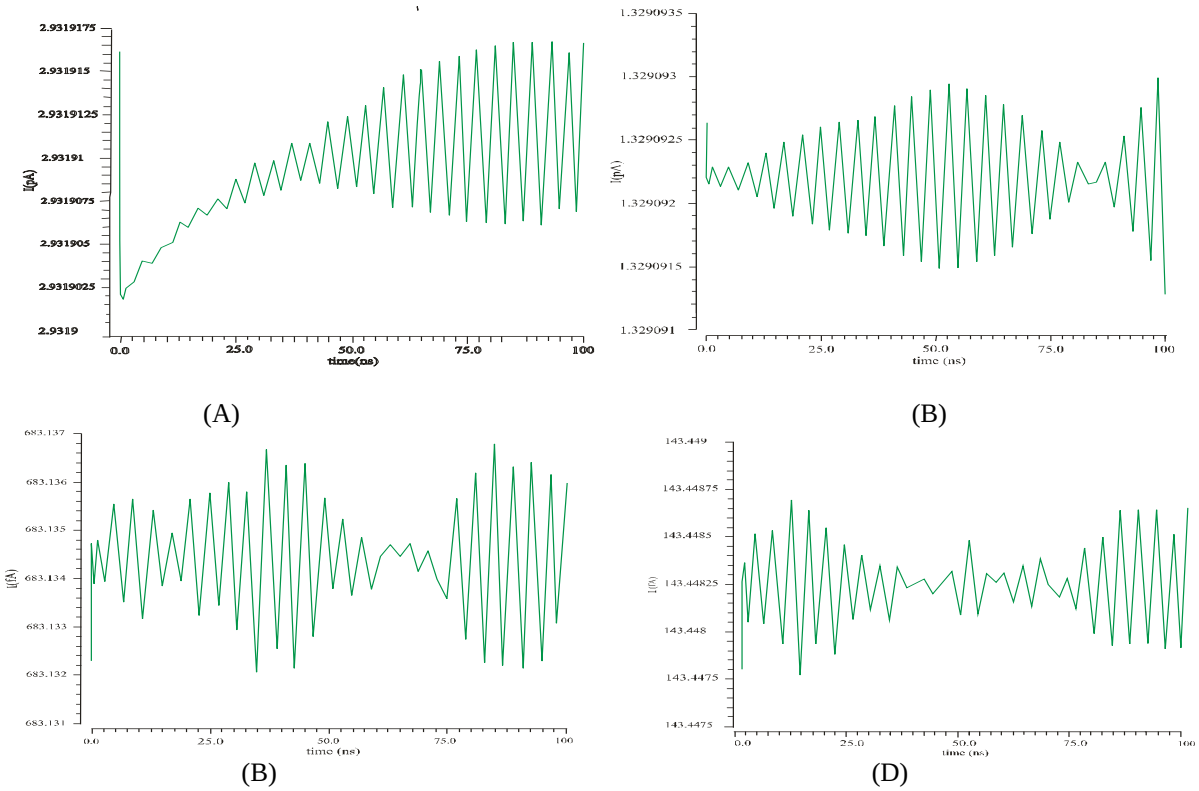

Fig.8 Simulation of Leakage Current in (A)conv. Full Adder (B)10T13A Full Adder (C)10T13A Full Adder with SVL technique (D)10T13A Full Adder with Power Gating technique

V. Conclusion

In this paper a 1-bit full adder named 10T13A with 10 transistors using static energy recovery technique is implemented. 10T13A Full Adder's simulation for input and output waveform shows the degradation of output voltage level due to use of pass transistor logic. Simulation result shows that leakage current in 10T13A Full Adder is reduced as compare to standard 28 T Full Adder due to reduction of transistors. There are two techniques are proposed 1) power gating technique and 2) SVL technique for further reduction of leakage current. Power gating technique reduces leakage current using different threshold voltages and SVL technique reduces leakage current through increasing threshold voltage using USVL and LSVL approaches. Simulation result shows that power gating technique is better in comparison of SVL technique for reducing leakage current but there is additional fabrication process for power gating technique.

Acknowledgements

This work was supported by ITM Gwalior, with collaboration Cadence Design System, Bangalore.

References

[1]. Deepak Garg, Mayank Kumar Rai. 2012. CMOS Based One Bit Full Adder Cell for Low Power Delay Product. IJECCT. vol. 2, issue. 4, pp. 18-23.

[2]. Subodh Wairya, Rajendra Kumar Nagaria, sudarshan tiwari. 2012. Comparative Performance Analysis of XOR XNOR Function Based High Speed Cmos Full Adder Circuits for Low Voltage VLSI Design. International Journal of VLSI Design and Communication System. vol. 3, No.2, pp. 221-242.

[3]. Richa Saraswat, Shyam Akashe and Shyam Babu Designing and Simulation of Full Adder Cell Using FINFET Technique in Proceedings of 7th International Conference on Intelligent Systems and Control (ISCO),2013 pp. 261-264.

[4]. Suresh, G., Rao, C. S. 2014. Performance Evaluation of Full Adder And its Impact on Ripple Carry Design. International Journal of Research in Engineering and Technology. Vol. 3, No. 4, pp. 23-28.

[5]. Yingtao Jiang, Abdul Karim Al-Sheraidah, Yuke Wang, Edwin Sha and Jin Gyun Chung "A Novel Multiplexer based Full Adder", IEEE Transaction on circuit and system vol. 55, No. 7, July 2013, pp. 01–04.

[6]. M.B. Damle, Dr. S.S Limaye*, M.G. Sonwani "Comparative Analysis of Different Types of Full Adder Circuits", IOSR Journal of Computer Engineering, Vol. 11, No.3, May. - Jun. 2013 PP 01-09.

[7]. Neeraj Devarari, Shashank Sundriyal "EFFICIENT DESIGN METHODOLOGIES AND POWER COMPARISON FOR FULL ADDER CIRCUITS", in proceeding of ISTP Journal of Research in Electrical and Electronics Engineering (ISTP-JREEE) 1st International Conference on Research in Science, Engineering & Management pp. 93 – 98.

[8]. Deeprose Subedi, Eugene John "STANDBY LEAKAGE POWER REDUCTIONIN NANOSCALE STATIC CMOS VLSIMULTIPLIER CIRCUITS USING SELFADJUSTABLE VOLTAGE LEVEL CIRCUIT", International Journal of VLSI design & Communication Systems (VLSICS), Vol.3, No.5, October 2012, pp. 01–12.

[9]. Amit Agarwal, Kaushik Roy "A Noise Tolerant Cache Design to Reduce Gate and Sub-threshold Leakage in the Nanometer Regime" ISLPED,Vol.3, august,(2003).
[10]. Vandana Sikarwar, Saurabh Khandelwal and Shyam Akashe). Optimization of Leakage Current in SRAM Cell using Shorted Gate DG FinFET. In proceeding of 3rd International Conference on Advanced Computing and Communication Technologies (ACCT 2013). pp. 166-170.
[11]. Shyam Akashe, Nitesh Kumar Tiwari, Jayram Shrivas and Rajeev Sharma "A Novel High Speed & Power Efficient Half Adder Design Using MTCMOS Technique in 45 Nanometre Regime", in proceeding of IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), 2012, pp. 157-161.
[12]. Raju Gupta, Satya Prakash Pandey, Shyam Akashe, Abhay Vidyarthi "Analysis and optimization of Active Power and Delay of 10T Full Adder using Power Gating Technique at 45 nm Technology", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Vol. 2, Issue 1, (Mar. – Apr. 2013), pp. 51-57.
[13]. Anuj Kumar Shrivastava, Shyam Akashe "Design of Low Power 14T Full Adder Cell Using Double Gate MOSFET With MTCMOS Reduction Technique AT 45 Nanometer Technology", International Journal of Nanoscience, Vol. 12, No. 6 (2013), pp. 01-06.
[14]. Khandelwal, S., Akashe, S. 2011. Supply Voltage Minimization Techniques for SRAM Leakage Reduction. Journal of Computational and Theoretical Nanoscience. Volume. 9, No. 8, pp. 1044-1048.
[15]. Manorama., Khandelwal, S. and Akashe, S. 2013. Design of a FinFET based Inverter using MTCMOS and SVL Technique reduction Technique. in proceeding of 2013 Students Conference on Engineering and Systems (SCES), Allahabad, India, pp. 1-6
[16]. Tadayoshi Enomoto,Yoshinori Oka, Hiroaki Shikano: "A Self Controllable Voltage Level Circuit And its Low Power High Speed Cmos Circuits Application" IEEE Journal of Solid Circuit,Vol.38, No.7, (2003). pp. 1220-1226.