# Performance Optimization of Dynamic and Domino logic Carry Look Ahead Adder using CNTFET in 32nm technology

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***Abstract:*** *Advanced electronic device technologies require faster operation and less average power which are the most important parameters in VLSI design. Conventional CMOS technology is found to have threshold voltage and sub threshold leakage problems in scaling of device which fail to adapt in sub-micron and nano technologies. The carbon nanotube field effect transistor (CNTFET) technology overcomes the threshold voltage and sub threshold leakage problems even though the size is reduced. Most of the fast adders are based on being able to calculate the carry propagation much faster without having to wait for it to ripple through each bit of the adders. The carry look ahead (CLA) technique is the most commonly used scheme for accelerating carry propagation. In this paper, a CNTFET based carry look ahead adder is evaluated with HSPICE simulation in 32 nm technology, using Domino and NP dynamic CMOS techniques which effectively suppress both dynamic switching and leakage power consumption without increase in propagation delay.*
***Keywords:*** *Carry look ahead adder, CNTFET, Domino logic, NP Dynamic logic*

## I. Introduction

Today VLSI industry requires ultra high speed processors, more functionality, portable devices, low chip area and also low power consumption. To fulfil above requirements there is a need to scale the devices and interconnects and follow Moore's law. But, CMOS device scaling leads to Leakage currents, Channel length and doping control, Short channel effects like IDBL, velocity saturation and mobility degradation which are undesirable. There are also problems in copper interconnect scaling like Electro-migration, Hillock and void formation, and Diffusion barrier width. These limits can be overcome to some extent by modifying the channel material in the traditional bulk MOSFET structure with the single Carbon Nanotube or an Array of Carbon Nanotubes.

Carbon nanotube (cnt) based technology develops the most promising devices among emerging technologies because it has most of the desired features. Cnfets are the novel devices that are expected to sustain the transistor scalability while increasing its performance. Recently, there have been tremendous advances in carbon nanotube technology for nanoelectronics applications. Cnfets avoid most of the fundamental limitations and offer several advantages compared to silicon-based technology.

## II. Carbon Nanotube Field Effect Transistor

Carbon Nanotube Field-Effect Transistors (CNFETs) are considered to be promising candidate devices for future technology nodes due to their superior electrostatic and transport properties.CNTs are sheets of graphene rolled into tubes, depending on the chirality (i.e., the direction in which the graphene sheet is rolled), a single-walled CNT can be either metallic or semiconducting. Parallel semiconducting CNTs are grown or transferred to a substrate of CNTFET. A typical structure of a MOSFET-like CNTFET device is illustrated in Fig.1. The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. The conductivity of these undoped regions is controlled by the gate. With ultralong ($\sim$1 µm) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance.
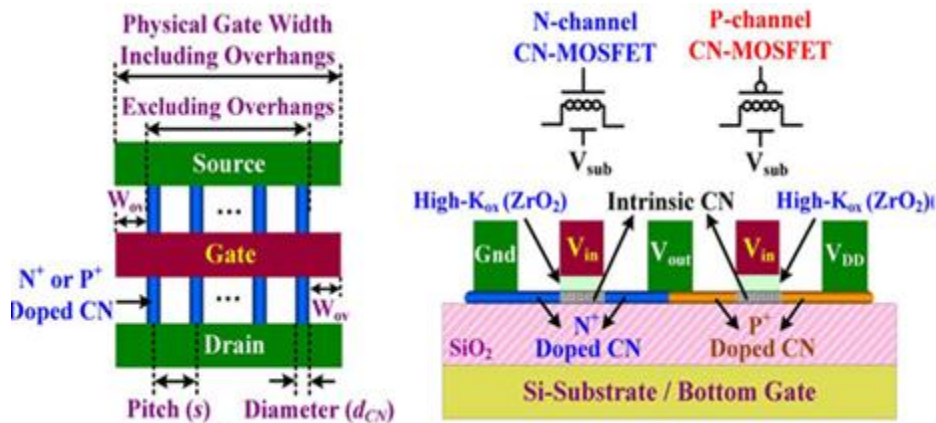
**Figure 2.1** Structure of CNTFET

Chirality: CNTFET utilizes a single carbon nano-tube or an array of carbon nano-tubes as the channel material instead of bulk silicon in the traditional MOSFET structure. It was first demonstrated in 1998. The structure of CNT described by an index with a pair of integers (n, m) that define its chiral vector.

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}\,n}{2m+n}\right)$$

$$d_t = \frac{L}{\Pi} = \frac{a}{\Pi}\sqrt{n^2 + nm + m^2}$$

Metallic when n = m. It has a small Band gap when n − m = 3i
Semiconducting when n − m ≠ 3i

The chiral angle is used to separate carbon nanotubes into three classes differentiated by their electronic properties:
armchair (n = m, Θ = 30°),
zig-zag (m = 0, n > 0, Θ = 0°),
chiral (0 < |m| < n, 0 < Θ < 30°).
Channel length (Lch): The channel length is chosen to reduce the occurrence of scattering. In this paper, Lch=10nm is chosen as it is less than Mean Free Path and scattering does not occur.
Diameter (D): Diameter of CNT is between 1.2nm and 1.8nm. In this range, the chirality vectors for zigzag tubes is (16, 0) (17, 0) (19, 0) (20, 0) (22, 0) (17, 0) is chosen as the chirality vector.
Diameter is given by

$$D = \frac{n\sqrt{3}\,a_{cc}}{\Pi}$$

where n=chirality vector and $a_{cc}$=lattice constant = 0.142nm for graphene. Diameter obtained is 1.33nm.
Pitch: Pitch is the minimum distance 2 adjacent carbon nanotubes. Here, pitch is calculated to be 4nm. Pitch is calculated by

$$Pitch = \frac{W_g - d}{N - 1}$$

$W_g$ = Gate width = 32nm, d = Diameter, N = Number of Parallel Channels = 9
Oxide Thickness ($t_{ox}$): For channel length of 10nm, the $t_{ox}$ is prescribed to be 2nm.
Dielectric constant ($k_{ox}$): The dielectric constant for graphite is between 12 and 15. As k increases, power consumption reduces. So value chosen for $k_{ox}$=15.
Length of doped CNT source-side extension region ($L_{SS}$): As channel length is 10nm, length of source side extension is also considered as 10nm.

Length of doped CNT drain-side extension region ($L_{dd}$): As channel length is 10nm, length of drain side extension is also considered as 10nm.

From, Stanford CNFET model physical channel is set as 32nm. This paper is implemented with hspice tool using 32nm technology. In comparison to Silicon based devices, CNTFET provides better control over channel formation, better threshold voltage, better sub-threshold slope, high mobility, high current density and transconductance.

## III. CNTFET based 32 bit Carry Look Ahead Adder

Carry look ahead adders (CLAs) are commonly used in modern processors. In this paper, the adders are designed as two-stage pipelines for high speed operation. Each pipeline stage contains 5 levels of dynamic logic gates and 5 levels of domino logic gates in the NP dynamic and domino adders, respectively. The input vectors of a 32-bit CLA are denoted as A (A1 to A32 ) and B ( B1to B32). The carry input and clock input of the adder are denoted as Cin and CLK_IN, respectively. The sum output and carry output for each bit position i ($1 < i < 32$) are denoted as Si and Ci, respectively.

### 3.1 NP Dynamic Logic Adder

The operation of the NP dynamic CMOS adder is as follows. When the clock signal CLK is low, the complementary clock signal CLKB is high. The CLK pipeline-stage is in precharging/predischarging phase, while the CLKB pipeline-stage is in evaluation phase. In the -stage, the dynamic nodes (P1_b ~ P16_b , G1_b ~ G16_b , C5_b ~ C8_b , and C13_b ~ C16_b ) of the n-type dynamic logic gates are precharged to VDD through the corresponding p-channel precharge transistors. Alternatively, the dynamic nodes ( C1~C4 and C9~C12) of the p-type dynamic logic gates are pre-discharged to 0 V through the n-channel pre-discharge transistors. In the CLKB pipeline-stage, the inputs of the dynamic gates are evaluated. If the pull-down transistor networks of the n-type dynamic logic gates are turned off by the corresponding input vectors, the dynamic outputs (P17_b ~ P32_b , G17_b ~ G32_b , C21_b ~ C24_b , and C29_b ~ C32_b ) are maintained at by the p-channel keepers. Alternatively, the dynamic outputs are discharged if the pull-down transistor networks of the n-type logic gates are activated. Similarly, the dynamic outputs (C17 ~ C20 and C25 ~ C28) are maintained at 0 V by the n-channel keepers provided that the pull-up transistor networks of p-type dynamic gates are cut off. The dynamic nodes are charged to VDD if the pull-up transistor networks of the p-type logic gates are activated. The carry output of the 32-bit CLA (C32) is determined by A17~A32 , A17_b~A32_b , B17~B32, B17_b~B32_b, and C16_b' . The sum outputs to are determined by A17~A32, A17_b~A32_b , B17~B32, B17_b~B32_b, C16~C31 and C16_b'~C31_b. Subsequently, when CLK and CLKB transition to high and low, respectively, the inputs of the dynamic gates in the CLK-stage are evaluated while the CLKB -stage is in precharging/predischarging phase.
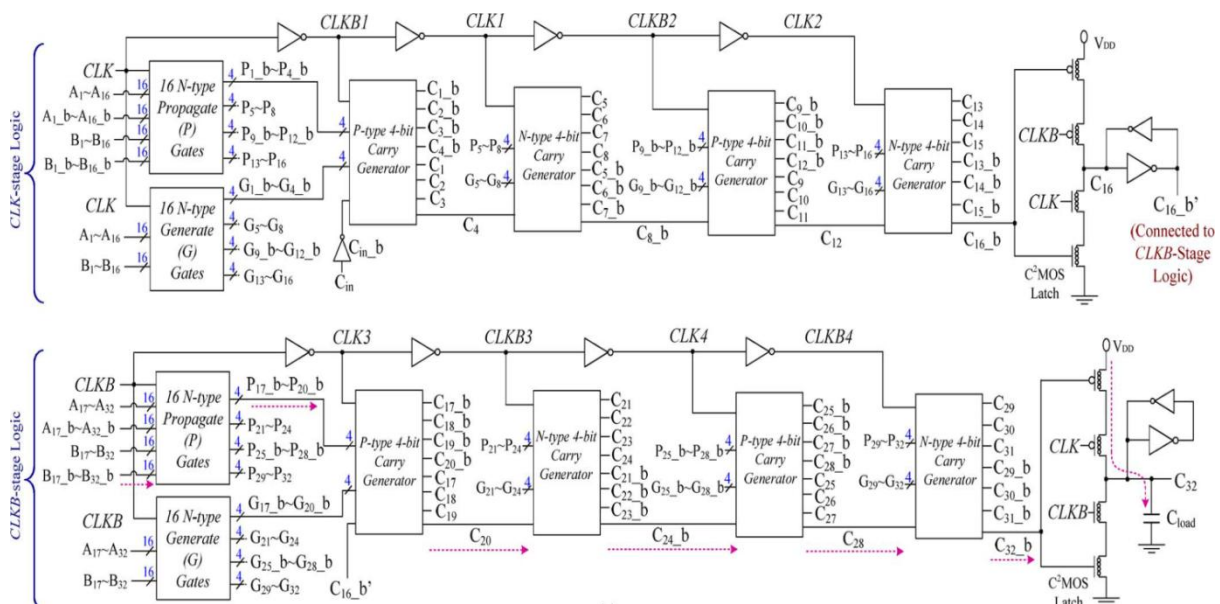


**Figure 3.1** 32-bit carry generator of the NP Dynamic logic CLA

### 3.2 Domino logic adder

Domino logic circuits are considered with n-type dynamic gates due to the higher electron mobility as compared to the hole mobility in silicon CMOS technology. The CN-MOSFET domino adder is also composed of only n-type dynamic gates in this study. The clock signals are properly delayed to eliminate the short circuit current paths at each level. The operation of the domino logic CLA is similar to the NP dynamic CLA.
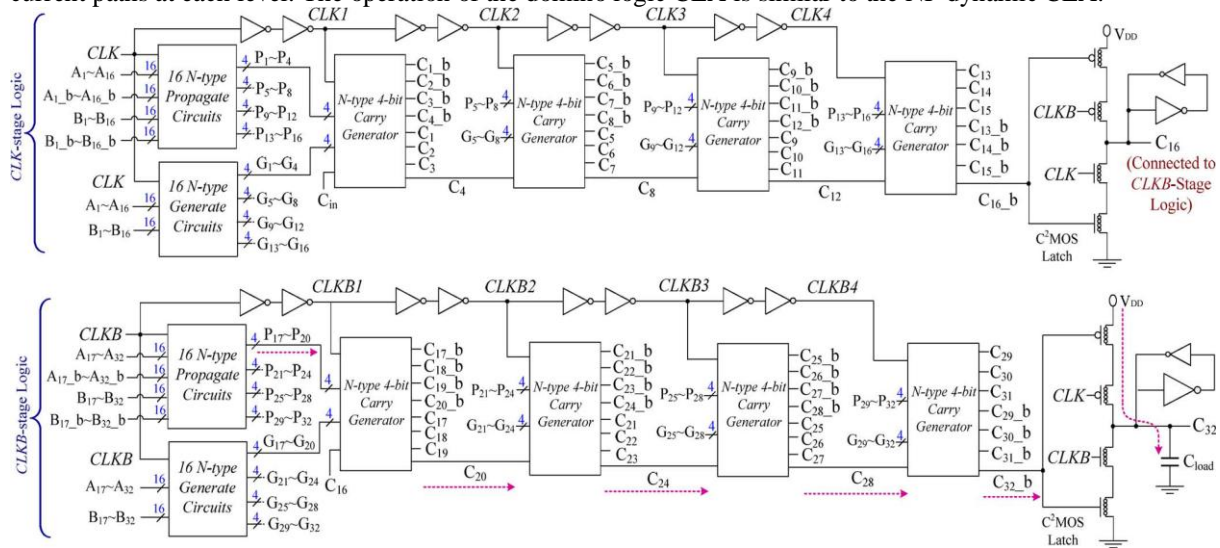


**Figure 3.2** 32-bit carry generator of the NP Dynamic logic CLA
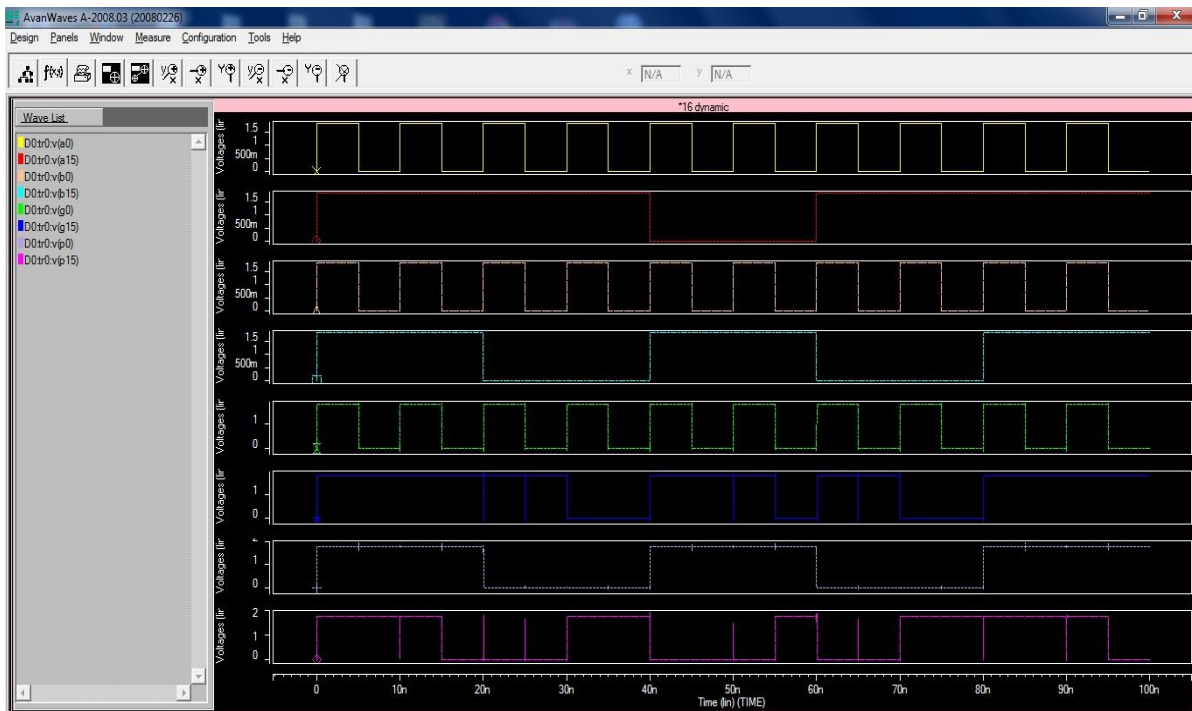
# IV.    Results

NP Dynamic logic



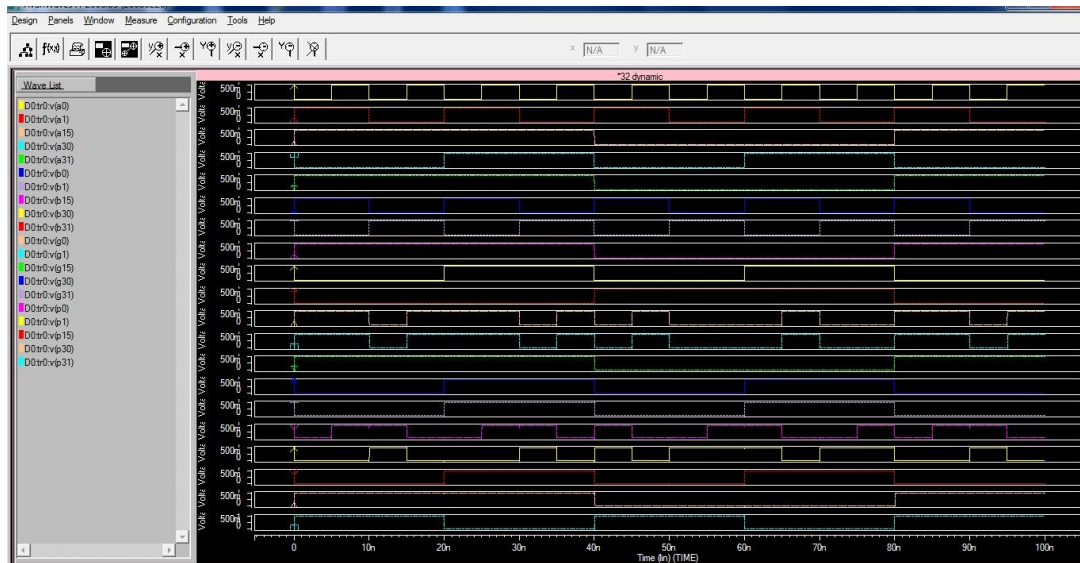**Figure 4.1** Output of 16 bit NP Dynamic CLA

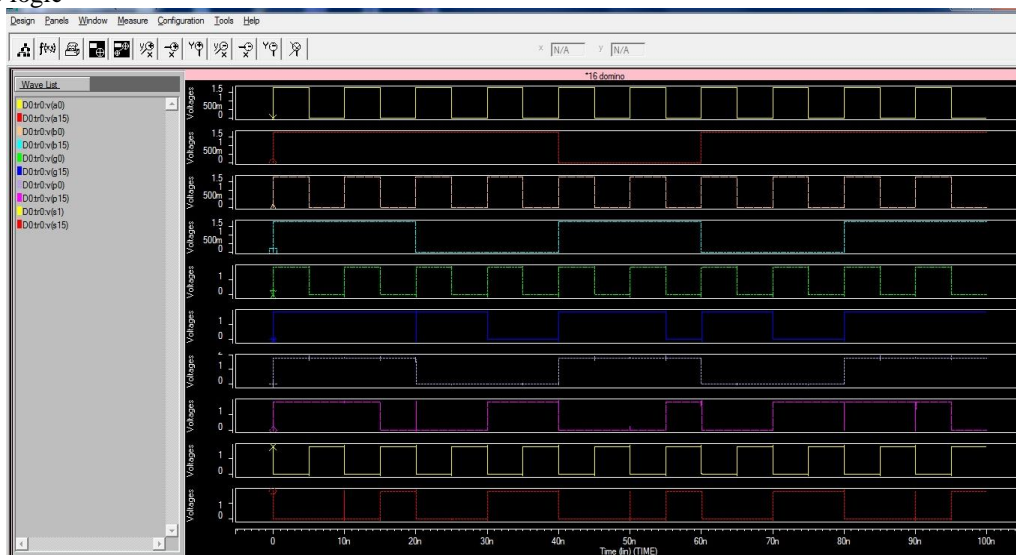**Figure 4.2** Output of 32 bit NP Dynamic CLA

Domino logic



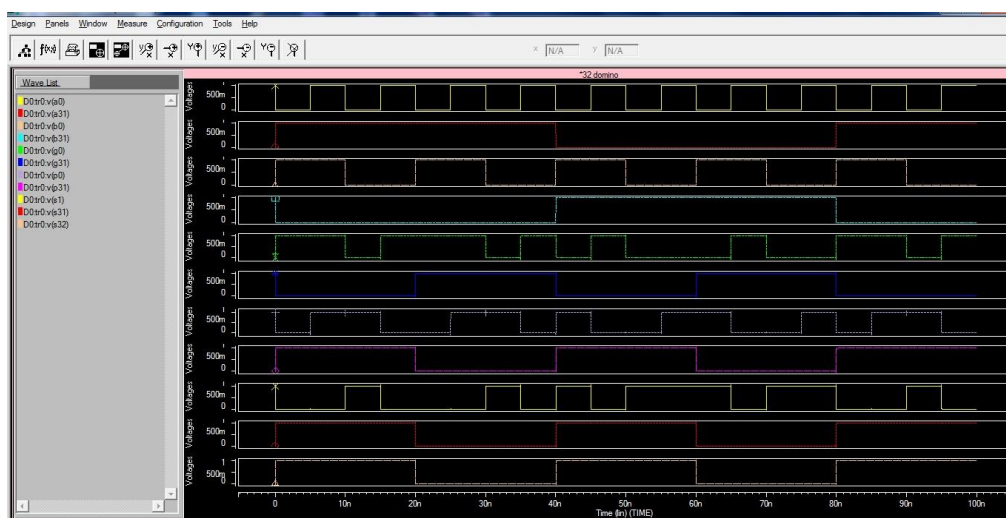**Figure 4.3** Output of 16 bit Domino logic CLA



**Figure 4.4** Output of 32 bit Domino logic CLA

**NP Dynamic Logic Adder**

**Table 1:** TOTAL POWER DISSIPATION, PROPAGATION DELAY, POWER-DELAY PRODUCT OF CN-MOSFET AND SI-MOSFET 32-Bit CARRY LOOKAHEAD ADDERS.

| Parameter | 16 bit | | 32 bit | |
|---|---|---|---|---|
| | Silicon | Carbon | Silicon | Carbon |
| Total power dissipation(watts) | 132.9407u | 61.7694u | 323.3528u | 76.8077n |
| Propagation Delay(s) | 155.61p | 385.05f | 262.36p | 680.36f |
| Power delay product(J) | 20.686E-15 | 23.78E-18 | 84.834E-15 | 52.256E-21 |

**Domino Logic Adder**

**Table 2:** TOTAL POWER DISSIPATION, PROPAGATION DELAY, POWER-DELAY PRODUCT OF CN-MOSFET AND SI-MOSFET 32-Bit CARRY LOOKAHEAD ADDERS

| Parameter | 16 bit | | 32 bit | |
|---|---|---|---|---|
| | Silicon | Carbon | Silicon | Carbon |
| Total power dissipation(watts) | 212.7797u | 63.5934u | 234.8754u | 79.3373n |
| Propagation Delay(s) | 96.388p | 658.85f | 174.63p | 339.27f |
| Power delay product(J) | 20.50E-15 | 41.89E-18 | 41.016E-15 | 23.916E-21 |

# V. Conclusion

Low-power, compact, and high-performance NP dynamic CMOS circuits with a 32 nm carbon nanotube transistor technology are presented in this paper. The performances of four 32-bit carry lookahead adders with different circuit techniques and technologies are characterized: Si-MOSFET domino logic, Si-MOSFET NP dynamic CMOS, CN-MOSFET domino logic, and CN-MOSFET NP dynamic CMOS. The carbon nanotube transistor technology is recommended as a better alternative to the conventional CMOS logic family for the implementation of future high speed digital integrated circuits.

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