High-Performance of Domino Logic Circuit for Wide Fan-In Gates Using Mentor Graphics Tools

Yalaganda Merlin[1], Minchula Vinodh Kumar[2]
[1](ECE, M.Tech Student, MVGR College of Engineering, India)
[2](ECE, Assistant Professor, MVGR College of Engineering, India)

Abstract: *Domino logic circuit is power efficient circuit, so it is widely used in digital design of applications. In this paper, a new domino circuit technique is proposed to have less power consumption. New technique is proposed to overcome the contention problem and reduces the power dissipation and it provides high noise immunity. Simulation results are shows the efficiency and effectiveness of the domino circuit. The domino circuit will reduce the power consumption. In this proposed circuit Simulations are done by using 130nm Mentor Graphics Editor Tools, with supply voltage 1V at 100MHz frequency and operating temperature of 27˚C, 110˚C for up to 64 input OR gates. The proposed circuit has small area, low power and high speed circuits for wide fan-in gates. The proposed circuit gives power improvement by proposed circuit for 32 input OR gate is 91.148% than HSD, 84.019% than CKD, 84.021% than LCR and 97.368% better power dissipation than CCD similarly improvement of area for proposed 64 fan-in OR gate is 8.724% than HSD, 13.129% than LCR, 20.176% than CCD.*

Key words: *Domino logic, noise immunity, keeper transistor, power dissipation, wide fan-in gates.*

I. Introduction

DOMINO logic circuit such as dynamic circuit, Which is widely used in many of the applications to achieve high performance, high-density, which cannot achieved with static logic styles. Power consumption is divided into two parts which are static and dynamic power consumption circuits. While discussing about low power, less area, and high speed preferably dynamic logic instead of static logic circuits. But the drawback of dynamic logic families is that they are more sensitive than static logic families in noise. By generating proper logic in dynamic logic to achieve high performance, by which all the properties of the dynamic node makes it robust circuit. Main limitations of dynamic logic occur during cascading of large circuit an enormous state occurs. Another problem for cascading of dynamic logic circuit is charge sharing which reduces the dynamic node voltage. To overcome the cascading problem a week keeper transistor is introduced in parallel to pre-charge transistor, which is feedback from the output node. A week keeper transistor is introduced with small W/L ratio. On the other hand, the supply voltage for low-power is drastically reduced, and the threshold voltage (V_{th}) is scaled down to achieve high-performance. Since by reducing the threshold voltage which exponentially increases the sub-threshold leakage current and reduction of leakage current, improving noise immunity are the major concerns in robust circuit and high-performance designs. Especially for wide fan-in domino gates which are typically employed in the read path of register files, tag comparators, programmable logic arrays, and wide multiplexer-flip-flop (MUX) and De-MUX, ALUs and DSP circuits.

The novelty of the proposed circuit is that our proposed work simultaneously increases performance as well as decreases leakage power consumption. To improve the efficiency of the circuit and performance the microprocessor, modifications are done on the circuit level to improve the robustness of the circuit without the penalty of noise immunity. The Keeper transistor is added to the robust circuit upsizing is a conventional method to improve the robustness of the domino circuit. A keeper is added in pre-charge node to improve the robustness of the dynamic node. The keeper ratio (K) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor, Where W and L denotes the size of the transistor, μ_n and μ_p are the mobility of the electron and hole respectively. As the keeper transistor is added at the output node of the logic feedback from the output. The keeper transistor W/L maintains very low to maintain charge in dynamic logic.

$$K = \frac{\mu p \left(\frac{W}{L}\right) \text{Keeper transistor}}{\mu n \left(\frac{W}{L}\right) \text{Evaluation transistor}}$$

Where W and L denote the transistor size, μ_n and μ_P are the mobility of electron and hole respectively. As the keeper transistor and the evaluation network increases in the evaluation phase this cause an increase in the evaluation delay, power consumption of the circuit and degrading the performance. Therefore keeper upsizing may not be a viable solution for high leakage immunity problem in scaled domino circuit. Several techniques are introduced to address the session. This paper is organized as follows. In the section 2 Literature review about existing domino circuit is discussed. In Section 3 the proposed circuit description is discussed. In Section 4 Simulation result is presented and compared with the brief conclusion of the paper in section 5.

II. Literature Review

Several circuit techniques are proposed in the literature to address these issues. The main goal of these circuits is to reduce leakage and power consumption for wide fan-in gates. High speed domino logic and conditional keeper are among the most effective solutions for improving the robustness of domino logic [6-9].

2.1 High – Speed Domino Logic (HSD):

The circuit of the High Speed Domino logic is shown in Fig. 1. The HSD logic operates as follows: When the clock is LOW during pre-charge, the dynamic node is pre-charged to V_{DD}. Transistor MN1 is OFF, P1 is ON charging the gate of the of the keeper transistor Q2 to V_{DD}, thus turning Q2 OFF. Q2 is OFF at the Beginning of the evaluation phase. Contention is thus eliminated between the keeper and the pull-down devices during evaluation. Therefore, the domino gate evaluates faster and no contention current exists. When the delayed clock becomes "1", the gate output is "1" if the Domino node evaluates to "0" and N1 is ON thus keeping Q2 OFF. If all the pull-down devices are OFF, the at Domino node stays "1",Causing the gate output to be "0",Which in turn discharges the keeper's Gate through N1.Therefore the keeper turns ON to maintain the voltage of the Domino node at V_{DD} and to compensate for any leakage currents. HS-Domino solves the contention problem by turning the keeper OFF at the start of the evaluation cycle. The keeper width can be sized up as V_{TH} scales down to maintain a controlled NMOS without worried about increasing the contention, and speed degradation

2.2 Conditional Keeper Domino Logic (CKD):

The conditional keeper domino (CKD) has a variable strength which is shown in Fig.2. The conditional keeper domino logic shows the operation of CKP on the output of the pre-charged gate. If the dynamic output should remain high, then the keeper transistor is weak during the state of the output transition window and strong for the rest of evaluation time. The weak keeper during the transition window results in reduced contention and fastest output transition, while the strong keeper is good robustness to leakage and noise during the rest of evaluation time. Fig.2. shows the circuit implementation with two keepers which are fixed keeper P_{K1}, and conditional keeper P_{K2}. At the time of the evaluation phase i.e. clock fluctuates from Low-to-High the P_{K1} is the only active keeper. After a delay time, the keeper transistor P_{K1} is activated i.e.

$$T_{KEEPER} = T_{DELAY \ ELEMENT} + T_{NAND}$$

The conditional keeper domino circuit works as follows: At the beginning of the evaluation phase, the fixed keeper P_{K1} is ON state for keeping the state of the dynamic node. If the dynamic node is still high, after delay of the inverters, the output of the NAND gate goes too low to turn on conditional keeper transistor P_{K2}. The conditional keeper transistor is sized larger than P_{K1} to maintain the state of the dynamic node for the rest of the evaluation period. If the dynamic node is discharged to the ground then the Conditional keeper transistor remains OFF. CLK logic has some problems like limitations on decreasing delays of the inverters and the NAND gate to improve noise immunity. Noise immunity can be improved by upsizing delay inverters, but this significantly increases power dissipation.

2.3 Leakage Current Replica Domino Logic (LCR):

Sub-threshold is tracked using a replica circuit, and mirrored into the dynamic gate keeper. The replica current mirror can be shared with all dynamic gates 1 FET overhead/gate Tracks all process corners as well as temperature and V_{DD}. In leakage current replica keeper, current mirror circuit is added to the keeper of standard footer less domino logic. Transistor m1 of the mirror circuit is connected in diode configuration, i.e., gate of the PMOS transistor is connected to the drain. By doing like this both gate and drain of the PMOS transistor is at potential voltage level of the keeper. Keeper voltage is same as the potential of drain of keeper transistor mk1. This leakage current replica keeper reduces the power consumption. Operation of circuit is as follows, in pre-charge phase, when clock is low and all the inputs are at low level, dynamic node charged up to V_{DD}. During pre-charge phase, output is at low which turns on the keeper transistor M_{K2} and it acts as a short circuit transistor. Now the drain of M_{K1} transistor is directly connected to the dynamic node and due to the diode

configuration of this keeper transistor M_{K1} drain voltage of M_1 is also at the logic low level of dynamic node. High voltage of drain of M_1 transistor reduces the leakage current. In this way, the leakage power is reduced.

2.4 Current-Comparison Domino Logic (CCD):

In case of wide fan in gates, the capacitance of dynamic node is large and then speed decreases severely. Due to the cause of large parallel leaky paths, power consumption increases and the noise immunity reduces. These problems will be solved if pull down implements logic function is divided from keeper transistor by comparison stage in which current of pull up network compared with the worst case leakage current. The Current-Comparison Domino Logic circuit has five additional transistors and a shared reference circuit when compared to other domino logic styles. Here current of the pull up network is mirrored by transistor M_2 and compared with the reference current, which replicates the leakage current of the pull up network. This Current-Comparison Domino Logic circuit employs PMOS transistors to implement OR logic functions. By using the n-well process, source and body terminals of the PMOS transistors can be connected together such that the body effect is eliminated. So the voltage of transistors is only varied due to the process variation and not the body effect.

This CCD circuit can be divided to two stages. The first stage is pre-evaluation stage and second is domino stage. The first stage pre-evaluation network includes the pull up network and transistors $M_{PRE,}$ M_{EVAL} and M_1. The pull up network which implements the desired logic is disconnected from dynamic node (DYN), unlike traditional dynamic logic circuits, and indirectly changes the dynamic voltage. The second stage is domino stage has one input without any charge sharing, one transistor M_2 regardless of the implemented OR logic in the pull up network and a keeper which has two transistors. Hence only one pull up transistor is connected to the dynamic node instead of connecting all transistors in the OR gate to reduce capacitance on the dynamic node. The Current-Comparison Domino Logic circuit is operated in two phases, pre-discharge phase and evaluation phase. Here dynamic power dissipation is reduced in the evaluation phase. This dynamic power dissipation is divided into two parts. First part is for the first stage of the Current-Comparison Domino Logic circuit and the second part is for the second stage. The dynamic power dissipation directly depends upon the capacitance, voltage swing, and leakage current on the switching node, frequency, power supply and temperature. Here power dissipation is reduced in both the stages. The first stages with N-input has a lower voltage swing V_{DD} to V_{TH} and has no leakage current due to less capacitance at dynamic node. The second stage has rail to rail voltage with minimum leakage. So by reducing voltage swing and capacitance, the dynamic power is reduced in both the stages with little area overhead.
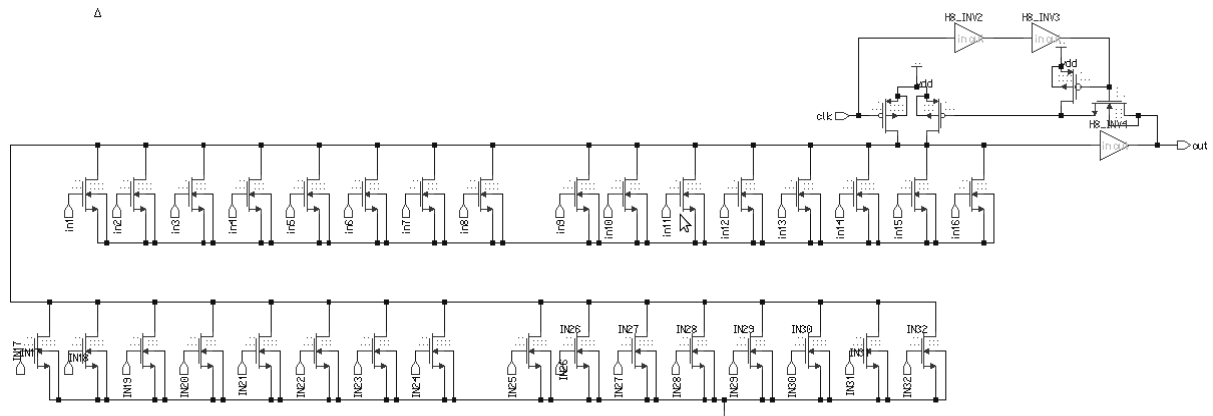

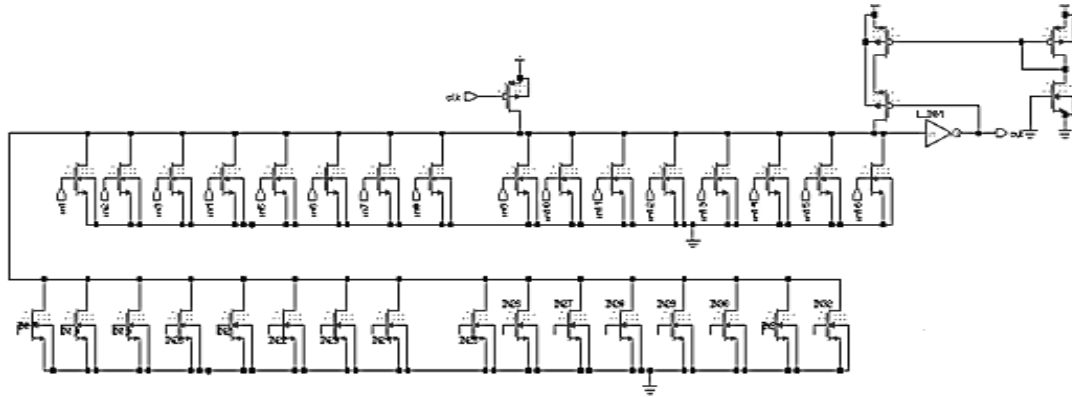Fig.1: High Speed Domino Logic for Wide Fan-In Gates

Fig.2: Schematic of Leakage Current Replica Keeper (LCR) for Wide fan-in OR gate
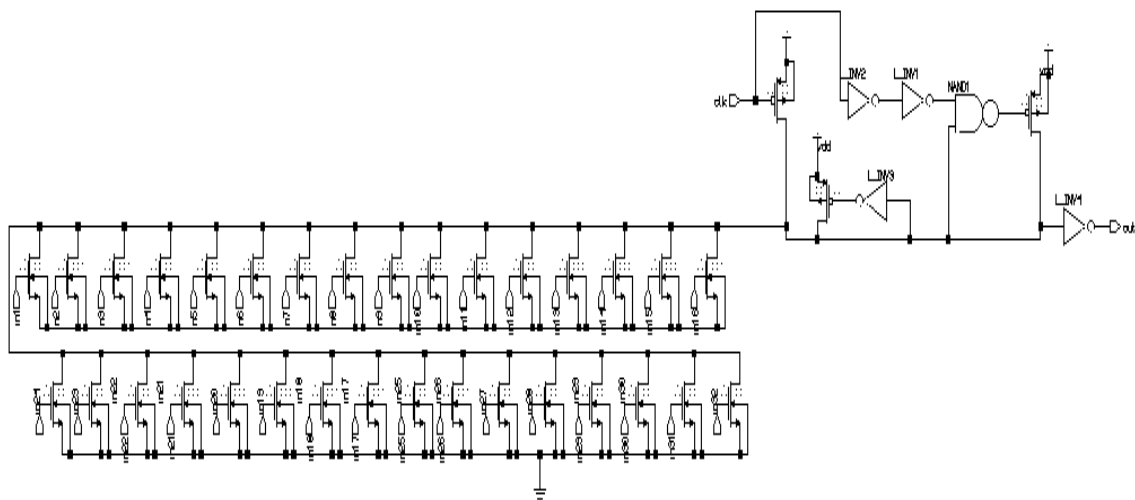

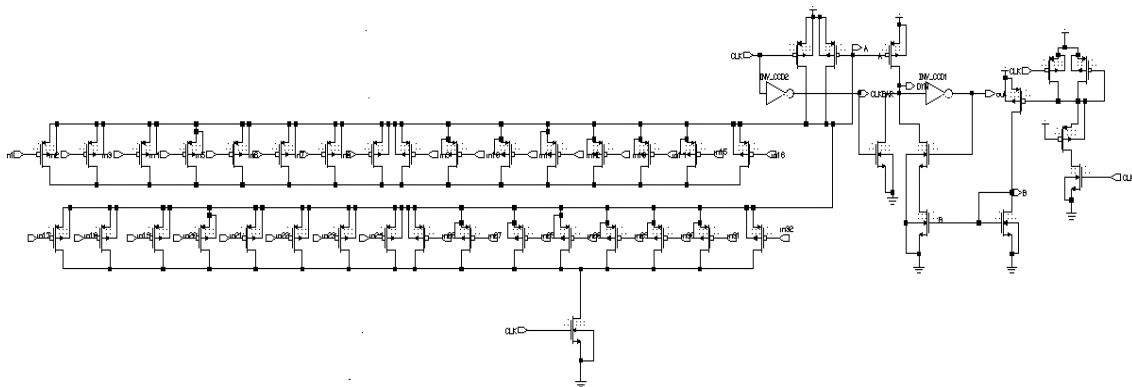Fig.3: Schematic of Conditional Keeper Domino logic for wide fan in gates

Fig.4: Schematic of Current Comparison Domino (CCD) logic for wide fan-in OR gate
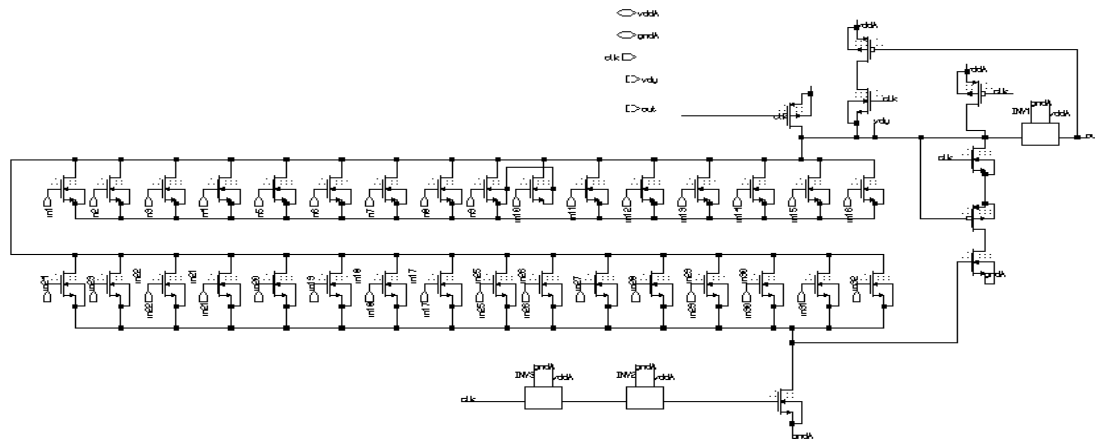
Fig.5: Schematic of Proposed Domino logic for wide fan-in OR gate

III. Proposed Domino Circuit

In this modified domino logic technique is introduced the corresponding schematic implementation along with its simulation results are shown in Fig.6 and Fig.7.

The Proposed circuit can be divided to two stages. The first stage is pre-evaluation stage and second is domino stage. The pre-evaluation network includes the pull up network and transistors $M_{PRE,}$ M_{EVAL} and M_1. The pull up network implements the desired logic is disconnected from dynamic node (DYN), unlike traditional dynamic logic circuits indirectly changes the dynamic voltage. The second stage has one input without any charge sharing, one transistor M_2 regardless of the implemented OR logic in the pull up network and a keeper which has a transistor M_K. Hence only one pull up transistor is connected to the dynamic node instead of connecting all transistors in the OR to reduce capacitance on the dynamic node. Input of footed transistor M_{EVAL} is connected to clock (CLK) and three inverters for generation of delay in the footed transistor. The delay element is used for slower the gate and greater noise robustness. These approaches do not reduce the overall leakage current, but only the leakage current at the dynamic node that drives the final static inverter and is the critical node. Hence we have more degree of freedom for increasing speed or enhance noise immunity by reducing the leakage current.

PRE-DISCHARGED PHASE: In Pre-Discharged phase, clock voltage is in low level i.e. CLK = "0", and the input signals are in high level. In pre-discharge phase (CLK = "0") the PMOS transistor is in ON state and charge the dynamic node from V_{DD}.

EVALUATION PHASE: In Evaluation Phase, the clock voltage is in the high level CLK = "1" and input signals can be in the low level. During evaluation phase (CLK = 1), a dynamic node doesn't able to maintain the constant because PMOS transistor is rail on OFF state from V_{DD}, only the keeper Transistor M_K connected to V_{DD} and it maintains the charge of dynamic node, if all the transistor is OFF in evaluation network. During evaluation phase when any one input is in ON state of the NMOS block and the dynamic node will discharge, which result in gate oxide leakage current and flow of sub-threshold which result in degradation of UNG of the circuit, for reduction of leakage current and enhance the noise immunity of the circuit of a proposed circuit.

In proposed circuit modification is done in evaluation network, we have inserted two NMOS transistors between dynamic node and pull down network. To improve the efficiency of the proposed circuit and extra NMOS transistor is connected to the dynamic node to produce the proper stacking of the evaluation network, to increase the noise immunity of the circuit and reduces the leakage current of the circuit by providing half swing logic at the output node. In footed portion we place NMOS transistor, during pre-charge phase footed transistor is OFF, during evaluation phase a charge discharge from dynamic node the two NMOS transistors provides the stacking effect for leakage reduction and high noise immunity. By using this type domino logic the circuit will be simple and the power consumption will be decreases, compare to the previous technique the delay and power is also decreases. The below wave form represents the 8 input OR logic by using proposed Domino logic with pre-charge and evaluation stages.

IV. Simulation Results

The proposed circuit was simulated by using MENTOR GRAPHICS EDITOR TOOLS in the high performance of 130nm technology at the temperature of 27˚C and 110˚C. The supply voltage is 1V for 8, 16, 32 and 64 input OR gates. Various parameters are considered such as power dissipation, delay transistor count and area. The circuit is operated at the operating frequency of 1GHz.

Table 1: Size of all transistors of proposed circuit for 8, 16, 32, and 64 bit OR gate

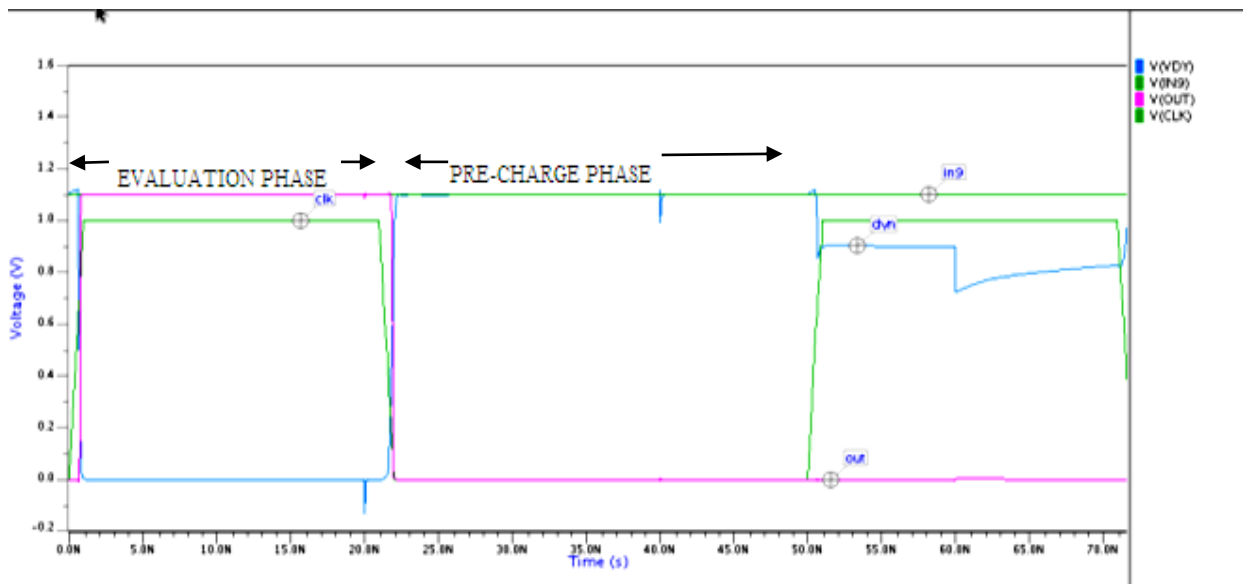| FAN-IN	W_{K1}	W_{K2}	(Wp/Wn) Inverter	W_{PRE}	W_{EVAL}	W_1	W_2	W_4	W_5	W_6	W_7
8	7Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin
16	8Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin
32	8Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin
64	8Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin

Fig.6: Simulated output waveform of proposed logic
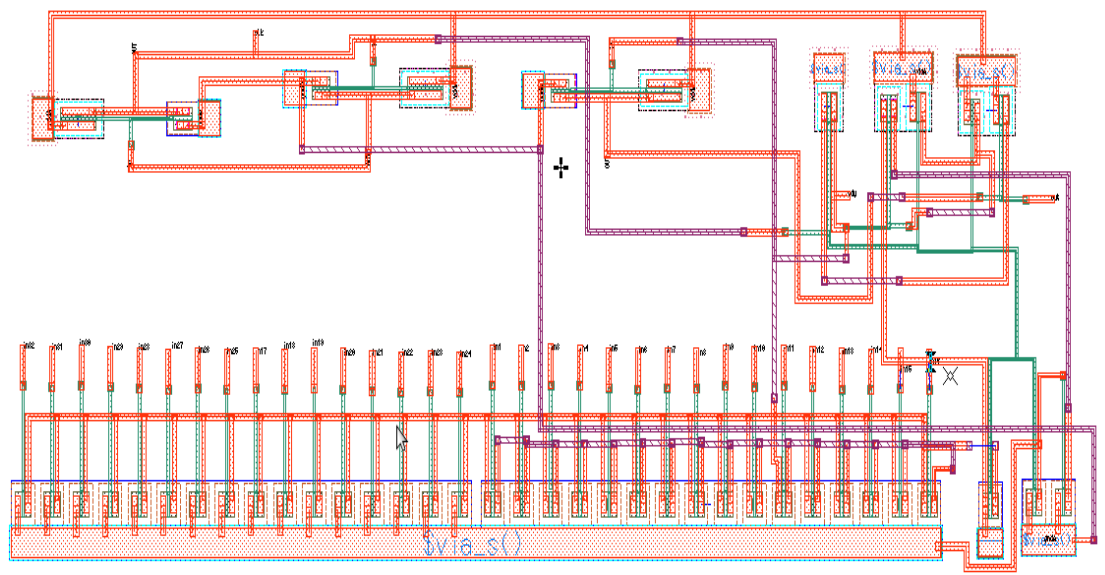
Fig.7: Layout design of 32 input OR logic using proposed domino circuit

Table 2: Comparison of delay normalized to HSD under same delay

FAN-IN		HSD		LCR		CKD		CCD		PROPOSED	
Temperature(˚C)		110	27	110	27	110	27	110	27	110	27
8	delay (ns)	21.445	21.430	21.357	21.317	0.00466	20.606	28.873	21.387	48.875	49.829
	Nor. Delay	1	1	0.961	0.994	0.00022	0.961	0.997	0.997	2.32	2.32
16	delay (ns)	21.310	21.390	21.292	21.354	21.298	20.509	28.420	21.298	49.800	49.807
	Nor. Delay	1	1	0.958	0.998	0.996	0.958	0.995	0.995	2.32	2.32
32	delay (ns)	31.277	31.362	21.008	31.278	31.281	20.490	20.630	21.110	49.711	49.760
	Nor. Delay	1	1	0.653	0.997	0.997	0.653	0.672	0.672	1.58	1.58
64	delay (ns)	529.81	31.16	0.00529	20.471	20.470	20.460	20.483	0.0046	49.598	49.85
	Nor. Delay	1	1	0.656	0.656	0.656	0.656	0.00015	0.0001	1.59	1.59

Table 3: Comparison of power consumption normalized to HSD under same power dissipation

FAN-IN		HSD		LCR		CKD		CCD		PROPOSED	
Temperature (˚C)		110	27	110	27	110	27	110	27	110	27
8	Power Dissipation (μw)	115.64	267.84	63.75	64.24	63.77	64.24	0.04412	0.00310	0.0028	0.0028
	Nor. Power Dissipation	1	1	0.55	0.24	0.55	0.23	0.00038	0.00001	0.00001	0.00001
16	Power Dissipation (μw)	118.08	268.43	64.91	64.37	64.37	64.35	0.03196	0.00310	0.0024	0.0024
	Nor. Power Dissipation	1	1	0.55	0.24	0.54	0.24	0.00027	0.00001	0.00001	0.00001
32	Power Dissipation (μw)	114.13	268.17	64.94	64.39	63.89	64.35	0.04397	0.00301	0.0029	0.0029
	Nor. Power Dissipation	1	1	0.57	0.24	0.56	0.24	0.00038	0.00001	0.00001	0.00001
64	Power Dissipation (μw)	117.38	268.45	63.96	64.41	63.95	64.39	0.04369	0.00309	10.22	10.22
	Nor. Power Dissipation	1	1	0.54	0.24	0.54	0.24	0.00037	0.00001	0.034	0.034

Table 4: Comparison OF 8, 16, 32, 64 inputs OR gate area parameter in μm's

FAN-IN		HSD	LCR	CKD	CCD	PROPOSED
8	Area (μm)	34.52*14.25	23.85*13.21	35.12*14.54	45.95*20.69	28.25*11.51
	Nor. Area	1	0.64	1.03	1.93	0.66
16	Area (μm)	35.15*14.34	24.77*13.23	41.04*13.01	46.69*21.70	26.40*19.34
	Nor. Area	1	0.65	1.06	2.1	1.01
32	Area (μm)	37.85*20.605	38.86*15.88	51.25*19.15	62.96*20.20	41.4*19.65
	Nor. Area	1	0.79	1.25	1.63	1.04
64	Area (μm)	69.51*25.24	63.52*24.65	75.21*24.58	78.65*25.58	65.15*24.65
	Nor. Area	1	0.89	1.05	1.15	0.92

Table 5: Parameter Comparison for 27˚C with 1V supply voltage

FAN-IN	PARAMETERS	HSD	CKD	CCD	LCR	PROPOSED
8	Power Dissipation	267.8464uw	64.2474uw	3.1044nw	64.2446uw	2.8956nw
	Delay	21.430ns	467.66ps	20.606ns	21.387ns	49.829ns
	Transistors	20	19	25	15	21
16	Power Dissipation	268.4374uw	64.3500uw	3.1044nw	64.3769uw	2.4824nw
	Delay	21.390ns	21.317ns	20.509ns	21.298ns	49.807ns
	Transistors	28	27	33	23	29
32	Power Dissipation	268.1217uw	64.3500uw	3.0156nw	64.3976uw	2.8956nw
	Delay	31.362ns	31.278ns	20.490ns	21.110ns	49.760ns
	Transistors	44	43	49	39	45
64	Power Dissipation	268.4296uw	64.3999uw	3.0907nw	64.4141uw	10.2248uw
	Delay	516.40ps	20.471ns	20.460ns	460.85ps	49.585ns
	Transistors	76	75	81	71	77

Table 6: Parameter comparison for 110˚C with 1V supply voltage

| FAN-IN	PARAMETERS	HSD	CKD	LCR	CCD	PROPOSED
8	Power Dissipation	115.6405μw	63.7724μw	63.7504μw	44.1245nw	1.8956nw
	Delay	21.445ns	466.3ps	21.357ns	28.873ns	48.875ns
	Transistors	20	19	15	25	21
16	Power Dissipation	118.0876μw	64.3769μw	64.9166μw	31.9643nw	1.4824nw
	Delay	21.310ns	21.298ns	21.292ns	28.420ns	49.800ns
	Transistors	28	27	23	33	29
32	Power Dissipation	114.1368μw	63.8979μw	64.9422μw	43.9752nw	1.8956nw
	Delay	31.277ns	31.281ns	21.008ns	20.630ns	49.711ns
	Transistors	44	43	39	49	45
64	Power Dissipation	117.3866μw	63.9592μw	63.9628μw	43.6931nw	9.2248μw
	Delay	595.81ps	20.470ns	529.75ps	20.483ns	49.598ns
	Transistors	76	75	71	81	77
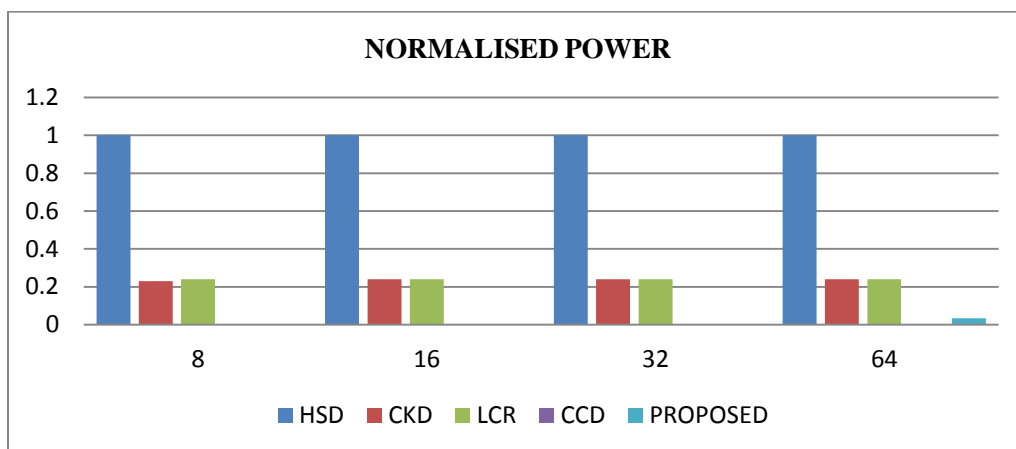
Fig.8: Normalized Power Dissipation for 8,16,32,64 Fan-in's
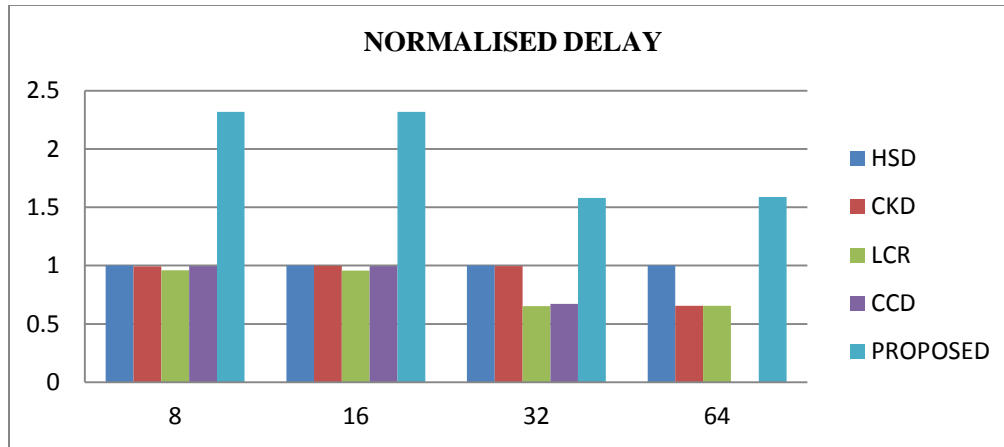
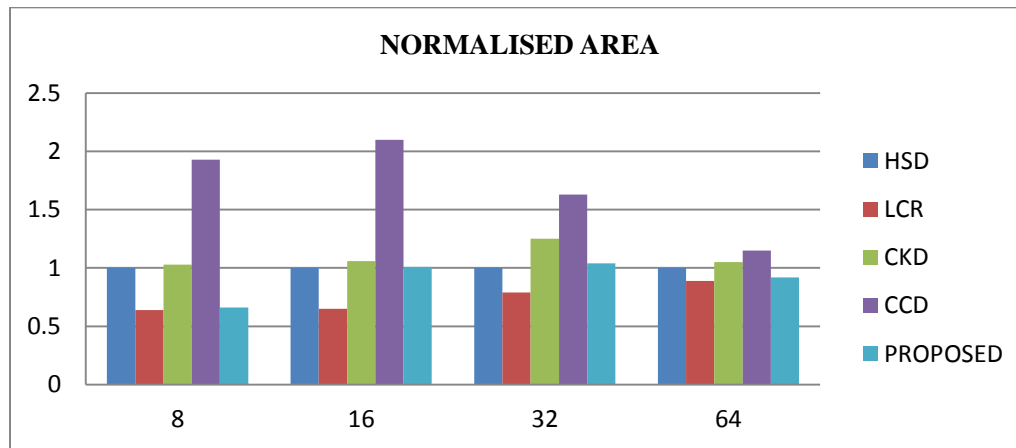Fig.9: Normalized delay for 8,16,32,64 Fan-in's

Fig.10: Normalized Area for 8,16,32,64 Fan-in's

The effect of CMOS technology scaling on the proposed circuit and HSD circuit is examined using a technology model for the 130-nm node in typical process at the 1V power supply. The power consumption and delay of the proposed circuit are normalized to HSD are plotted in Fig. 9, Fig.10 and Fig.11. As shown in this figure, the normalized power dissipation which is lower than previous techniques i.e., HSD, LCR, CKD and CCD domino techniques.

V. Conclusion

Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. In this thesis, introduction of domino logic, background and previous techniques of domino logic and corresponding Domino logic techniques have been designed & simulated. Simulations have been carried out using 130nm Mentor Graphics ELDO simulator to evaluate the new design of 8, 16, 32, 64 fan-in OR domino logic circuit. A wide comparison made for the designs described in the literature and a significant improvement in terms of Delay, Total power dissipation and area parameter are illustrated. This circuit has small area, low power and low device count circuits for wide fan-in gates. The proposed circuit gives power improvement by proposed circuit for 32 input OR gate is 91.148% than HSD, 84.019% than CKD, 84.021% than LCR and 97.368% better power dissipation than CCD similarly improvement of area for proposed 64 fan-in OR gate is 8.724% than HSD, 13.129% than LCR, 20.176% than CCD.

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