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Analytical and Comparative Study Of Quantum Dot Cellular Automata Technology Based 2:4 Decoder Circuits

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Abstract : *Quantum dot cellular Automata technology is used in this paper which overcomes the design constraints of nanoscale CMOS circuits. This paper presents the analysis of 2:4 decoder circuit using four different methodologies. QCA based Decoder circuit is implemented using coupled majority voter minority gate, 45^0 rotated cells, multilayer wire crossings and five input Majority Voter gate. Comparative study of these four decoder shows that performance of Coupled majority voter minority gate based 2:4 decoder is good in terms of area, latency and complexity. QCADesigner 2.0.3 tool is used for the implementation of QCA based Decoder circuits.*

Keywords: *Coupled majority voter minority gate, Decoder, Multilayer wire crossings, Quantum Dot Cellular Automata.*

I. Introduction

Moore's law says that, the number of transistors on a unit area doubles every 24 months [1]. The International Technology Roadmap for semiconductors (ITRS) projects that the scaling of the CMOS technology will continue till 2019 [2]. Technology that may replace CMOS when the scaling limit is reached is Quantum Dot Cellular Automata (QCA). QCA technology is built up in cells. Each cell has two electron and 4-5 islands. However due to coulomb repulsion they will always settle down to one of the two stable states which can be labeled as logic '0' and logic '1'as shown in fig.1 . These are known as binary states. When the cells are placed beside each other, because of Coulombic interaction, the adjacent cell will also try to settle to the same logic as that of the first cell. Using these four dot cells binary wire can be obtained, just by placing the cells adjacent to each other.

The advantage of the QCA circuits is that it doesn't need the power to run the circuit; instead QCA clock will be responsible to trigger the circuit and run it. QCA clock has four phases[11][12] i.e. switch, hold, release, relax [3] as shown in fig.2

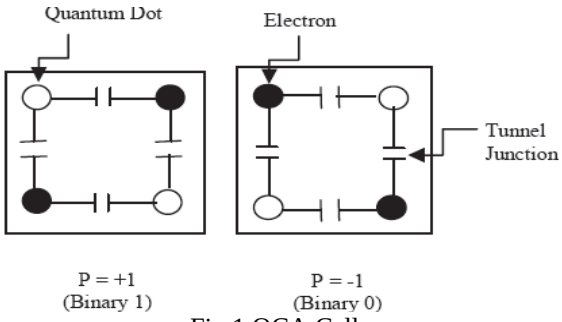


Fig.1 QCA Cell

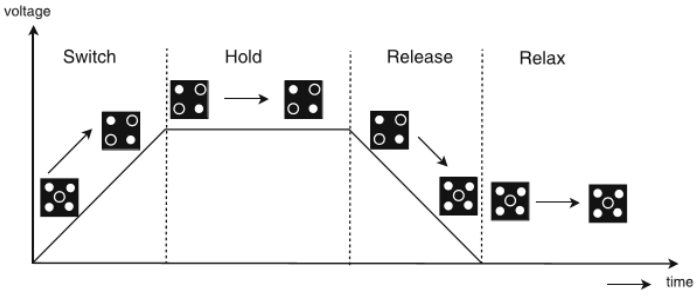
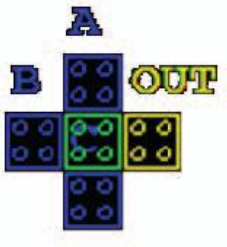
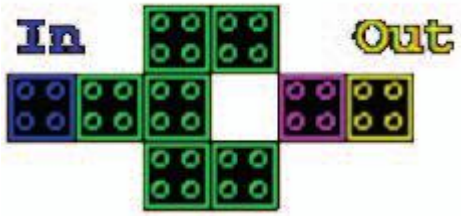


Fig. 2 QCA Clock Zones

For the implementation of any QCA circuits basic QCA gates are required. Majority Voter (MV) and Inverter are the basic QCA gates using which any circuit can be implemented. QCA MV gate and Inverters are shown in Fig. 3 and Fig. 4 respectively.





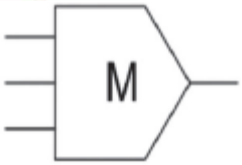


Fig. 3 QCA Majority Voter Gate

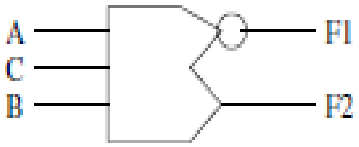
Fig. 4 QCA NOT Gate

II. Methodology

In this paper QCA base 2:4 decoder is implemented with the help of different methodologies.

2.1 Coupled Majority Voter Minority Gate

One of the advantages of CMVMIN gate is that, the number of wire crossings in the circuit can be reduced as well as the number of clock cycles required for the implementation of any QCA based logic circuit will be reduced [13][14]. CMVMIN has 3 inputs i.e. A,B,C and two outputs F1 and F2. Outputs F1 and F2 are complement of each other as shown in Fig. 5.



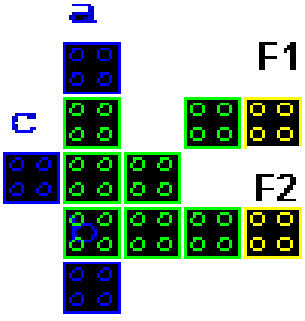
$$F1 = AB + AC + BC$$
$$F2 = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$

Fig. 5 Symbolic representation of CMVMIN Gate and its Equations

Truth table of CMVMIN gate [10]is shown in Table 1. Here output F1 will be 1 when majority of zeros are there in the input. Similarly output F2 will be 1 when majority of the inputs are 1.

Table 1: Truth Table of CMVMIN Gate

A	B	C	F1	F2
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1



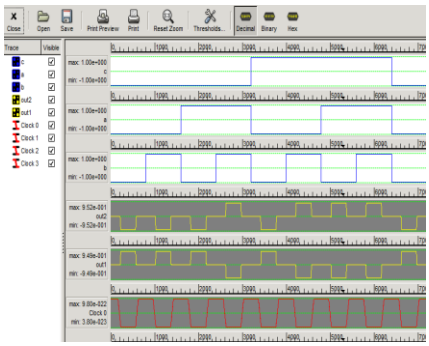


Fig. 6 Layout and Simulation Result of CMVLMIN Gate

2.2 45^0 rotated QCA Wires:

QCA wire is made up from the number of QCA cells connected in series. When the cells in QCA cells are oriented by 45^0 and if these 45^0 rotated cells are placed adjacent to each other, it forms a wire. The advantage of this type of wire is that we will get the true and complement value at the output. If odd number of rotated cells are connected in the wire, it provides the output same as that of input, similarly when even number of rotated cells are connected the wire, it provides the output which is complement of the input. The concept of 45^0 rotated cells is illustrated in Fig. 7 and Fig. 8.

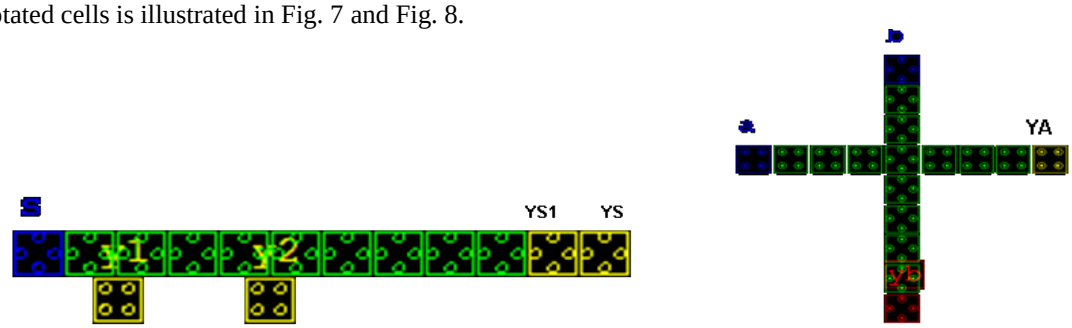


Fig. 7 45^0 QCA wire and wire overlapping

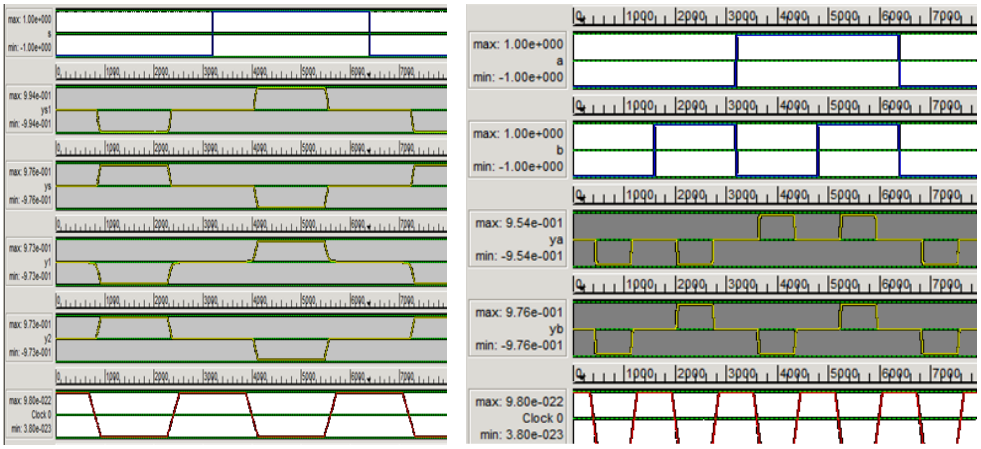


Fig. 8 Simulation Result of QCA Wire

2.3 Multilayer Wire Crossings:

Multilayer wire crossings make use of three components i.e. main layer, via layer and crossover layer. Example of multilayer wire crossing is shown in Fig.9 where input A is passed to the output as AOUT and input B is passed to the output side as BOUT. These vertical wire and horizontal wire are not affecting each other.

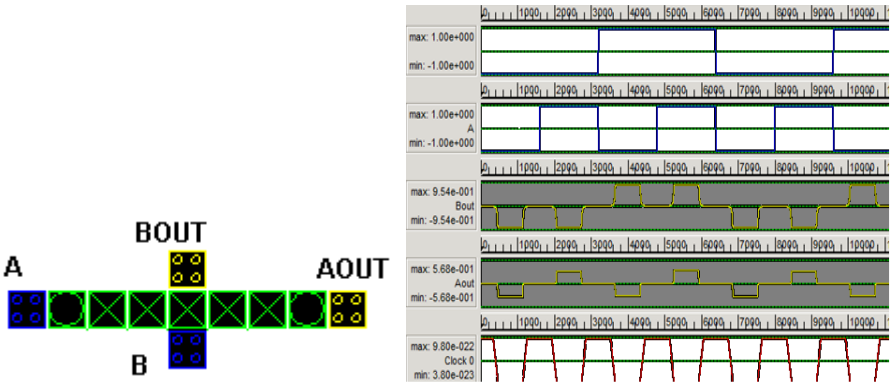


Fig. 9 Layout and simulation result of Multilayer wire crossing

2.4 Five Input Majority Voter Gate

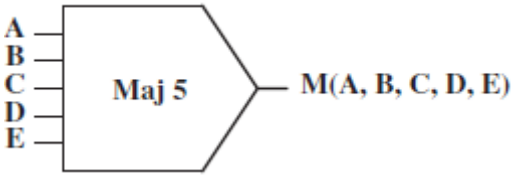


Fig.10 Symbolic representation of 5 input MV gate

Five input MV gate has 5 inputs and one output as shown in Fig. 10. Output will be '1' when majority of the inputs are 1. Polarization of input cells is fixed and that of middle cells as well as of output cell can be changed. Layout and simulation result of 5 input MV gate is shown in Fig. 11.

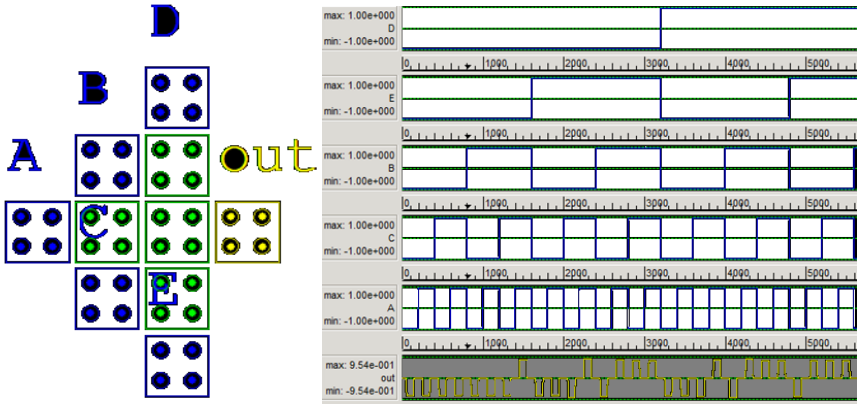


Fig.9 Layout and simulation result of 5 input MV gate

III. QCA Based 2:4 Decoder Circuit

As mentioned in section II, four different methodologies are used for the implementation of 2:4 decoder circuits. Here in Fig. 10 n = 2 and m = 4.

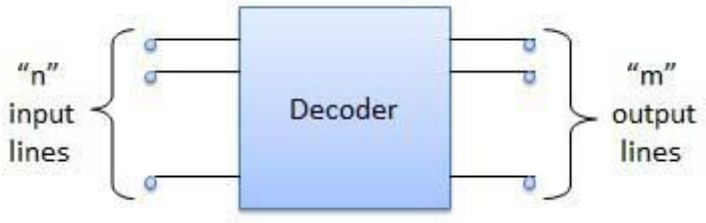


Fig. 10 Block Diagram of 2:4 Decoder

IV. Results

4.1 QCA based 2:4 Decoder using CMVMIN Gate [5]

QCA based 2:4 decoder circuit is shown in Fig. 11. For the implementation of circuit CMVMIN, MV and Not gates are required.

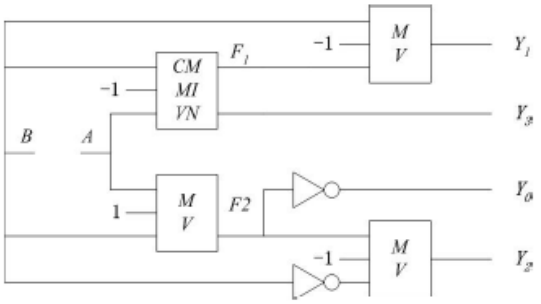


Fig. 11 Logical Diagram of QCA based 2:4 Decoder using CMVMIN Gate[5]

Equations of four outputs of decoder i.e. Y_0, Y_1, Y_2, Y_3 are shown below

$$Y0 = MV(A,B,1) = \overline{A+B} = \bar{A}\bar{B}$$

$$Y1 = MV\big(MV(A,B,0),0,B\big) = (\bar{A}+\bar{B})B = \bar{A}B$$

$$Y2 = MV(MV(A,B,1),\bar{B},0) = (A+B)\bar{B} = A\bar{B}$$

$$Y3 = MV(A,B,0) = AB$$

Implementation of QCA based 2:4 Decoder using CMVMIN Gate is shown in Fig. 12. Only 3 Majority Voter gates, 1 Coupled majority voter minority gate and 2 not gates are required for the implementation of circuit.

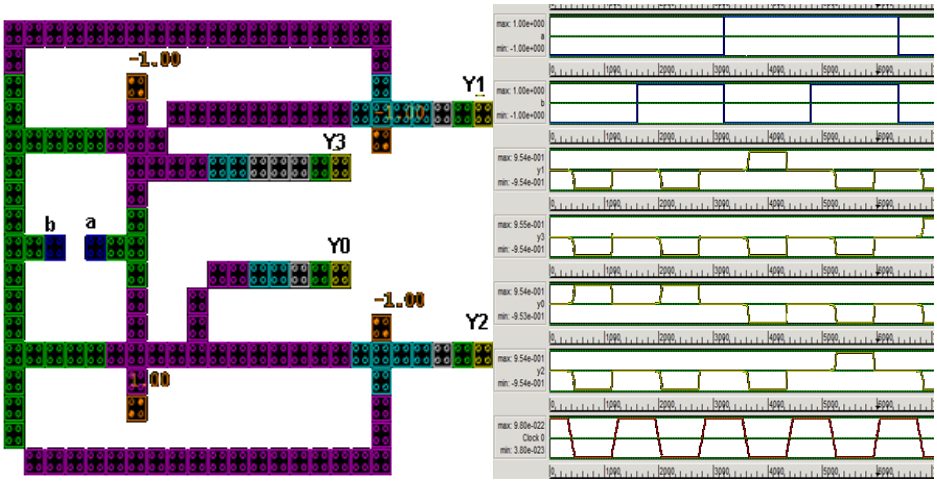


Fig. 12 Layout and Simulation of QCA based 2:4 Decoder using CMVMIN Gate

4.2 QCA based 2:4 Decoder using 45^0 rotated cells [6]:

For the implementation of QCA based 2:4 decoder circuit using 45^0 rotated cells only 4 Majority voter gates and 4 Not gates are required [6]. Implementation and simulation result of QCA based decoder circuit using 45^0 rotated cells is shown in Fig. 13

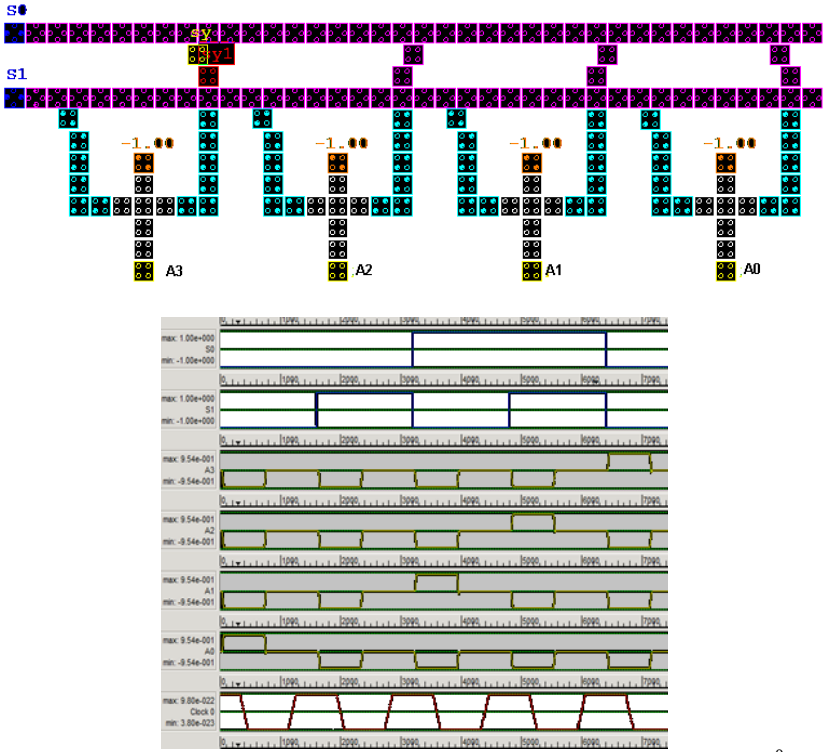


Fig. 13 Layout and Simulation Result of QCA based 2:4 decoder circuit using 45^0 rotated cells

4.3 QCA based 2:4 Decoder using Multilayer Wire Crossings [Traditional Method]:

For the implementation of QCA based 2:4 Decoder using Multilayer Wire Crossings total 8 QCA gates are required i.e. 4 MV gates and 4 NOT gates. Implementation and simulation result is shown in Fig. 14

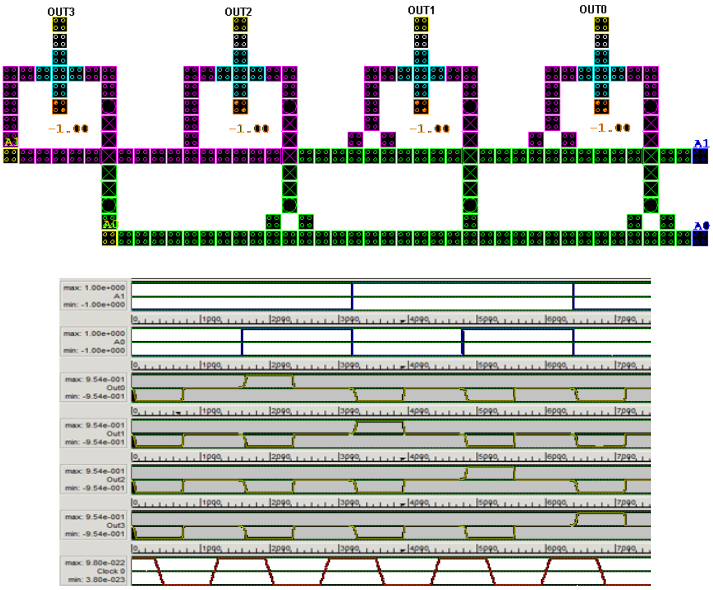


Fig. 14 Layout and Simulation result of QCA based 2:4 Decoder using Multilayer Wire Crossings [Traditional Method]

4.4. QCA based 2:4 Decoder using 5 input Majority Voter Gate[9]:

4 Five input Majority Voter gates and 2 NOT gates are required for the implementation of QCA based 2:4 Decoder using 5 input Majority Voter Gate[9]. Logical diagram of the circuit is shown Fig. 15.

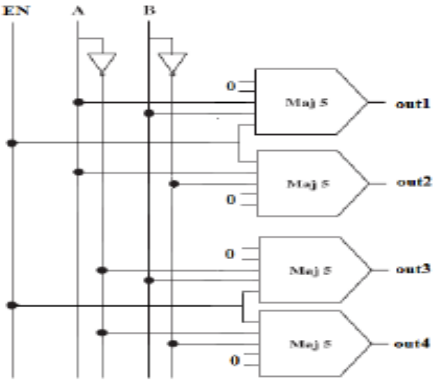


Fig. 15 QCA based 2:4 Decoder using 5 input Majority Voter Gate

Total 6 gates are required for the implementation of circuit i.e. 4 five input MV and 2 NOT gates. Implementation and Simulation Result of QCA based 2:4 Decoder using 5 input Majority Voter Gate is shown in Fig. 16

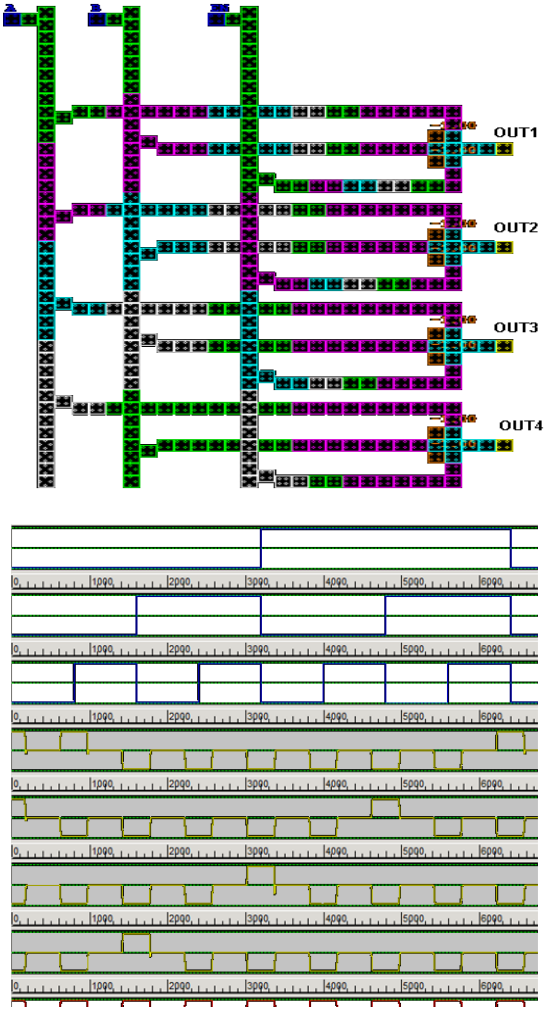
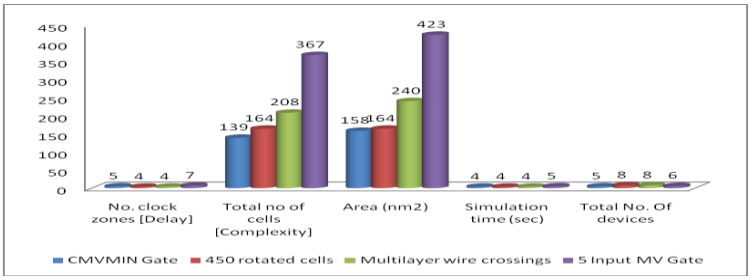


Fig. 16 QCA based 2:4 Decoder using 5 input Majority Voter Gate [9]

V. Comparative Study

Table 2 Comparison QCA based 2:4 Decoder Circuits

QCA Technology	**CMVMIN Gate[5]**	**45^0 rotated cells [6]**	**Multilayer wire crossings [Traditional method]**	**5 Input MV Gate [9]**
No. clock zones [Delay]	5	4	4	7
Total no of cells [Complexity]	139	164	208	367
Area	0.33 µm X 0.48 µm = 158 nm^2	0.76 µm X 0.24 µm = 182 nm^2	0.86µm X 0.28µm = 240 nm^2	0.55µm X 0.77µm = 423 nm^2
Simulation time	4 Sec	4 sec	4 sec	5 Sec
Total No. Of devices	Total – 6 1 CMVMIN 3 MV and 2 Inverters	Total – 8 4 MV 4 NOT Gates	Total – 8 4 MV and 4 INV	Total – 6 4: five input MV 2: NOT Gates



VI. Conclusion

Comparative study and parametric analysis of QCA based 2:4 decoder circuit shows that the use of Coupled Majority Voter Minority gate method will provide the fast area efficient circuit as compared to that of other three methods. Complexity of 2:4 decoder circuit using CMVMIN gate is very less as it has only 139 QCA cell count. This circuit is 17% less complex as compared to others. Latency of 2:4 decoder circuit using CMVMIN gate is 5 clock zones, that means it requires one clock zone extra as compared to the decoder circuit using 45^0 rotated cell but it requires two clock zones less when compared to last two methods as shown in Tale 2. Total number of devices required for the implementation of 2:4 decoder using CMVMIN gate is only 5 which is 6 and 8 in other three methods. Hence 2:4 decoder circuit using CMVMIN gate is proved to be efficient in terms of area, speed, complexity and latency, when compared to other three methods. Here it is concluded that CMVMIN gate is used to reduce the number of wire crossings as well as the number of clock cycles required to operate the QCA circuit.

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