Comparative Analysis of Quaternary SETMOS Multiplexer

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 Abstract: *This paper introduces the comparative analysis of binary logic with quaternary logic.As quaternary logic build the circuits which are more compact and simple as compared with binary logic .For This two devices are used the first one is PMOS and other one is N-Type single electron transistor(NSET).For Comparative analysis basic hybrid SETMOS Quaternary logic gates as well binary SETMOS Quaternary logic gates are desined and simulated.Similarly three different multiplxers are designed and simulated .Comparison is done with the help of power dissipation.*
Keywords: *single electron transistor,mosfet,quaternary,binary power dissipation.*

I.   Introduction

Many of these devices are capable of dealing with more than two logic states, so their efficiency could be utilized if we use multi-valued logic for digital circuits. Some multi-valued logic systems such as ternary and quaternary logic schemes have been developed and they have been being experimented for a long time .These logic systems are derived as propositional or quantum logic [1], [2]. Quaternary logic has several advantages over binary logic. Since it requires half the number of digits to store any information than its binary equivalent, it is good for storage; given that the quaternary storage mechanism is less than twice as complex as the binary system. For the same reason, quaternary devices require simpler parallel circuits to process same amount of data than that needed in binary logic devices[9].

Binary & Quaternary Logic

This paper discussed about binary and quaternary logic for the implementation of multiplexer. Multiplexers are important part in designing of selective circuits as well as for the design of full adders. As the interconnections gets reduced in quaternary logic as compared to binary logic hence can be used where more complicated applications need to design.Three different quaternary multiplexers are designed and discussed in the following sections.
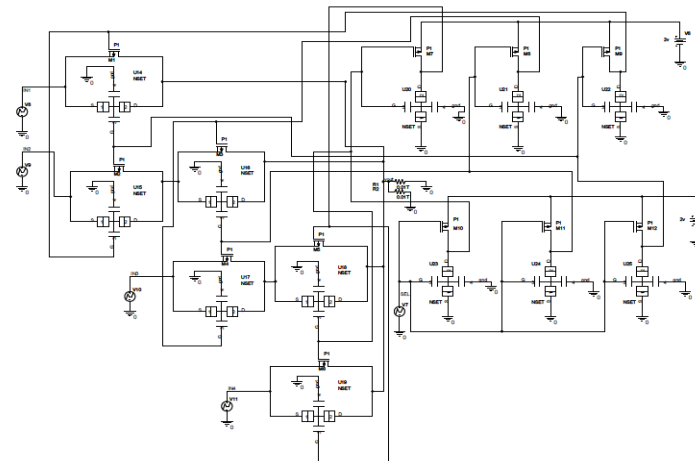
II.   Quaternary Multiplexer

In this section type I quaternary logic is implemented.This multiplexer is designed with use of transmission gates and inverters.Then type II inverter is implemented with use of threshold logic.And finally type III quaternary multiplexer is imented with use of MIN & MAX gate.
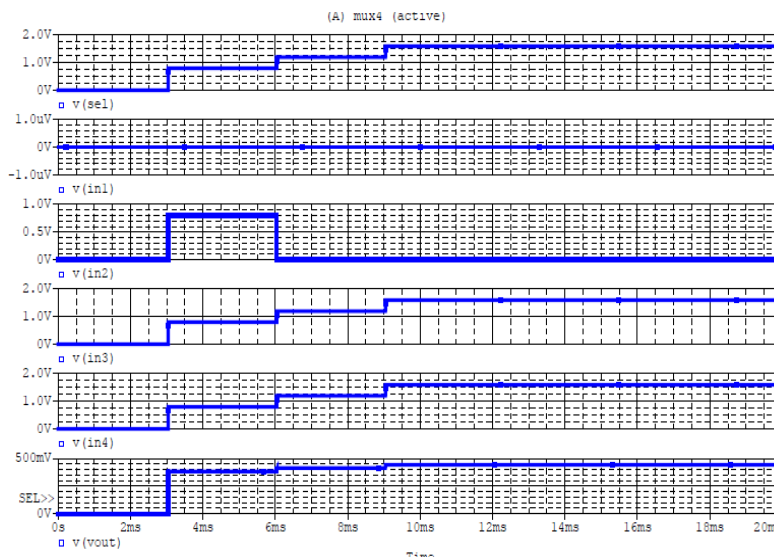
2.1 Quaternary Multiplexer Type I

Fig.1 shows the circuit diagram of 4:1 multiplexer in which only one select line is required as compare to binary logic where four select line are required. In this design two different devices are used one is single electron transistor and other is mosfet.One PMOS and one N-type single electron transistor (NSET) is to create one transmission gate.This type transmission gates are used for the the design of selective circuit.Hence total six transmission gates are used in this complete design.And remaining inverters are used.
Fig.2 shows the input and output waveforms of quaternary multiplexer. In which four inputs ,one select line and one output waveform is shown in fig .2.
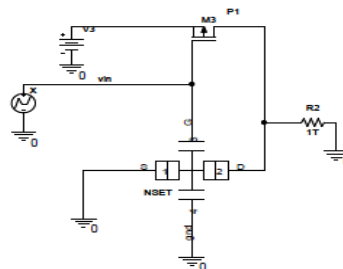
Fig.1 Type I Quaternary SETMOS Multiplexer

Fig.2 Input & Output Waveform of Quaternary SETMOS Waveforms
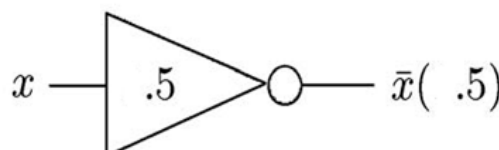
2.2 Quaternary Multiplexer Type II

Fig.3 shows the logical circuit diagram of threshold concept in which one PMOS and one NSET is used.If.input X is less than 0.5V then VDD will appear at the output. And if input X is greater than 0.5v then VSS will appear at the output

**Fig.3** Threshold logic using SETMOS

If X <0.5V THEN VOUT=VDD

If X >0.5V THEN VOUT=VSS

Fig.4 Symbol of SETMOS threshold Logic

**Four Logic Level Voltages Can Be Calculated As   VDD,VDD/3,2VDD/3,0 Threshold Voltage = VDD/6**

Fig.4 shows the symbol of SETMOS threshold logic.And four logic levels can be calculated as VDD,VDD/3,2VDD3,0.These are the levels are used throught all the designs of quaternary SETMOS multiplexer.
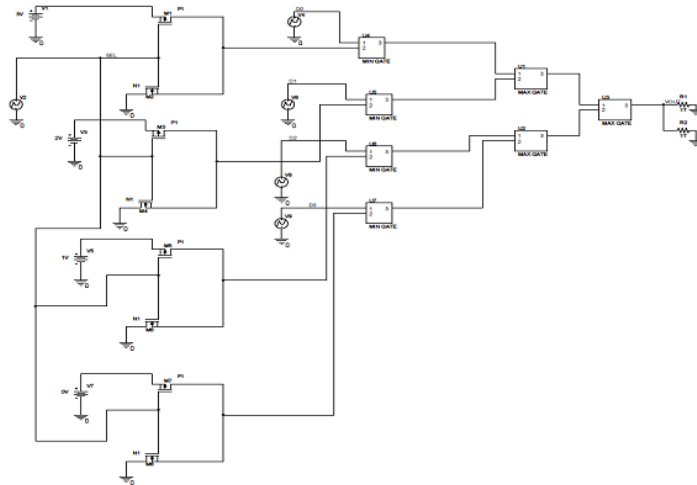
Fig.5 Type II Quaternary SETMOS Multiplexer

Fig.5 shows the circuit diagram of type II Quaternary SETMOS multiplexer in which for the design of selective circuits threshold logic design is used which is discussed in above section.

Four threshold logic circuits and four different inverters are are used for the design of quaternary SETMOS inverter which is shown in fig.5
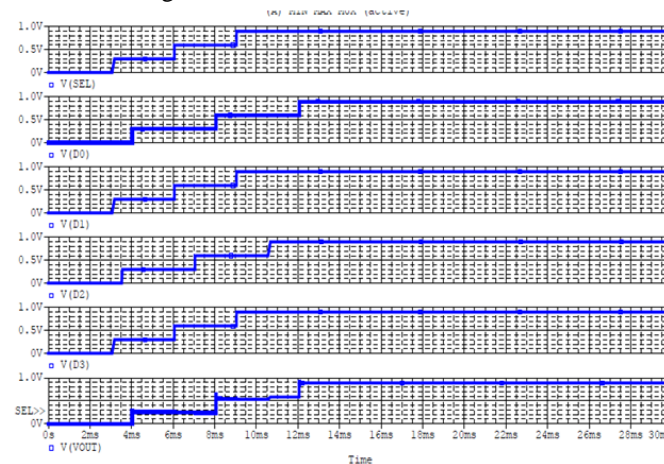
Fig.6 Input And Output Waveform Of Type II SETMOS Quaternary Multiplexer

2.3 Quaternary Multiplexer Type III

Fig.7 shows the circuit diagram of type III SETMOS Quaternary Multiplexer in which hybrid inverters and MIN and MAX gates are used for the design of type III SETMOS quaternary multiplexer.In which circuit is compact and requires only one select line according to the logic of quaternary.

Fig.8 shows the input and output waveforms of type III SETMOS quaternary multiplexer.

In this way three different SETMOS quaternary multiplexers are designed and implanted whose input and output waveforms are also discussed and verified according to the required logic.Then power dissipation of each type SETMOS quaternary multiplexer is taken from simulation results.Then comparative analysis of each type SETMOS quaternary multiplexers are discussed in following sections.

As basic gates are the fundamental requirements of any application .So initially all the basic gates were designed and simulated and comparison of them in terms of power dissipation is also given in the following section.
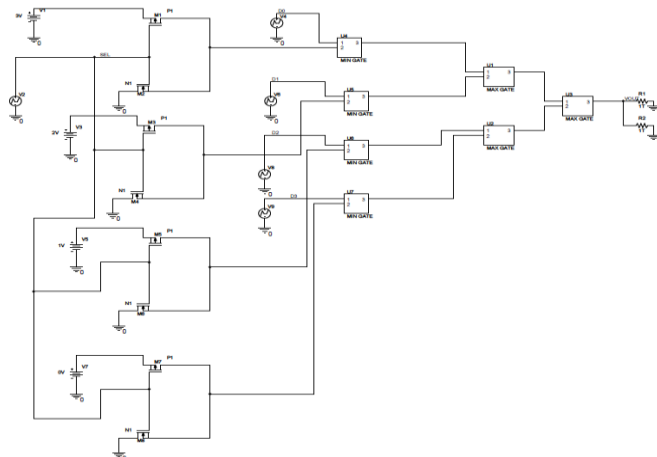
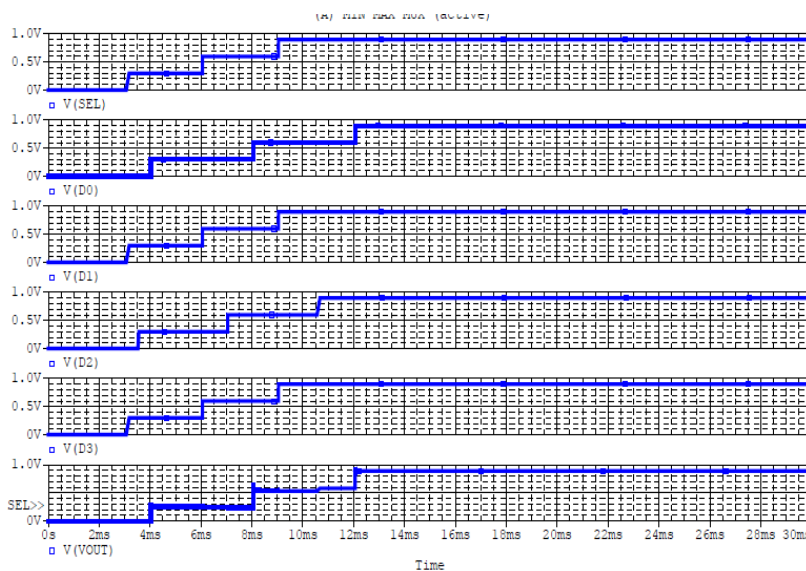**Fig.7** Type III SETMOS Quaternary Multiplexer

Fig.8 Input and Output Waveform of type III SETMOS Quaternary Multiplexer

III.   Comparative Analysis Of Multiplexer

Table I shows the comparative analysis of power dissipation for three different types of SETMOS Quaternary Logic Multiplexer.As well requirements of transistor s are also almost same for type I & II multiplexer.Where as for the type III multiplxer more transistors are required as compared with other two.

Table I Comparative Analysis Of three SETMOS Quaternary Multiplexer In terms Of Power Dissipation

Sr.No.	Type Of Multiplexer	Power Dissipation(μW)
1	TYPE I	51.9
2	TYPE II	33.4
3	TYPE III	40

Table II Comparative Analysis Of Basic Quaternary SETMOS Gates In terms Of Power Dissipation

Name Of The Circuit		Hybrid Binary Gate	Hybrid Quaternary Gate
Power Disipation(μW)	NOR	12	11.9
	MIN	5.9	0
	MAX	5.9	0
	XOR	10.87	8.96
	MV	18	0

Table II shows the comparative analysis of fundamental basic SETMOS Quaternary gates in terms of power dissipation.In which MIN,MAX,XOR and MV gtaes are discussed.In this table binary as well quaternary gates are compared in terms of power dissipation.

IV. Conclusion

As today's requirements are more compact low power circuits which can be fulfilled with help of quaternary logic is discussed. Initially all the basic gates which are required for any design are discussed and simulated in terms of binary as well as quaternary logic. Then three different SETMOS Quaternary Multiplexers are designed and simulated .Comparative analysis shows quaternary circuits are more compact and requires low power.

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