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High Performance Design Analysis of DG MOSFET Using High Dielectric Permittivity

Rajesh Kumar[1], Rajesh Mehra[2]
[1]*(ECE, NITTTR Chandigarh, India)*
[2]*(ECE, NITTTR Chandigarh, India)*

Abstract: *The Evolution of Silicon Technology in the Semiconductor Industry is Prevalent . However, as the technology is scaled down to nanometer regime, there is susequent degradation in MOSFET Characteristics. In this Paper, Comparative Analysis of Proposed DG MOSFET device with previous Model was done using High-k Dielectric material and conventional Bulk* SiO_2 *to investigate the various performance characteristics like Threshold Voltage, DIBL, Sub-threshold Voltage and Leakage (OFF) current using COGENDA VTCAD Simulator. We have observed that the Proposed DG MOSFET model is quite effective in reducing Sub-threshold Slope(SS) , Leakage current and obtaining optimum value of DIBL. It is observed that using proposed model there is significant reduction in Leakage current about 100% in HfO2 and 94% in ZrO2 with* L_G*= 25nm as compared to previous model . In case of* L_G*= 13nm, there is 16% and 23% reduction in leakage current is achieved. Also ,Sub-threshold slope reduces by almost 14% with respect to all gate eletrodes as compared to previous model.*

Keywords: *Dielectric, High-k, MOSFET, Scaling, SCEs, Leakage, DIBL, SS*

I. Introduction

CMOS Technologies have been advancing faster day by day. With the Passage of time, the requirement for faster, cheap and low power devices is becoming the important factors for achieving high efficiency. Another important factor is cost of IC Manufacturing [1]. The rapid decrease in price of ICs has activated new applications and semiconductor devices. The most important factor that speeds up the era of electronics is "miniaturization". By decreasing the size of transistors and interconnects, more circuits can be fabricated on small silicon wafer. So, circuit becomes cheaper. Miniaturization plays an important role in the improvement of speed and power consumption. Reducing the length of channel has many serious side-effects [2] .Such as subsequent decrease in threshold voltage, increase in speed, size reduction, decrease in capacitive effect and low power dissipation as well. Different technology generations are 180nm, 90nm, 60nm, 45nm 32nm and further reduction in gate length .Scaling which is usually recommended to achieve better device performance and very high integration density [3]. But however, the major drawback about development of silicon technology is side-effects of continuous reduction of dimensions of devices. Due to decrease in channel length, leakage current and short channel effects (SCEs) becomes a vital factor that continuously degrades the performance of device [4].

II. Short Channel Effects

To enhance device performance and speed, Scaling have been focused to a larger extent in MOSFET. However as the channel shrinks [5] ,the controllability of the gate over the channel depletion region reduces to a greater effect due to the increased charge sharing from corresponding source and drain depletion regions. SCEs gave rise to several serious problems including the dependence of threshold voltage over channel length . The main drawback of SCEs is Leakage current and decrease in threshold voltage. However, SCEs also degrades the controllability of gate voltage over drain current which in turn affects the sub-threshold Slope contributing the drain leakage current. This particular degradation has been demonstrated as charge sharing by the gate and drain electric fields in the channel depletion layer in Poon and Yau's Model [6] which is also known to be first SCE model. There are various SCEs in MOSFETs. In this paper, following SCEs has been discussed and analyzed:

1.1 Theshold Voltage

The Drain to Source current in the MOSFET can be defind as given in equation (1) for $V_{GS}<V_{th}$. The equation clearly depicts the dependence of drain or leakage current [7] on V_{th} and η .

$$I_{DS}=100\,(\frac{W}{L})e^{q(V_{GS}-V_{th})/\eta KT} \tag{1}$$

Where V_{GS}= Gate to Source Voltage, V_{th}=Threshold Voltage, I_{DS}=Drain to source Leakage current, T=temperature, W=Width, L=length of Gate. To reduce Leakage current there are two ways: one is to increase

Threshold voltage and other is to operate transistor at lower temperature which is very rarely used as due to high cost of cooling. However threshold voltage is increased to some extent by increasing Work function as depicted by equation (2) given below for an n-channel MOSFET [8] :

$$V_{th} = \varphi_{MS} - \frac{Q_{SS}}{C_{OX}} + 2\varphi_F + \frac{qN_a X_{d\max}}{C_{ox}} \tag{2}$$

Where φ_{MS} is the work function difference between the gate and the channel , Q_{ss} is the surface state charge of the channel, Cox is the gate capacitance and equal to $\frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}}$, here t_{ox} is the gate oxide thickness. φ_F is the Fermi potential, equal to $\frac{KT}{q}\ln\frac{(N_a)}{n_i}$, where N_a is the channel doping concentration, X_{dmax} is the maximum depletion width. Threshold Voltage can be found out by constant current method. In this method First of all We calculate the difference ΔV_T between the gate voltage V_{G1} and V_{G2} corresponding to two different drain voltage V_{d1} and V_{d2} for some constant current I_{DS} at the linear portion of the I_{DS}-V_{GS} Curve characteristics .

2.2 Drain Induced Barrier Lowering (DIBL)

In Case of long–channel MOSFETs gate has control over the channel and contributes for most of its charge. Also, For the weak inversion regime [9] there is presence of potential barrier between source and the channel region. The height of this barrier is indicates balance between drift and diffusion current between the two regions. However, the barrier height for carriers of channel should be controlled by the subsequent gate voltage to maximize ON Current. The DIBL effect came into existence when this barrier height decreases due to Short channel effect after the use of high drain voltage. This increase the quantity of carriers into the channel from the corresponding source thus consequently increase drain OFF current. So, the drain current is now not only controlled by the gate voltage but also by the drain voltage. This effect is usually known as charge sharing. Since, drain and source also takes part in charge region of the channel which would otherwise was only controlled by the gate. As with the increase in bias drain depletion region continues to rise so that it can actually make interaction with the source to channel junction which in turn decrease the potential barrier [10]. DIBL is usually given by equation:

$$\text{DIBL} = -\left[\frac{V_{th2} - V_{th1}}{V_{d2} - V_{d1}}\right] \tag{3}$$

Where (V_{th2})= saturated threshold voltage, (V_{th1})= linear threshold voltage, (V_{d2})=Drain voltage applied in saturation region, (V_{d1})= Drain voltage applied in linear region. Here, we have use (V_{d2}) = 0.75 V and (V_{d1}) =0.05 V.

2.3 *S*ub-threshold Slope

It usually defines the way that how effectively the drain current of a device can be stopped whenever V_{GS} is reduced below threshold voltage (V_{th}). It is usually present when some electrons are induced in the channel even before strong inversion takes place. Sub-threshold Slope [11] is given by:

$$\text{SS} = \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1} = \frac{KT}{q}\left(1 + \frac{c_d}{c_i}\right) \tag{4}$$

Where C_d= depletion layer capacitance
C_i=gate oxide capacitance.

III. Transport Of Carriers

The Cogenda Genius TCAD Device simulates the I_{DS}-V_{GS} performance of DG-MOSFET using the basic drift-diffusion transport model.

1.2 Drift diffusion model

The conduction in this model depends upon the Poisson’s equation (5) and continuity equation of the carriers (6), (7). The Poisson’s equation which transforms the electrostatic potential V to the density of charge is given by [12]:

$$\nabla^2 V = -\frac{q}{\varepsilon}[p - n + N^+{}_D + N^-{}_A + n_T] \tag{5}$$

Where n and p represent the densities of the electrons and the holes, respectively, N_D^+ and N_A^- are the ionized donor and acceptor impurity concentrations respectively, n_T denotes the density of charge carriers due to presence of centre of recombination and ε is the corresponding dielectric constant. The current densities of electrons and the holes are given by the transport equations usually composed of two components, drift and diffusion .

$$J_n = q\mu_n nE + q\,D_n \nabla_n \qquad (6)$$

$$J_p = q\mu_p pE - q\,D_p \nabla_p \qquad (7)$$

Where μ_n, μ_p are electron and hole mobilities respectively, D_n and D_p are the diffusion coefficients of electrons and holes. Also ∇_n , ∇_p are the corresponding two dimensional concentration gradients of electrons and holes respectively. E is the electric field which is being applied. The equations of continuities demonstrate the Conservation of carriers in a particular volume element for electrons and holes respectively.

$$\frac{\partial n}{\partial t} = GR_n + \frac{1}{q}\nabla J_n \qquad (8)$$

$$\frac{\partial p}{\partial t} = GR_p - \frac{1}{q}\nabla J_p \qquad (9)$$

The GR_n and GR_p represents the process of recombination and generation and J_n , J_p are their corresponding current densities . The EOT (Equivalent Oxide Thickness) is given by [13]

$$\text{EOT} = \frac{Ksio_2}{K_{High-k}}(T_{high-k}) \qquad (10)$$

Where K_{sio2}, K_{High-k} are the dielectric constant of SiO_2 and the High-k dielectric material and T_{high-k} represents the thickness of high-k material. Work function plays in important role in device Simulation of DG MOSFET. By using appropriate Work Function we can change the threshold voltage at same Voltage, Thus helps in decreasing Leakage current.

1.3 Work Function

may be defind as the energy that must be supplied to an electron to take it across the surface energy barrier . It is denoted by Φ_m (eV). Also it is the energy difference between the vaccum level E_0 and the Fermi energy of the metal E_{fm} that is $\Phi_m = E_0 - E_{fm}$. In a semiconductor and insulator, the height of the surface energy barrier is specified in terms of electron affinity χ .given by $\chi = E_0 - E_c$ that is the energy difference between the vaccum level E_0 and conduction Band edge E_c at the surface. χ function varies with respect to doping.[14] For p-type semiconductor, $\Phi s = \chi_s + \frac{E_g}{2} + q\Phi_{fp}$ (eV) Where Eg=Band gap energy, Φ_{fp} is fermi potential for p-type, $|\Phi_{fp}| = |\Phi_{fn}|$(Fermi potential for n-type)= Φ_f that is for same doping concentration, Then $\Phi_f = V_T \ln(\frac{N_b}{n_i})$,where $V_T = \frac{KT}{q}$ =Thermal Voltage, N_b=Substrate Dopant Concentration [15] .

IV. Device Structure

The DG MOSFET structure is shown below. As we have worked on 25nm, 13nm technology so the length of channel is 25nm or 13nm. The structure consists of two heavily doped n-type source and drain regions of length 25nm .It contains a p-type doped silicon channel of width 8nm. The polysilicon gates are separated from the silicon channel by gate oxide layer having a power supply voltage V_{DD} of 0.7 V. In this paper, Proposed model DG MOSFET using high dielectric permittivity SiO2,HfO2 and ZrO2 with channel length 25nm and 13nm have been compared with previous ,Slimani Samia and Djellouli Bouaza model [16] having same channel length 25nm, 13nm and gate oxide thickness 1.5nm. We have used Work function (φ_m) of about 4.45 eV and 4.90 eV , where as in previous model they have used work function of about 4.1eV. The values of dielectric constant used in this work are 3.9 for SiO_2 , 21.2 for HfO_2 [17], and 25 for ZrO_2 [18].One of the main parameter in between the high Dielectric materials and silicon substrate is the conduction band offset (CBO). The values used of conduction band offset in our work are 3.1eV for SiO_2 [19], 1.4 eV for ZrO_2 [20] and 1.3 eV for HfO_2 [21,]. The various parameters used for device in our simulations are summarized in Table1.

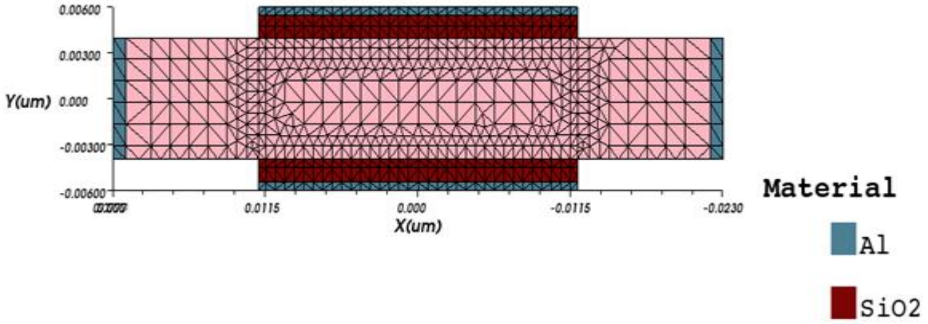

Table1. Various Parameters used for device simulation

Parameter	**DG MOSFET**
Channel Doping	10^{15} cm ^{3}
Source and Drain Doping	1×10^{20} cm ^{3}
Channel length (L_G)	25nm, 13nm
Oxide thickness	1.5nm
Channel width	0.08µm
Work function of metal gate	4.45eV,4.90eV

V. Results And Discussion

Using the proposed model, the $I_D(V_{GS})$ curves having gate dielectrics as SiO_2, HfO_2 and ZrO_2 for EOT=1.5nm at $V_{DS}=V_{DD}=0.7V$ are plotted in Figures 2-3 for channel length 13nm and 25nm respectively. These Figures shows the variations of the Drain current with respect to gate voltage for DG MOSFET devices .Some important parameters for device operation derived from $I_D(V_{GS})$ characteristics are summarized in Tables 2-4. These parameters usually includes DIBL, Sub threshold Slope, and Leakage current at $V_{GS}=0$. The large reduction in gate leakage current in the proposed model as compared to previous can be demonstrated by the fact that the use of a high-k gate material having high work function .From Table 2-4, it is clear that using proposed model there is subsequent decrease in Sub-threshold Slope as well. Almost degraded by 14% as compared to previous Model . As, we all know that Threshold Voltage is Channel length dependent. With the increase in channel length (L_G), Threshold voltage increases. Threshold voltage can be found from I_{DS} - V_{GS} curve using Constant current method. From equation (2), it is observed that as we increase work function from 4.1 eV(used in previous model) to 4.45 and 4.90 (proposed model), there is increase in threshold voltage. With the increase in threshold voltage leakage current decreases clear from equation (1).

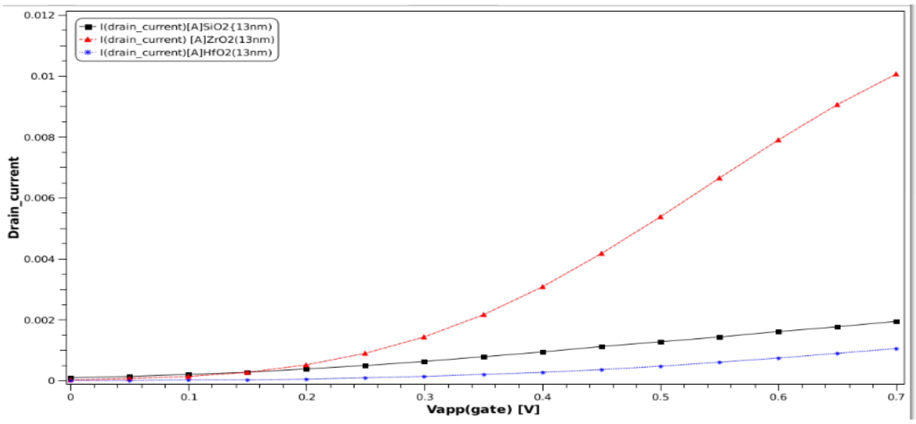

Figure2. I_{DS} versus V_{GS} curve of For Proposed model with L_G=13nm,

Further we have observed from the proposed model that there is huge reduction in leakage current almost 100% and 94% when L_G =25nm as compared to previous model for gate dielectrics HfO_2 and ZrO_2 respectively. In case of L_G=13nm there is about 16% and 23% reduction in leakage current in HfO_2 and ZrO_2 respectively shown in Figure5 .It is clear from Figure4. and Table 2-4, there is decrease in DIBL with the increase in channel length. However consequent decrease in DIBL is observed more in case of proposed model as compared to previous one. So, gate electrode with L_G=13nm shows more decrease in DIBL as compared to previous model. Consequently, ZrO_2 with L_G=13nm shows largest reduction in DIBL that is 86% as compared to HfO_2 (19%) and SiO2 (58%) in proposed model. However with the decrease in channel length, DIBL increases due to increase in work function, but sub-threshold slope decreases. So, we have to choose the optimum value of work function for which both DIBL and Sub-threshold Slope have better values .

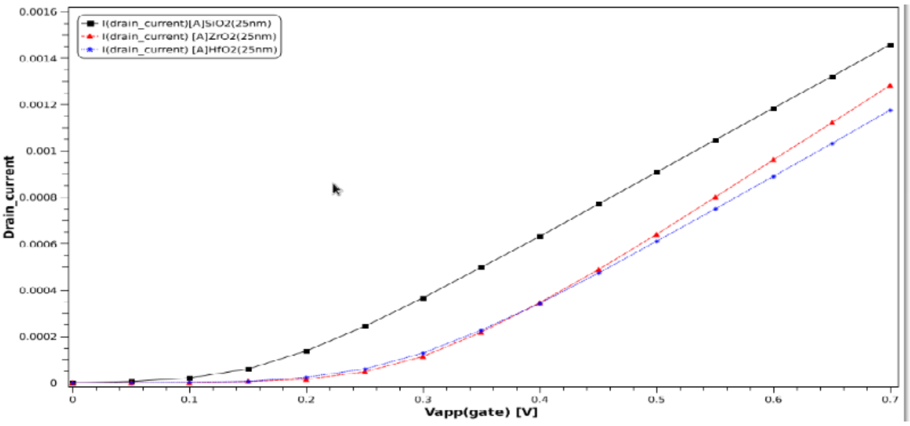

Figure.3 I_{DS} Versus V_{GS} curves For Proposed Model with L_G =25nm

Table 2.Simulation results for DG MOSFET with SiO_2 as Gate Dielectric

Parameter	L_G=25nm EOT=1.5nm Previous	L_G=25nm EOT=1.5nm Proposed	L_G=13nm EOT=1.5nm Previous	L_G=13nm EOT=1.5nm Proposed
Sub-threshold Slope (mV/decade)	119	102	219	202
OFF(Current)A/µm	1.48e-06	1.20e-06	3.4e-05	3.035e-05
DIBL(eV)	0.0419	0.0220	0.055	0.0230

Table 3.Simulation results for DG MOSFET with HfO_2 as Gate Dielectric

Parameter	L_G=25nm EOT=1.5nm Previous	L_G=25nm EOT=1.5nm Proposed	L_G=13nm EOT=1.5nm Previous	L_G=13nm EOT=1.5nm Proposed
Sub-threshold Slope (mV/decade)	82	70	94	80
OFF(Current)A/µm	2.83e-07	8.60e-11	5.53e-06	4.99e-06
DIBL(eV)	0.018	0.0153	0.0199	0.0160

Table 4.Simulation results for DG MOSFET with ZrO_2 as Gate Dielectric

Parameter	L_G=25nm EOT=1.5nm Previous	L_G=25nm EOT=1.5nm Proposed	L_G=13nm EOT=1.5nm Previous	L_G=13nm EOT=1.5nm Proposed
Sub-threshold Slope (mV/decade)	63.4	50	84.67	72.01
OFF(Current)A/µm	9.6e-08	4.98e-11	2.99e-07	2.30e-07
DIBL(eV)	0.014	0.0070	0.055	0.00760

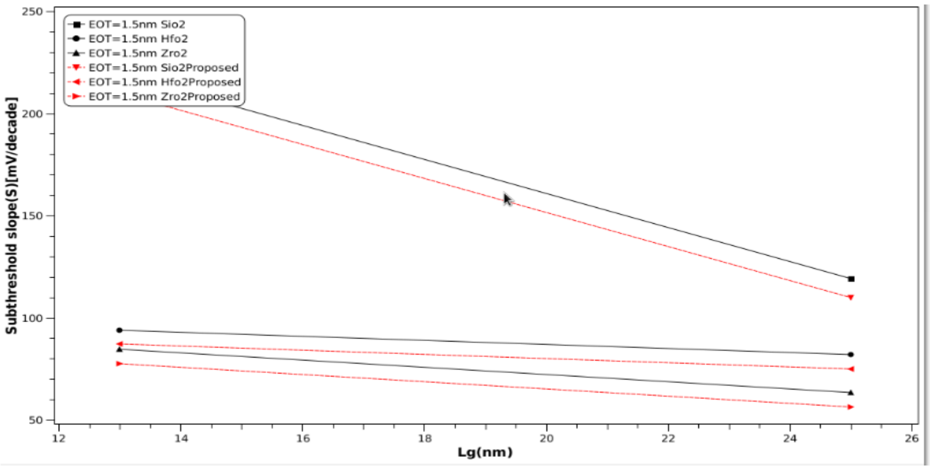

Figure 4. Sub-threshold Slope versus channel length (L_G)

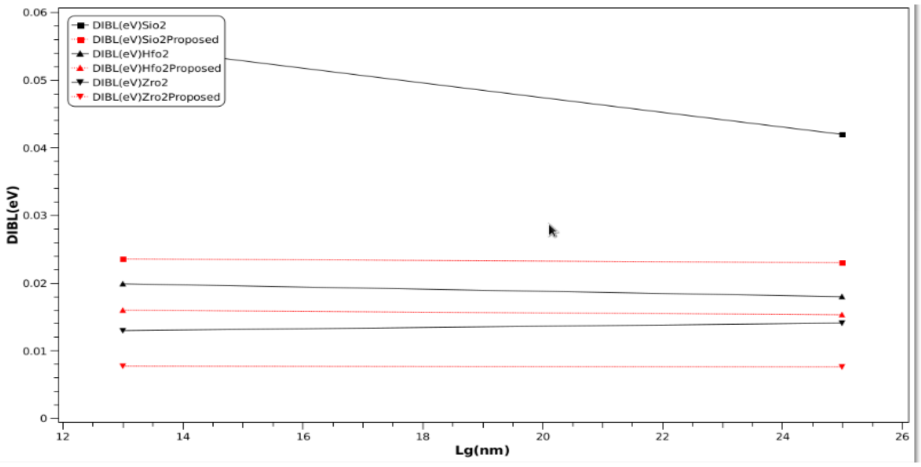

Figure 4 . DIBL versus channel length (L_G)

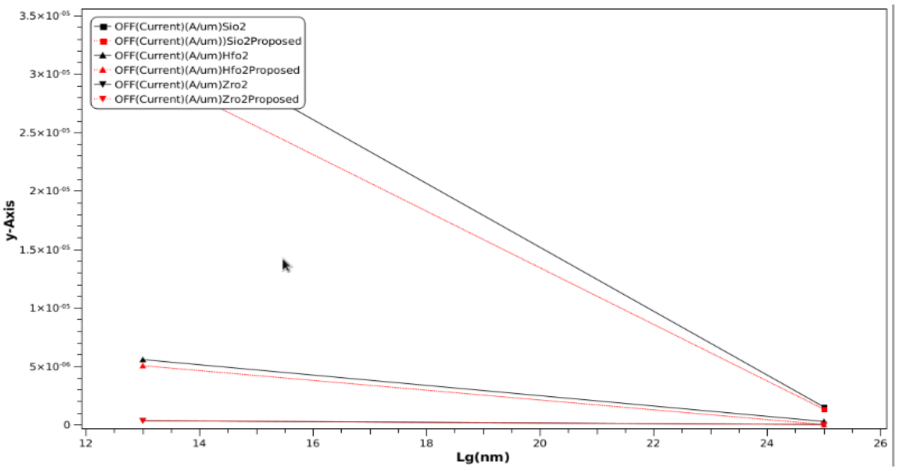

Figure 5. Leakage current versus channel length (L_G)

VI. Conclusion

Scaling of MOSFET device is needed to increase the speed and density, but it degrades the Device performance with respect to short channel effects and Leakage current. In this proposed model DG MOSFET structure using High-k dielectric material and high work function value , threshold voltage is increased , so as to decrease leakage current, sub-threshold Slope and achieve optimum value of DIBL so as to increase device performance. The proposed model is then compared with previous one and we found that leakage current and sub-threshold slope reduces significantly as compared to previous model. The Simulations were performed by 3-D TCAD COGENDA GENIUS Simulator which makes use of Drift-Diffusion model for respective transport of carriers. Using High-k Dielectric material having high work functions, there is significant decrease in I_{off} current, lowers Sub-threshold Slope, takes optimum value of DIBL and increase On current . So, in turn maximizing I_{on}/Io_{ff} ratio.

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