

Design Analysis of Full Adder Using Cascade Voltage Switch Logic

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Abstract: The paper presents a new design for full adder by utilizing the cascade voltage switch logic. Adders are the basic building block for all the functional units of microprocessors and digital signal processors. In the growing era of nanotechnology, it has become necessary to develop methodologies to efficiently reduce the area and power consumption. The CVSL helps in achieving the higher layout density with minimal delay time. The design is implemented at 45nm technology and compared with standard cell 45 nm technology full Adder. The delay occurring and power considerations along with the transistor count have been studied and it has been found that in CVSL, power is 22% better and delay time is 39 % better than the conventional design with almost same transistor count.

Keywords : Circuit Simulation, CMOSFET Circuits, CVSL, Full Adder.

I. Introduction

Adders are the one of the most important logic components used in the design of digital VLSI circuits. Addition is the basic arithmetic operation. It forms the basis for almost all computations from multiplying to counting to filtering. Apart from carrying out the tasks of addition which is its basic function, the adder forms the basis for many complex circuits like the multipliers, subtractors, to RAMs, address calculations and many more [1]. The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. There are two types of adders: Half Adder and Full Adder. The half adder is the simplest type of adder which is capable of performing the simplest type of addition logic while generating a carry. It takes two inputs and generates two outputs Sum and Carry. The Full Adder is the complex type of addition circuit. The basic difference between the two types of adders is that the full adder has 3 inputs that include the carry of previous output as well while the half adder doesn't uses that [2]. This paper deals in the study of most widely used adder which is full adder. The full adder is a simple, functional digital circuit built from two logic gates. The logic gates used for the design of the full adder are the XOR ,AND gates and an OR gate [3]. A full adder can be constructed using two half adders. A 1 bit full adder is used to carry out the addition of three one bit numbers. For A, B and C_{in} , where A and B are operands to be added, and C_{in} is the carry that is the bit carried forward form the least significant bit of last calculation [4]. The basic logic arrangement and truth table for full adder is as shown in Figure 1 and Table 1 respectively.

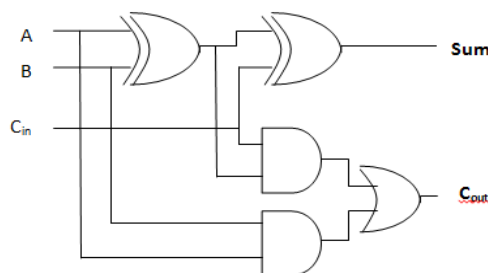


Figure 1: Full Adder

Table 1: Truth Table for Full Adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	0	1	1	1

As is seen from the above logic circuit diagram and the truth table, the first half of the logic circuit will be used to perform the partial SUM of A & B while the second half logic will be used to perform the addition of the C_{in} and the partial sum produced in the first half logic to get the final output SUM (S) of the Adder. The carry generated if any in the two half adders will be used to produce the final Carry output by implementing the OR of the two, and the final output Carry (C) is obtained. The critical calculation of the adder runs with the help of XOR and AND gates. The logic for SUM is computed by using XOR gate while the carry is generated with the logic of AND gate [5]. The Boolean expressions for the full adder logic are as given in equations 1 and 2 below:

$$\text{SUM} = A \oplus B \oplus C_{in} \quad (1)$$

$$\text{CARRY} (C_{out}) = A \cdot B + (C_{in} \cdot (A \oplus B)) \quad (2)$$

The XOR gate is the basic logic block required to build full adder circuit. Thus by enhancing the performance of the XOR gate, efficient full adder can be obtained. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip there by reducing the area and delay.

Several logics have been proposed regarding its implementation since it was introduced. These modifications are aimed at reducing the number of transistors used to perform the required logic. The major aim in reducing the number of transistors is to accommodate more devices on a given silicon wafer there by reducing the total area utilized. One of the ways to reduce power is to explore new types of circuits in order to find better circuit techniques for energy savings [5].

II. Cascade Voltage Switch Logic

The CVSL, acronym for cascade voltage switch logic is one such type of logic circuit. CVSL is a type of logic circuit whereby both true and complement inputs are required. Two complementary NMOS switch structures are constructed and then connected to a pair of cross-coupled pull-up PMOS transistors [6]. The clocked CVSL circuit is two domino gates operating on true and complement inputs. The CVSL has two storage nodes for each gate instead of one, resulting in higher tolerance of SET pulses than CMOS. Static and clocked CVSL test circuits are fabricated utilizing two complementary NMOS switch structures are constructed and then connected to a pair of cross-coupled pull-up PMOS transistors. The clocked CVSL circuit is two domino gates operating on true and complement inputs. The CVSL has two storage nodes for each gate instead of one, resulting in higher tolerance of SET pulses than CMOS. Static and clocked CVSL test circuits are fabricated utilizing a double polysilicon double metal N-well CMOS technology [7, 8]. The gate level design for the basic CVSL is as shown in figure 2.

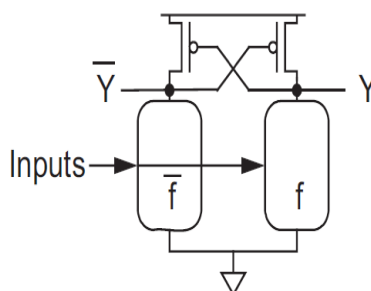


Figure 2: Basic CVSL Circuit

As is seen in the figure above, N pull down trees are the dual of each other and the P pull up devices are cross coupled to the latch output. The pull down network f implements the logic as in a static CMOS gate while \bar{f} uses inverted inputs feeding transistors arranged in the complement. The true input is applied to right pull-down leg below and complement input is applied to left leg of the N pull down network. The basic working principal is as explained below:

1. For any given input pattern, one of the pull down networks will be ON and the other OFF.
2. The pull down network that is ON will pull that output low. This low output turns ON the pMOS transistor to pull the opposite output high.
3. When the opposite output rises, the other pMOS transistor turns OFF so no static power dissipation occurs [9].

For the sake of understanding, a basic CVSL implementation of OR/NOR logic is as shown in figure 3 below with a voltage source V_{dd} applied to it. The logic is generated between two inputs A & B and the output is generated for OR and NOR logic [10].

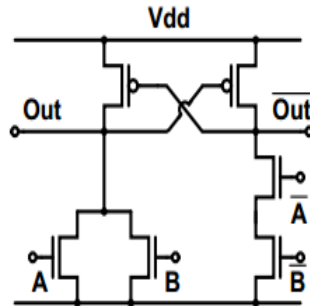


Figure 3 : OR/NOR implementatuion in CVSL

There is another concept while studying the CVSL which the dual rail domino. Dual-rail domino or clocked CVSL is shown in Figure 4. This category of domino does not suffer from contention problems, which makes it as fast as standard domino. Also, dual rail domino logic provides both inverting and non-inverting functions, which makes it easy to use in digital logic design [9].

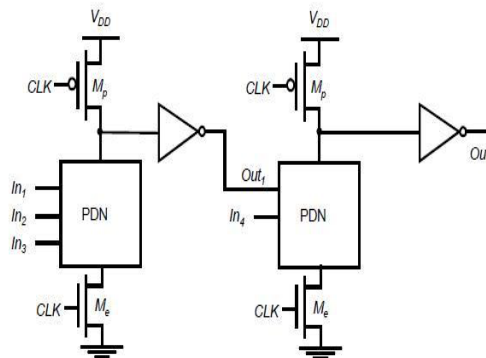


Figure 4: Dual-Rail Domino Logic

The main disadvantage of dual rail domino gate is its unity activity factor since an evaluate/precharge transition is guaranteed at every cycle regardless of the input activity or input states. Therefore, dual-rail domino suffers from high power consumption, added to that is the clocking power [10]. Also, dual-rail domino cannot recover from noise upsets, similar to standard domino.

Dynamic Differential Cvsl

Dynamic DCVSL is a combination between the domino logic and the static DCVSL. The advantage of this style over domino logic is the ability to generate any logic function. Domino logic can only generate non-inverted forms of logic [11]. For example, in the design of a ripple carry adder, two cells must be designed for the carry propagation, one for the true carry signal and another for the complementary one. Using DCVSL to design dynamic circuits will eliminate p-logic gates because of the inherent availability of complementary signals. The p-logic gates usually cause long delay times and consume large areas [12-13].

III. Cvsl Designs

The result & analysis of the full adder is done using the cascade voltage switch logic (CVSL) in CADENCE software. The schematic is constructed using 45nm technology. The logic output for the full adder is obtained. The designed schematic is compared with the standard cell Full Adder present in the standard gpdk 45nm standard cell library. The standard full adder is present in the 45 nm standard cell library. Suitable biasing is done to make it functional. The schematic for the standard gpdk 45 nm CMOS based Full Adder is as shown below in figure 5. The biased symbol, showing the 3 input variables and the output Sum and carry, used for performing the simulation is as shown in the figure 6.

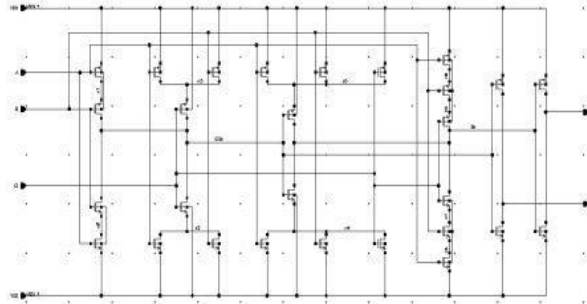


Figure 5: Standard 45nm Full Adder.

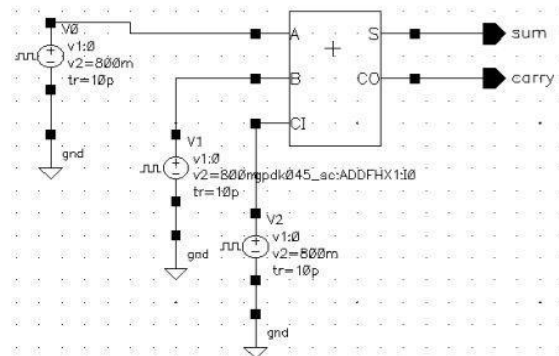


Figure 6: Biased Standard Full Adder

The Cascade voltage switch level based design for the full adder is designed using the 45 nm technology. The designed logic implementation is as shown below in figure 7.

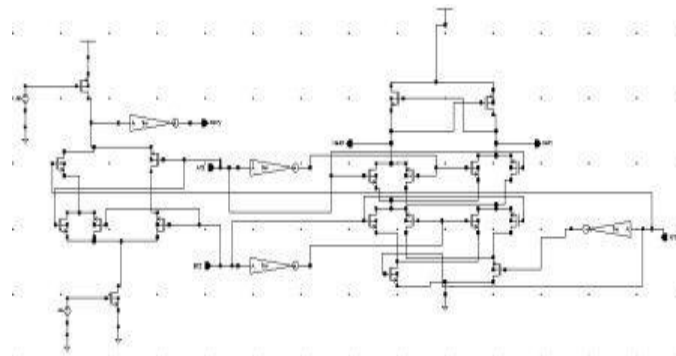


Figure 7: CVSL based Full Adder

IV. Result Simulation

The simulations of the standard cell and CVSL based Full Adder are done using identical standard so as to maintain the symmetry in the analysis. The waveforms obtained for the standard cell full adder is as shown in figure 8 below.

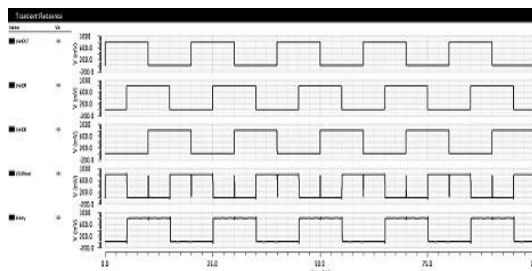


Figure 8: Standard Cell Full Adder Output Waveform

The CVSL based design of the proposed FULL Adder is as shown the figure 8 and the corresponding waveform is shown in figure 9.

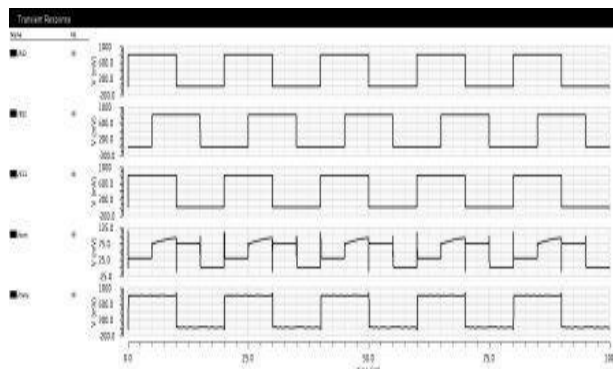


Figure 9: CVSL Full Adder output waveform.

Both the adders are designed and the analysis is done and both the designs are compared for the two most important parameters considered in the design of logic circuits. These are the power consumed in the circuit and the delay produced in the device during the simulation phase. Along with these, the number of transistors are counted and compared the results. The results obtained are tabulated and is shown below in the Table 2.

Table 2: Parameter Comparison for Full Adder.

Circuit	Power consumption (nW)	Propagation Delay (ns)	Transistor Count
Conventional Full Adder	24.146	110.0 ns	29
CVSL Full Adder	18.942	67.22 ns	27

V. Conclusion

From the design and analysis done for the standard and CVSL based design of Full Adder, it has been studied that the CVSL based design provided much less Power consumption whose value for CVSL design is 18.943nW which is much less than 24.146nW, being the power consumption of conventional design. Also the delay time during simulation is only 67.22ns which is also much better than conventional design delay which is 110 ns. Thus, the CVSL design is a better choice for the efficient design of Full Adder for use in complex circuit design.

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