IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 3, Ver. I (May. -Jun. 2016), PP 38-44
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and Performance Analysis of Barrel Shifter Using 45nm Technology

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Abstract:*Barrel Shifter plays an important role in optimizing the RISC processor and used for rotating and shifting the data either in left or right direction. This shifter is useful in many signal processing ICs. The arithmetic and logical shifter are itself a type of barrel shifter. The main objective of this paper is to design a fully custom two bit barrel shifter using 2x1 multiplexer with the help of CMOS logic and analyse the performance on basis of power consumption, time delay and no of transistors. The tool used to fulfill the purpose is cadence virtuoso using 45nm technology. The power consumption is reduced by 76.37% and time delay by 91.77% in the proposed design.*

Keywords:*Barrel Shifter, CMOS, MUX, Power consumption, Time delay*

I. Introduction

In RISC processor Arithmetic Logical Unit performs math and intelligent operations. Number-crunching operations incorporates expansion, subtraction, increase and division likewise sensible operations incorporates AND, OR, NOT, NAND, NOR, XNOR and XOR. The RISC processor contains register documents used to store the operand in burden/store directions. The point of control unit is to give a control flag that controls the operation of the processor which tells the small scale building design which operation is done at which time Barrel shifter puts a noteworthy part amid augmentation operation. In augmentation operation, fractional items to be moved and included by barrel shifters [1]

Fundamentally there are four sorts of shifters i.e. consistent shifter, math shifter, barrel shifter and channel shifter. A barrel shifter is a combinational rationale hinder that will move the substance of a transport determined number of positions left or great by a control word. This is an imperative capacity in PCs and numerous sign preparing ICs. Regularly, when moving to one side, the positions cleared will be loaded with qualities from the left, or if no qualities are accessible, then loaded with zeros also when no qualities are accessible, the emptied positions might be filled the estimation of the most critical piece (MSB) [2]. A few shifters really turn the substance of a transport filling the slightest critical bits (LSBs) with the past substance of the MSBs for a shift left and the other way around for a shift right.

The logical shifter is used to shift the bit in left or right direction; the empty spots are filled by zeros. In Arithmetic shifter the procedure for left shifting is same as logical but in case of right shifting the empty spot is filled by signed bit. Barrel shifter carries out the rotation of bits in left or right direction; in this the empty space is filled by the bit shifted. Funnel Shifter is combination of all shifters and rotator [3]. In this paper barrel shifter is designed using multiplexer and implemented using CMOS logic. The MUX used is made with the help of universal gates so that the time delay and power dissipation is reduced.

II. Barrel Shifter

A Barrel Shifter is part of a microprocessor CPU which can typically specify the direction of shift left or right, the type of shift circular, arithmetic, or logical and the amount of shift (typically 1 to n-1 bits). Barrel Shifters are usually used for the digital signal or general purpose processors to calculate the data. A barrel shifter is a digital combinational circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers (mux), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance [4].

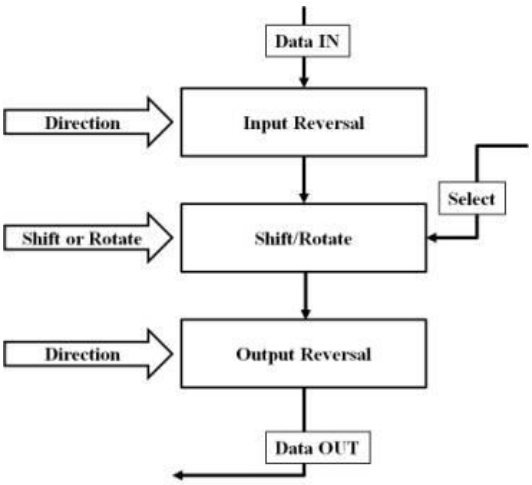

Fig.1 Basic block diagram of Barrel shifter

In Fig.1 data in provides the data to be rotated or shifted, the selects the mode whether the data is to shifted or rotated. The input and output reversal decides the direction and dataout provides the final desired output [5].

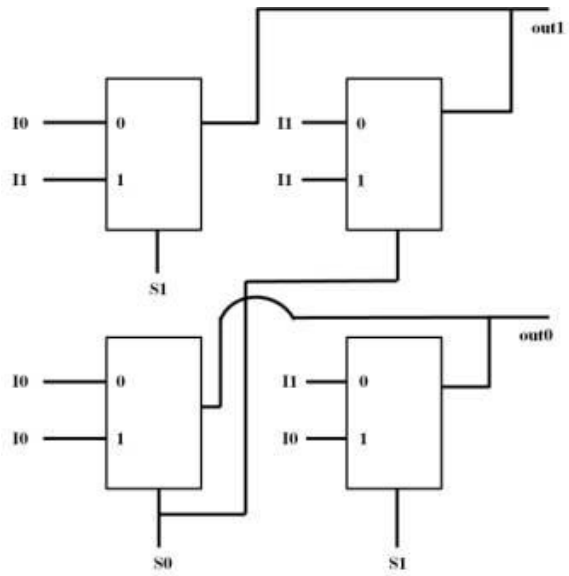

Fig.2 Multiplexer based 2X2 barrel shifter

The fig.2 shows the multiplexer implementation of 2x2 barrel shifter which is performing a left rotation of two bit if we provide i0 i0 i1 i1 as input then the output produced is in the sequence i1 i1 i0 i0.Input sequence is shifted by two bit to the left and LSB is filled by the shifted bits. Thus the rotation of two bits from left side is accomplished.

Now the shift and rotate logic is as shown below:

	1	1	1	1	1	0	0	0	0	1
Rotate Right 1	1	1	1	1	1	1	0	0	0	0
Rotate Right 6	1	0	0	0	0	1	1	1	1	1
	1	1	1	1	1	0	0	0	0	0
Shift Right 1	0	1	1	1	1	1	0	0	0	0
Shift Right 6	0	0	0	0	0	0	1	1	1	1
	0	0	1	1	1	1	1	1	1	0
Shift Left 1	0	1	1	1	1	1	1	1	0	0
Shift Left 6	1	1	1	0	0	0	0	0	0	0
	1	0	1	1	1	1	1	1	1	0
Rotate Left 1	0	1	1	1	1	1	1	1	0	1
Rotate Left 6	1	1	1	0	1	0	1	1	1	1

Fig.3 Shift and rotate operation in Barrel Shifter.

There are different operations that can be performed using barrel shifter.In rotate operation the data can be rotated either in right or left direction.For example 1111100001 after rotating right by one bit the data is shifted in right direction by one bit and the output is 1111110000.Similarly if rotate the same data in right direction by 6 bit then the the output obtained is 1000011111.

In second example 1111100000 it is shifted to right by one bit 0111110000 while the same data shifted right by six bit which gives the output 0000001111.Similarly for the next input 0011111110the shifting of data is shown in left direction,firstly the input is shifted in left direction by one bit the output is 0111111100,in left shift the shifted data is removed and empty spaces are replaced by zeros.In rotating data left the input is 1011111110,firstly the data is rotated by one bit output is 0111111101,secondly the data is rotated by two bit output is 1111111010,lastly the data is rotated by six bit output is 1110101111.

Multiplexer

A multiplexer is a device used for selecting one input from several digital or analog inputs using combination of selection line to provide single output. It is also known as data selector.MUX is also used as parallel to serial converter. It has 2^n input lines using n select lines. Different types of mux can be designed for example 2:1,4:1,8:1..etc [6].

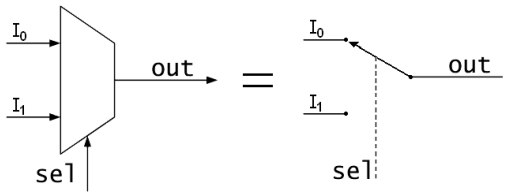

Fig.4 Basic block diagram of 2:1 Muliplexer.

The logic table for the implementation of 2:1 MUX is as shown in the Table 1. It shows the input select line (sel) and the output for the corresponding inputs I_0& I_1 [7].

Table 1 : Logic of 2:1 MUX

sel	I_0	I_1	out
0	0	0	0(I_0)
1	0	1	1(I_1)
0	1	0	1(I_0)
1	1	1	1(I_1)

Expression for the MUX logic table is as shown :
Out = sel'.I_0 + I_1.sel

III. Schematic Design

In Fig.4 the conventional design of 2:1 MUX is shown which is made by using NAND gate and NOT gate symbol in 45nm technology.

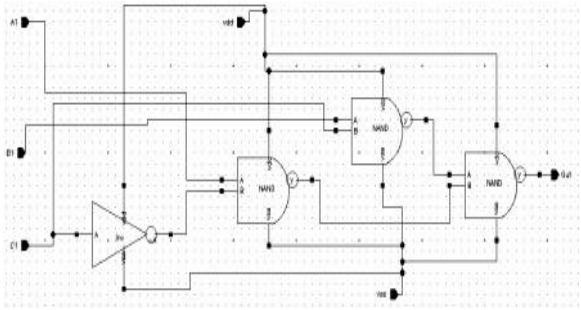

Fig 5: Conventional design of 2: 1 MUX

In Fig 5 proposed design of 2:1 MUX is shown in which transistor are placed using transistor logic.thus the no of transistors is reduced.Therefore the power consumption and time delay is also reduced further in the design of barrel shifter.

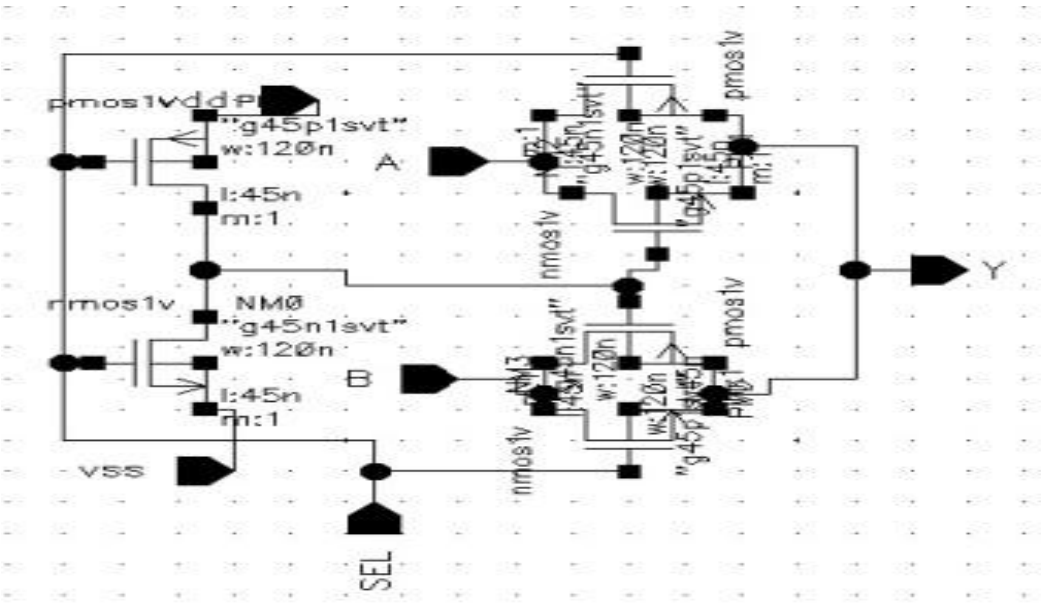

Figure 6: Proposed Schematic design of 2:1 MUX

In Fig.7 Barrel shifter is designed using mux symbol.The schematic of conventional and proposed design is discussed previously.

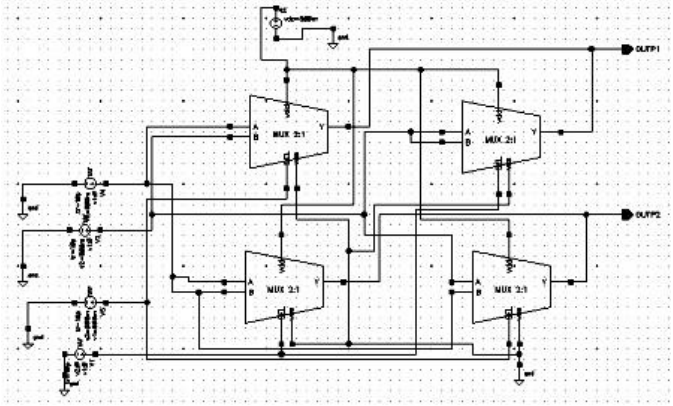

Fig 7: Schematic of 2X2 Barrel Shifter

IV. Simulations And Analysis

In fig.8 two inputs A, B and one selection line(SEL)are taken, the value of A is 0110011and so on and B is 1100110 and so on and SEL is 1000100 and so on and the output(Y) is obtained according to 2X1 mux, thus when A is low,B is high and SEL is high the output Y is high.Similarly, when A,B both are high and SEL is low then Y is high. In the same way output waveform is obtained but with a little distortion and after analysis it can be concluded that distortion occurs in output at the time of change of values of inputs.

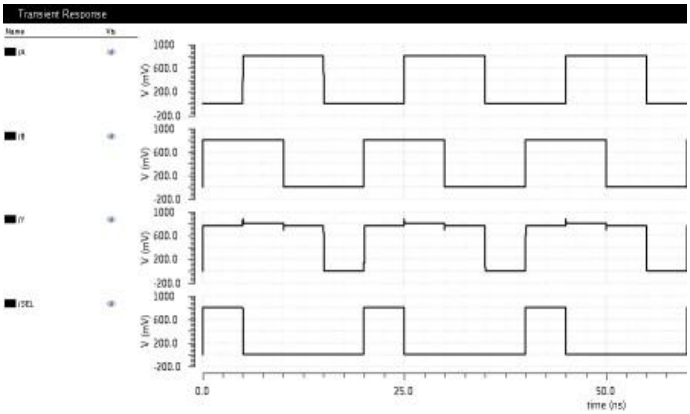

Fig 8: Transient Response of 2:1 MUX

Fig.9 shows the waveform of 2X2 barrel shifter in which input is shifted/rotated to the right by one bit and output is obtained. The output is shown for two inputs, in the first one rotated by one bit and in the second input its is shifted by one bit.

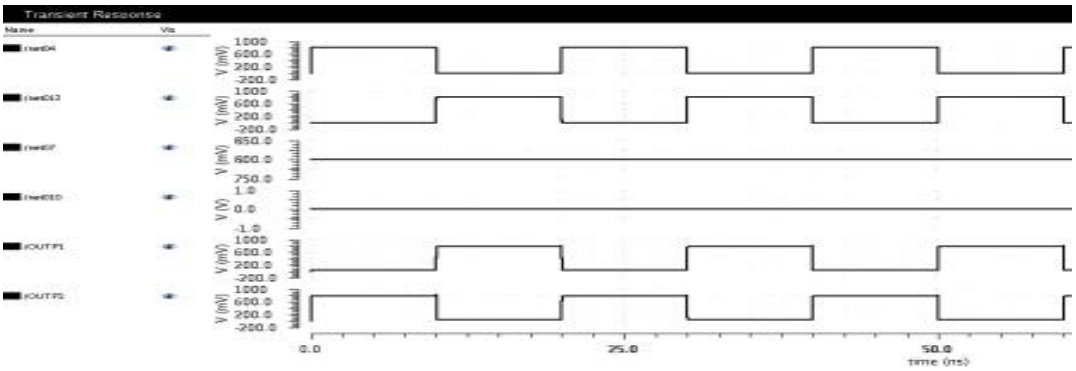

Figure 9: Transient Response of Barrel Shifter

The result & analysis of the barrel shifter is done in cadence virtuoso software. The schematic is constructed using 45nm technology. The transient response for the multiplexer and barrel shifter is obtained. The proposed designed schematic is compared with the conventional Barrel shifter made in the gpdk 45nm. The analysis is as shown below in table 2.on the basis of power consumption, time delay and no of transistors used. The same analysis is shown in fig 10 with the help of bar graph for easy understanding.

Table2: Performance analysis of Barrel Shifter.

Parameter	Conventional design	Proposed design	Percentage reduced
Power consumption (watt)	0.0435nW	0.01029nW	76.37%
Delay (sec)	0.0512ns	0.004ns	91.77%
Transistor Count	56	24	57.14%

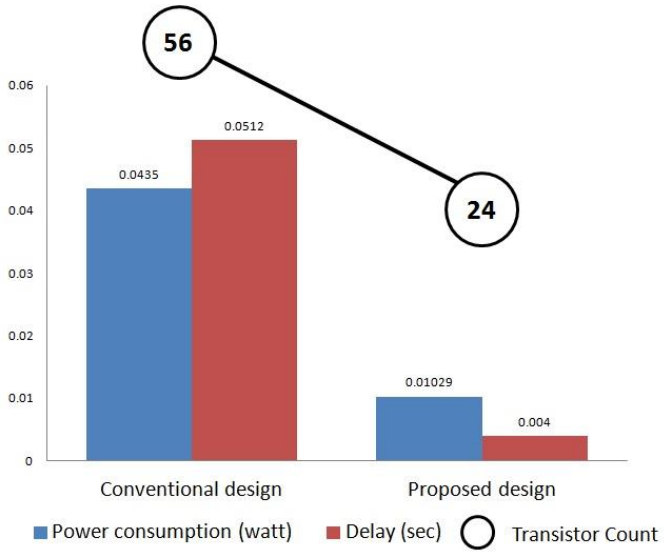

Figure 10: Performance analysis of Barrel Shifter

V. Conclusion

In this paper, two different MUX is designed one is using universal gates and other is using pass transistor logic, In NAND gate design no of transistors used are 14 while in pass transistor logic the no of transistors used are 6.Thus the final circuit for barrel shifter using conventional design i.e. using universal gate, uses 56 transistors with more power consumption and time delay .On the other hand the proposed barrel shifter uses total 24 transistors with less power consumption and time delay. From table2 the percentage reduced can also be seen. Thus it can be concluded that proposed barrel shifter is better than conventional circuit.

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