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Design and Implementation of Uart with Bist for Low Power Dissipation Using Lp-Tpg

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Abstract: *The main aim of this paper is to design and implement efficient UART and test the UART with built in self testing technique . A new Test pattern generator is simulated and used in BIST architecture in order to reduce power dissipation. As we know that power dissipation is more during the test mode than in normal mode hence In this project the pattern generator used is the low power pattern generator in order to reduce the power dissipation during test mode. The project is synthesized using Xilinx 14.5 design suite*
Keywords: *BIST,DFT,LP-LFSR, Test pattern generator, UART*

I. Introduction

As the number of components are increasing on the chip testing becomes more and more difficult, hence built in self testing technique is used in order to achieve high fault coverage and in speed testing.. The objective of the BIST is to reduce power dissipation[1].The main areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices are increasing rapidly. These applications require low power dissipation for VLSI circuits[1]. In general, the power dissipation of a system in test mode is more than in normal mode[2]. BIST is a DFT(design for testability) methodology aimed at detecting faulty components in a system by incorporating test logic on-chip. The main components of a BIST are the test pattern generator (TPG), the response compactor, and the signature analyzer. Test pattern generator used is basically LFSR that is linear feedback shift register this is mainly used to generate random patterns ,As the randomness of the patterns increases fault coverage will be increase. Among various Built in self test schemes, pseudo random BIST is most widely used since it is most economical. Power dissipation is a big problem for today's System on Chips (SOCs) design and test. Four reasons are blamed for power increase during test [3]. As the randomness of the patterns increases fault coverage will be increase. Among various BIST schemes, pseudo random BIST is one of the widely used since it is most economical. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test. Four reasons are blamed for High switching activity due to nature of test patterns, Parallel activation of the internal cores during test mode, Power consumed by extra design-for-test(DFT) circuitry and Low correlation among the test vectors. This extra power consumption (average or peak) can create problems such as instantaneous power rush that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime[3]. Built-In Self-Test (BIST) is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip.In BIST, a linear feedback shift register (LFSR) generates pseudo-random patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit). On the comparison side, a multiple input signature register (MISR) compacts test responses received from primary outputs or scan chain outputs. This paper is organized as follows: The Section 1 discusses brief introduction. The Section 2 deals with literature review. The Section 3 deals with proposed system design and methodology. The Section 4 provides the results and discussions.

II. Literature Review

There are various techniques available to reduce the switching activities of test pattern, which reduce the power in test mode. For LFSR that is linear feedback shift register, Giard proposed a modified clock scheme in which only half of the D flip-flops works, hence only half of the test pattern will be switched [4]. S.K. Guptha has proposed a BIST TPG for low switching in which there is d-times clock frequency between normal LFSR and slow LFSR thus the test pattern generated by original LFSR is rearranged in order to reduce the switch frequency. LT-TPG is proposed to reduce the peak and average power of a circuit during test [5]. The above said techniques can reduce the average power compared to conventional linear feedback shift register (LFSR). Modifying the LFSR by adding weights to tune the pseudo-random patterns for various probabilities reduces energy consumption and increases fault coverage [6], [7]. A low-power random pattern generation technique to decrease signal activities in the scan chain is proposed in [8].In the proposed Built in self test (BIST) architecture the pattern generator used is low power pattern generator, this pattern generator produces

random patterns with single input change, thus as the switching at the primary input(PO) reduces the power dissipation also reduces during the test mode

III. Proposed System Design And Methodology

3.1 Uart with Bist Architecture

The architecture proposes an 8-bit UART(Universal Asynchronous Receiver Transmitter) which operates at a baud rate of 9600 bps(bits per second) with a status register to monitor the correctness of every received data byte and to improve the testability of the circuit by the introduction of BIST module. The architecture of the 8-bit UART with Status register, incorporated with BIST module. The proposed model has two major modules that is UART and BIST[6]. later in the UART, we have transmitter, baud rate generator and receiver. Baud rate generator works at 50 MHz and later reduced as required for the operations in transmitter and receiver in order to achieve baud rate of 9600 bps. BIST module has a control register, pattern generator and a comparator. In BIST here we are using Low power test pattern generator in order to reduce power dissipation during the Test mode. The power dissipation during test mode is larger normal mode UART with Built in self test module is shown in figure 1

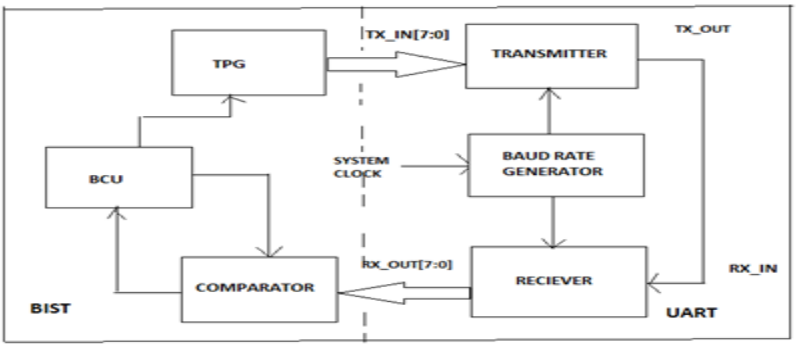

Fig 1. UART with BIST architecture

3.2 Bist Module

BIST module mainly consists of Test pattern generator, multiplexer ,circuit under test (CUT), output response analyzer, Rom and Comparator . Test pattern generator is used to produce random patterns ,output response analyzer used here is MISR(multiple input signature register) which is mainly used to produce signature this signature obtained is compare the obtained result with the golden signature and in this case CUT is UART.UART is the design which is tested using BIST technology. UART is set as a loop for the BIST by which it can test both the transmitter and receiver in the UART The Test pattern is generated by using Linear Feedback Shift Register method for the BIST. These test patterns are applied into the transmitter FIFO one by one and will be stored there and when the shift register is ready the data will be sent to TSR where the frame format is done by adding start bit, stop bit and parity bits then it is transmitted serially through TXOUT which will be received by the receiver where the additional bits except the data bits are sent into the error logic block and the data bits will be parallel sent into the receiver FIFO then they are sent into the MISR(multiple input signature register)here data compaction takes place and a unique signature will be produced for each output obtained from the UART output, data compaction is done in order to reduce the ROM size, then obtained result is compared with golden signature using BIST comparator. The BIST module comparator compares both the TX FIFO and RX FIFO and if the data is same then error will b will be set to '0' or else '1'.Block diagram of BIST module is shown in figure 2

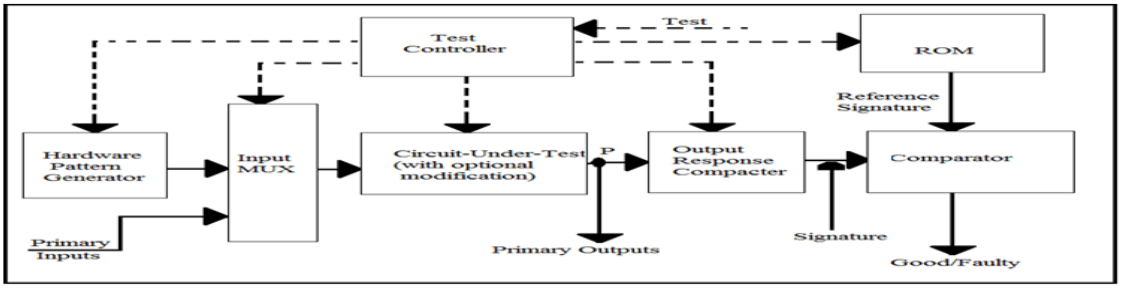

Fig. 2 BIST module

3.3 Low Power Pattern Generator

A low power test pattern generator has been proposed here consists of a modified low power linear feedback shift register (LP-LFSR) is shown in fig 3. The seed generated from LP-LFSR is Ex-ORed with the single input changing sequences generated from the gray code generator, effectively reduces the switching activities among the test patterns, when these patterns are applied to the UART during test mode it reduces power dissipation because of one bit switching between each consecutive patterns.

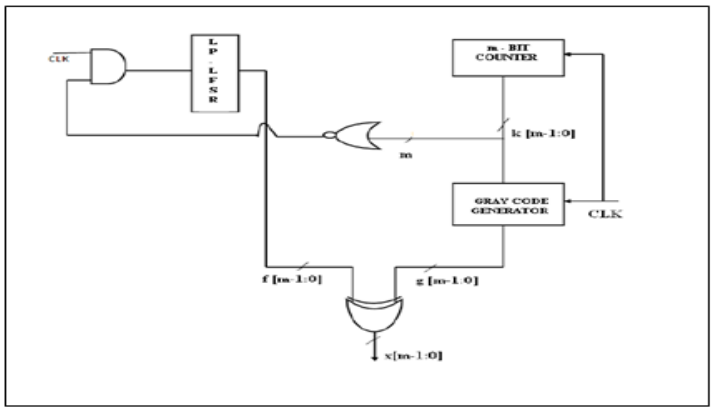

Fig.3 Low power pattern generator

3.4 Multiple Input Signature Register(MISR)

A response analyzer is the comparator with stored responses or an LFSR used as signature analyzer. It analyses the value sequence on primary output(PO) and compares it with expected output. Signature analysis is done with the help of multiple input signature register (MISR). we assume that the circuit under test has n outputs. It is seen that this circuit functions as n single-input signature analyzers. An n-stage Multiple input signature register has the property that the parity over all the bits in the input bits equals the parity of the final signature. The signature is produced after 2^n patterns generated.

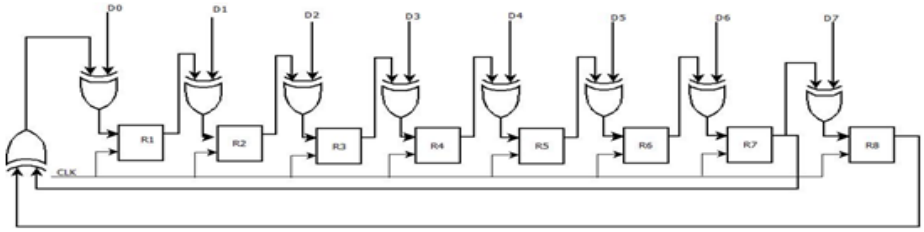

Fig.4 MIS

IV. Results And Discussions

The proposed system is designed using Xilinx 14.5 design suite and its implemented in Spartan xc3s400-4tq144. The language used here is VHDL. Design utilization summary is shown in Table.1

Design utilization summary			
LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION
Total number of slice register	2,182	7,168	30%
Number used as flip flops	109		
Number used as latches	2,073		
Number od 4 input LUT's	1,436	7,168	20%
Number of occupied slices	1,811	3,584	50%

Table. 1 Design utilization summary

The proposed system simulation results as follows. The simulation shows the 8 bit UART frame format UART frame with one start bit ,stop bit without parity bit as shown in figure 4

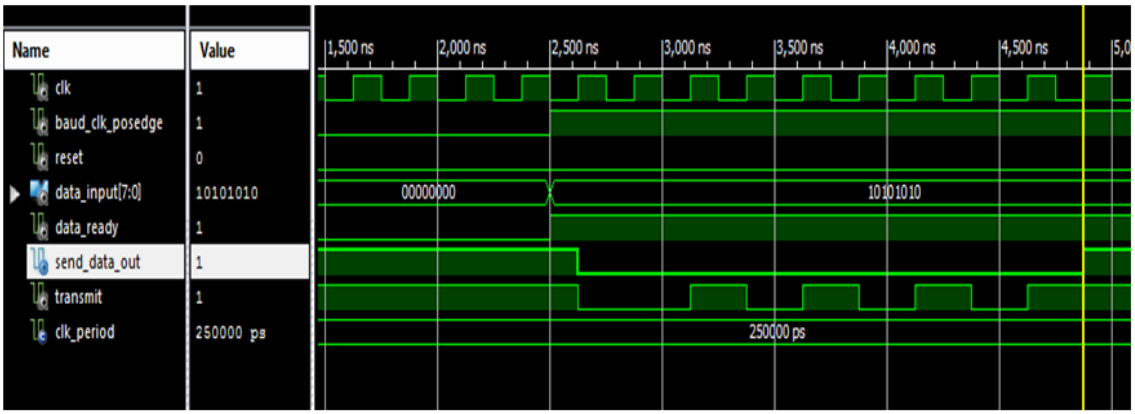

Fig.5 UART Transmitter output

The serial input is given through rs232_rxd signal and it is converted into parallel in the reciever side . when the recieving occurs byte_enable signal is set to logic high shown in figure 6

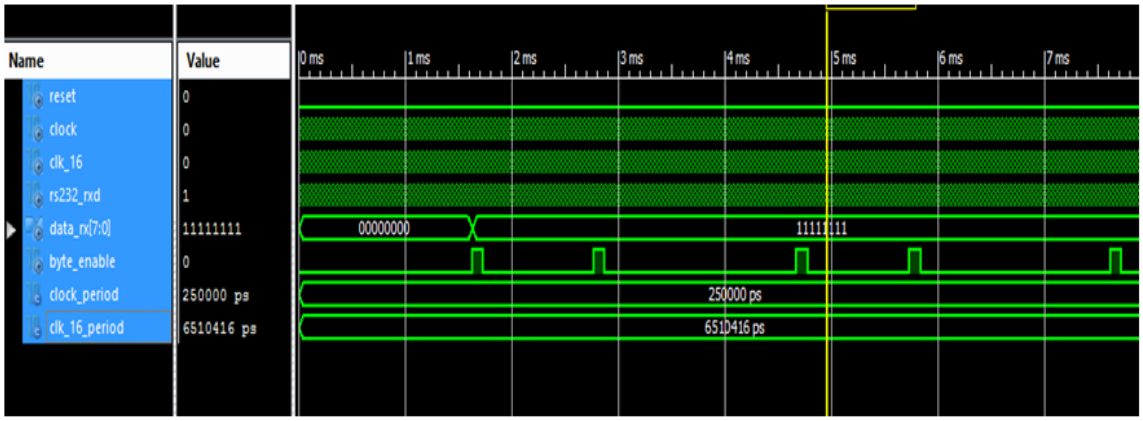

Fig.6 UART Receiver output

The parallel data is given through the input of the transmitter side and recieved at the reciever side as shown in Figure 7

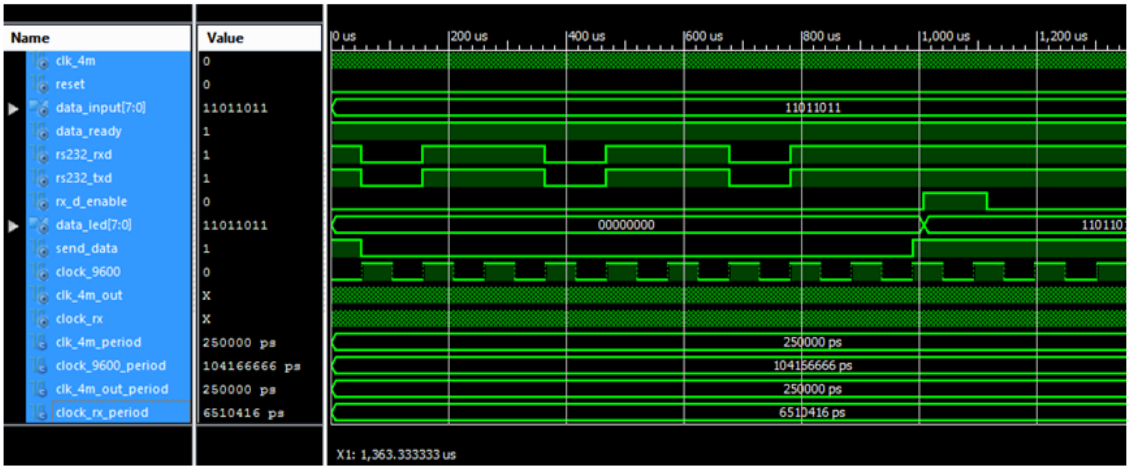

Fig.7 UART module

Low power pattern generator output is shown in the figure 6 every output is 1 bit switched which reduces switching activity.LP-LFSR outputs are shown in Figure 8

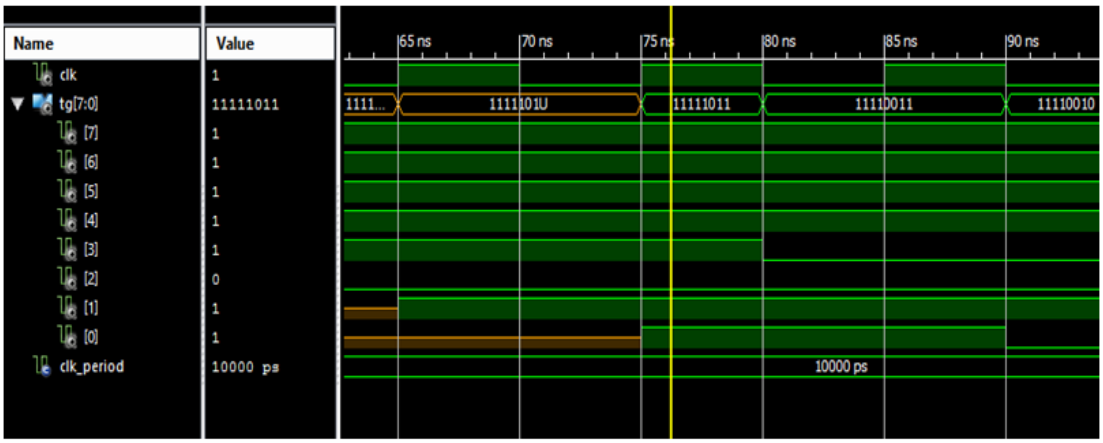

Fig.8 LP-LFSR

MISR(multiple input signature register) output shown in figure 9.The parallel input is given then the signature is generated after 2^n cycles. In this case 8 bit data is given and signature is obtained after 255 cycles .

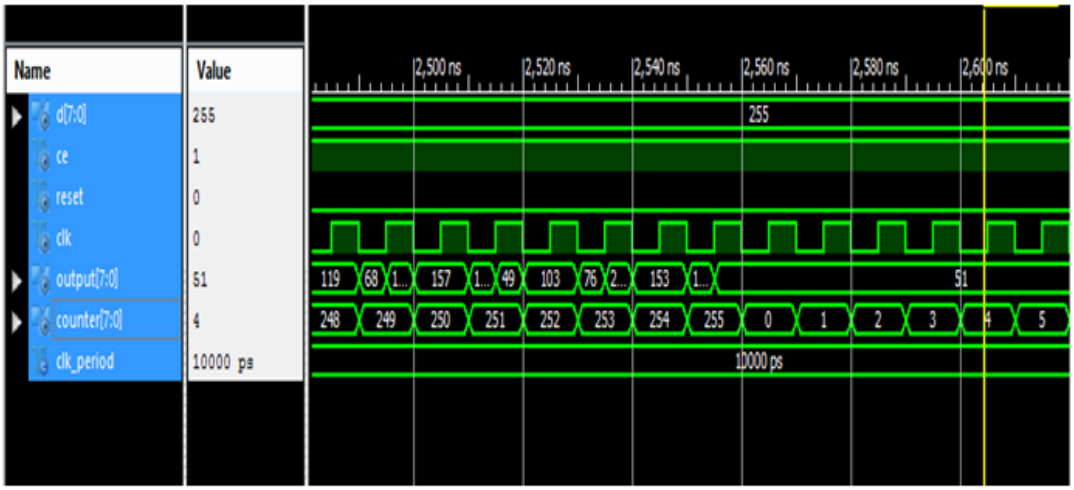

Fig.9 MISR output

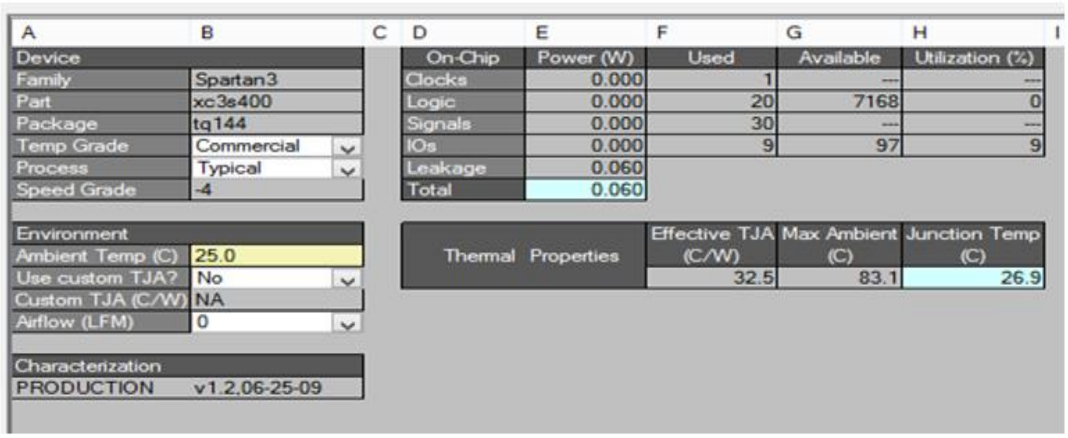

Fig.10 power analysis

POWER DESSIPATION		
	LFSR previous method	LP-LFSR latest method
POWER	70 mW	60 mW

Table.2 Comparison table

V. Conclusion

The simulated waveform presented in the paper shows VHDL implementation of UART embedded BIST technique and low power pattern generator is used in order to reduce the power dissipation during testing .The design is synthesized using Xilinx 14.5 design suite and implemented in Spartan 3s

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