

VLSI IMPLEMENTATION OF ARITHMETIC OPERATION

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Abstract: Design of reducing area, high speed and power are the major areas in VLSI system design. In this design parallel prefix adders are designed such as Kogge-stone adder, Brent-Kung adder, Ladner-Fischer adder. Radix-4 Booth multiplier is designed by using Kogge-Stone adder. Vedic multiplier and Vedic division is used to reduced area, LUT tables and increase the speed. The design is synthesized using Xilinx ISE 10.1 design suite and done Cadence Encounter.

Keywords: Prefix adders, Vedic multiplier, Vedic division, Radix-4 Modified Booth Multiplier.

I. Introduction

In leading technology arithmetic operation is the most important part in VLSI. Addition and multiplication is the fundamental function in arithmetic operation. Fast and accurate operation depends on the performance of the arithmetic operation. Ancient Vedic mathematics is used to reduce the computation time and also speed can be increased. Parallel adders like Kogge-Stone adder(KSA), Brent-Kung adder(BKA) and Ladner- Fischer adders(LFA) are used. Kogge-Stone adder is used to implement radix-4 booth multiplier by which area delay can be reduced. Urdhwa Tiryakbhyam and Pravartya Sutra is used by which area, delay and power consumption can be reduced. In advance technology different arithmetic operations are used by which delay, area, speed, power consumption, and performance can be improved. Depending on these factors efficient architecture were designed to implement arithmetic operation which is used in some of the VLSI applications. It is widely used in signal processing applications. Different types of methods are used by which speed of the system can be increased. Comparison of different types of operation is done by which parameter can be varied. One of the applications of arithmetic operation is DSP. The main aim of application is to reduce LUT, power, delay, and utilization so on. Adders and Multipliers are the important part in design of the processors. The speed of the addition and multipliers is a very important part in processing application. Adder is the most important block in digital system. As the technology improves the performance of the adder becomes more complicated. In digital and analog system addition of two numbers is done by dividing into individual and poly bit. Adders are not only used for calculation purpose but also in analog and digital components. The main part of the adder is to reduce the number of stages so that calculation can be done easily. Different types of adders are designed to compare the area, speed, delay in that one among is parallel adders. Parallel adder is same as carry look ahead adder. It can be designed in different ways to improve the speed of the adders It can be also called as faster adder. As the technology is growing widely there is vast demand for fast and accurate performance of processing application. So Vedic method is used by which speed, area can be increased. 'Vedas' means it is a treasure of knowledge. It is like storehouse where all arithmetic operation can be performed. So Vedic sutra is used by which calculation can be done easily. Vedic mathematics contains list of mathematical techniques used for calculation. There are 16 Sutra based on computation for efficient mental calculation. There are 16 Sutras: Ekadhikena Purvena, Nikhilam, Navatashcaramam Dashatah(ND), Urdhva Tiryagbyham Sutra(UM), Paravartya Yojayet Sutra, Shunyam Saamyasamuccaye Sutra, Anurupye Shunyamanyat Sutra, Sankalana-Vyavakalanabhyam Sutra(SV), Puranapuranyam Sutra, Chalana-Kalanabyham Sutra, Yaavadunam Sutra, Vyashstisamanstih Sutra, Shesanyankena Charamena Sutra, Sopaantyadvayamantyam Sutra, Ekanyunena Purvena Sutra, Gunitasamuchyah Sutra, and Gunakasamuchyah Sutra.

Among these 16 Sutra Urdhva-Tiryagbyham and Paravartya Yojayet is used for multiplication and division. Multiplication is the important component in fundamental operation. Usually in multipliers as the bit increases size of the design, area also increases. But in Vedic multipliers it consumes less size, delay, power. So usually Urdhva-Tiryagbyham is used by which speed of the multiplication can be increased. It is one among the fastest multiplier. It is a multiplication method in which calculation is done column and cross wise. Paravartya Sutra is used for Vedic division.

II. Implementation of Adders

The parallel prefix adders such as Kogge -stone adder, Brent-Kung adder and Ladner- Fischer adders are discussed below:

2.1 Kogge Stone adder

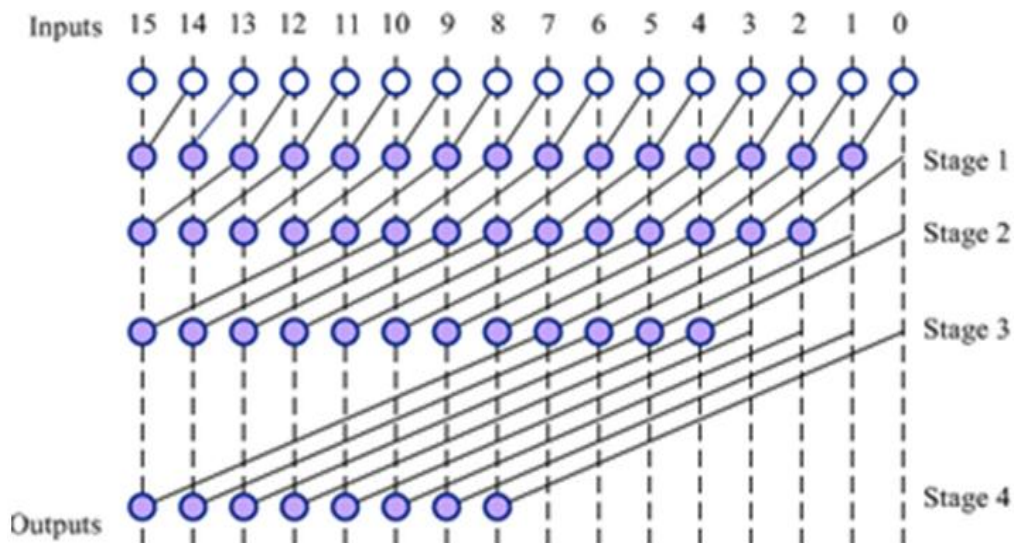


Figure 1. 16 bit Kogge Stone adder

In the Figure 1 the block diagram of 16 bit Kogge Stone adder is shown .It requires more area to implement but it has less fan-out.It generates and propagates the signal. It is considered as the fastest adder. It is widely used in industry because of high performance. Various components are used in this adder such as black cell, grey cell, generate and propagate block, buffers. Black cell is used computing generate and propagate signals. Grey cells is used computing generate signals. Buffer is used for balancing loading effect.

2.2. Brent Kung adder

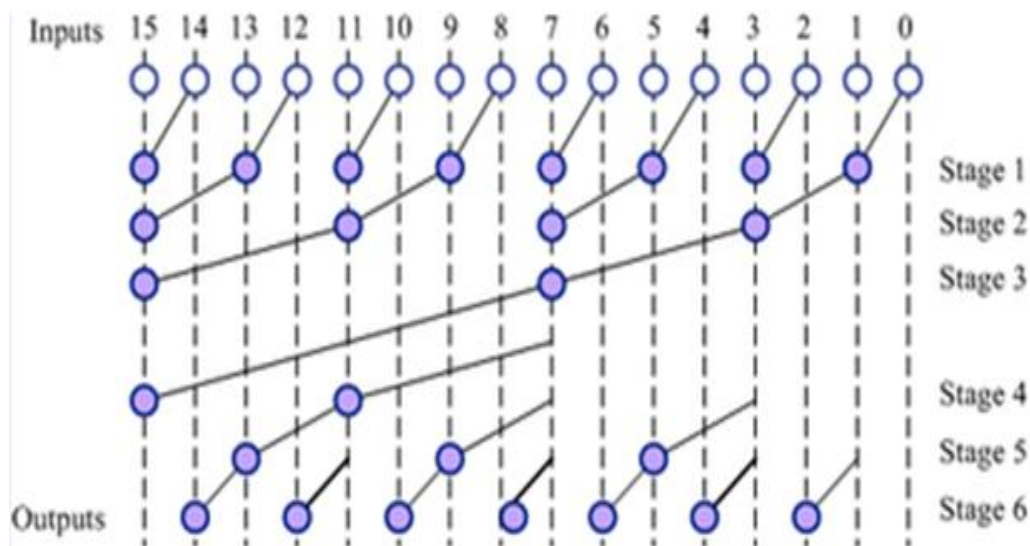


Figure 2. 16 bit Brent Kung adder

The block diagram of 16 bit Brent Kung adder is shown in above Figure 2.Less area is required to implement but it has large fan-out. It is also a logarithmic adder which generates number of stages from input to output. The depth of the gate level is $O(\log_2(n))$.The number of stages is calculated by $2(n-1) - \log_2^n$.

2.3 Ladner Fischer adder

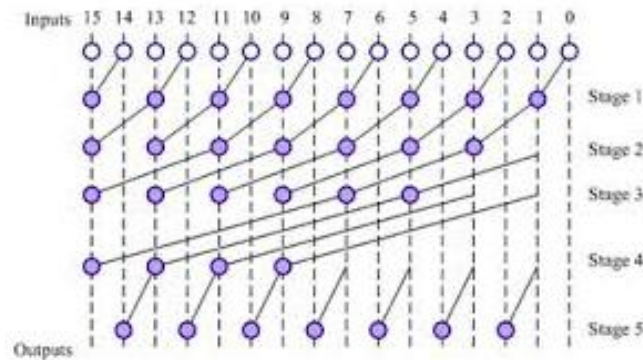


Figure 3.16 bit Ladner Fischer adder

In Figure 3 the block diagram of 16 bit Ladner Fischer adder is given in above Figure 3 To generate carry signal $O(\log n)$ time is required. It is also a faster adder. The performance of this adder depends on the minimum logic depth and fan-out. But it has large area.

III Vedic Multiplier

Vedic mathematics is obtained from 16 sutras to perform mathematical calculation. Sutras help to reduce time and also lessen effort by solving. Among those sutras Urdhwa Tiryakbhyam is used to perform multiplication. Urdhwa Tiryakbhyam is obtained from Sanskrit word Urdhwa and Tiryakbhyam which means vertical and crosswise.

2.1 2X2 Vedic Multiplier

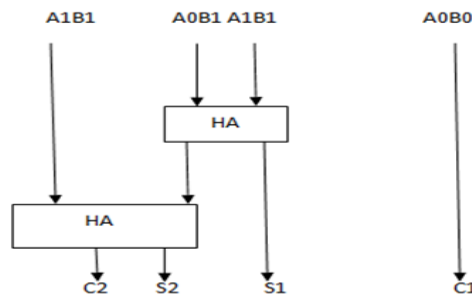


Figure 4. 2x2 Vedic multiplier

2 bit Vedic multiplier is implemented by four input AND gate and two half adder. 2 bit Vedic multiplier is same as the 2 bit array multiplier. The block diagram of 2x2 Vedic multiplier is shown in above Figure 4.

3.2 4x4 Vedic Multiplier

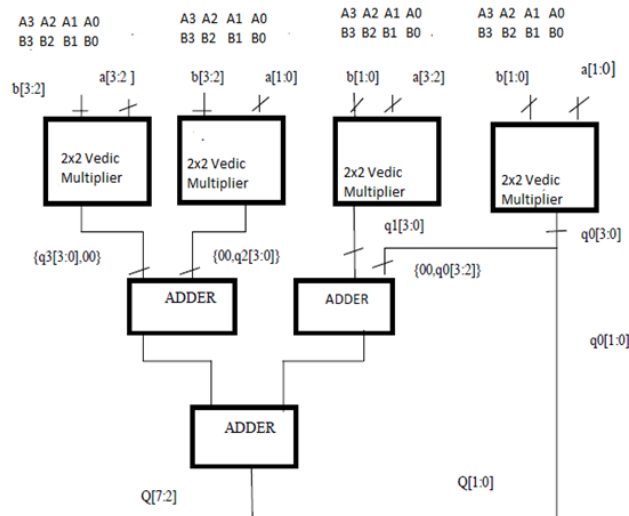


Figure 5. 4x4 Vedic Multiplier

4 bit Vedic multiplier is done by using single line in Urdhva Tiryagbhyam sutra. 4 bit Vedic multiplier is implemented by using four 2x2 multiplier and 3 adders. 2x2 Vedic multiplier is also done using two half adder and also by using four gates. The block diagram of 2x2 Vedic multiplier is shown in above Figure 5.

3.3 8X8 Vedic Multiplier.

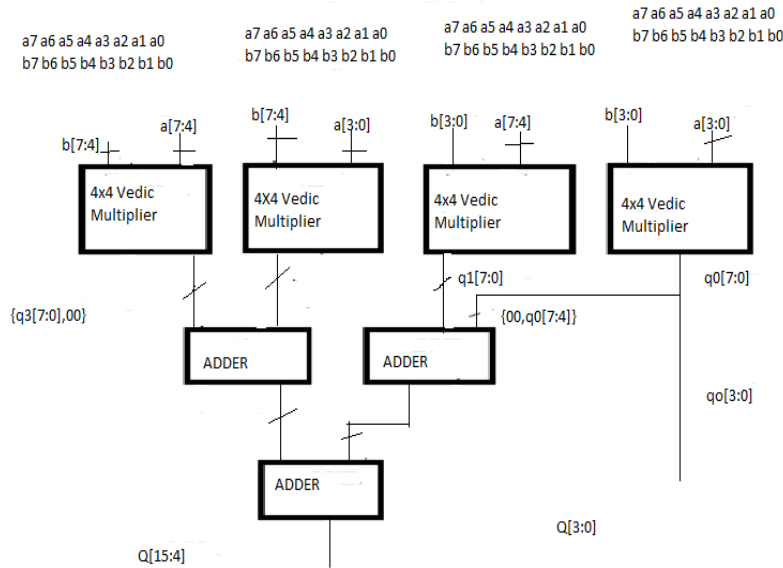


Figure 6. 8x8 Vedic Multiplier

8 bit Vedic multiplier is implemented by using four 4x4 multiplier, also 8bit and 12 bit adder is used. The block diagram of 8x8 Vedic multiplier is shown in above Figure 6.

3.4 16X16 Vedic multiplier

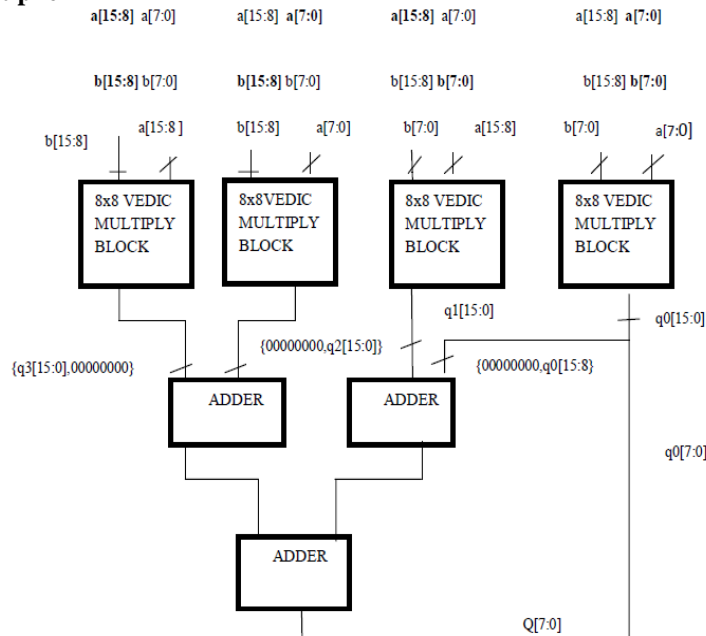


Figure7.16x16 bit Vedic Multiplier

16 bit Vedic multiplier is implemented by using four 8x8 multiplier, also 12 bit and 24 bit adder is used. The block diagram of 16x16 Vedic multiplier in above Figure 7.

III. Vedic Division

A lot division technique was developed in order to reduce the latency, area and number of iteration in the division circuit. A new method was implemented in which division operation is done easily by Vedic

division. Paravartya –Yojayet method is used which means ‘Transpose and apply’. This method is implemented by using multiplication and division operation, in order to reduce the delay and power dissipation.

4.1 Analysis of Vedic Division

Paravartya method helps to minimize the optimization, latency, accuracy, as well as iteration step can be reduced. This sutra is used only for division of decimal number. Thus it is necessary to have basic knowledge of division of decimal number using this method.

4.2 Division algorithm

According to this algorithm the digit of the divisor is complemented except the MSB. Then the complemented digit is multiplied with the sum of each column of the dividend followed by addition of each digit of the column. Then the last result obtained is the quotient and remainder. Consider an example where dividend is 13650 and divisor is 123. So using this methodology iteration is reduced to 8. Figure 8. shows an example for division of two number.

Divisor	Dividend
1 2 3	1 3 6 5 0
-2 -3	-2 -3
	-2 -3
	-2 -3
	1 1 1 0 -3
	Q=111 123-03=120

Figure 8. Vedic division of two number

4.3 Crumb encoding

Crumb encoding is done by using 2 bit to represent single crumb. The first bit is the sign bit and second bit is value bit. If sign bit is 0 then it is considered as positive or negative. Table 1 gives the analysis of the crumb encoding.

Table 1. Analysis Of Crumb

Divisor	Ds	Dv	Crumb encoding
0	0	0	00
1	0	1	01
-1	1	1	11

Figure 9. shows an example for Modified Vedic division of 8 bit dividend and 4 bit divisor. In this example LSB of the divisor crumb is complemented and then it is partially multiplied with dividend. Quotient is obtained by most significant bit and the remainder is obtained from remaining three bit from final result.

01 00 01 01	01 00 00 01 00 00 01 01
00 11 11	00 11 11
	00 00 00
	00 01 01
	00 00 00
	00 11 11
	01 00 11 00 01 01 00 00
	q=10001-00100
	Q=01101 R=100

Figure 9. Modified Vedic division

Modified Vedic division is split into three steps: Partial multiplication is complimented into divisor crumb. Second the algorithm for division is designed using addition and partial multiplication. Last step is the quotient is decoded into bits. Modified Vedic architecture is shown in Figure10.

1. Bitwise XOR operation is done for all the bits of divisor crumb except the MSB.Using XOR logic 01 is converted into 11,00 will be same and MSB will be same.
2. 2x2 partial multiplier and 2 bit adder is used.

The result of the addition is used as one of the multiplicand for further partial multiplication. The input for the 1st adder is 2 and for 2nd adder is 3 and is increased till 4 for 8 by 4 bit division. It can be also called as M and N bit division.

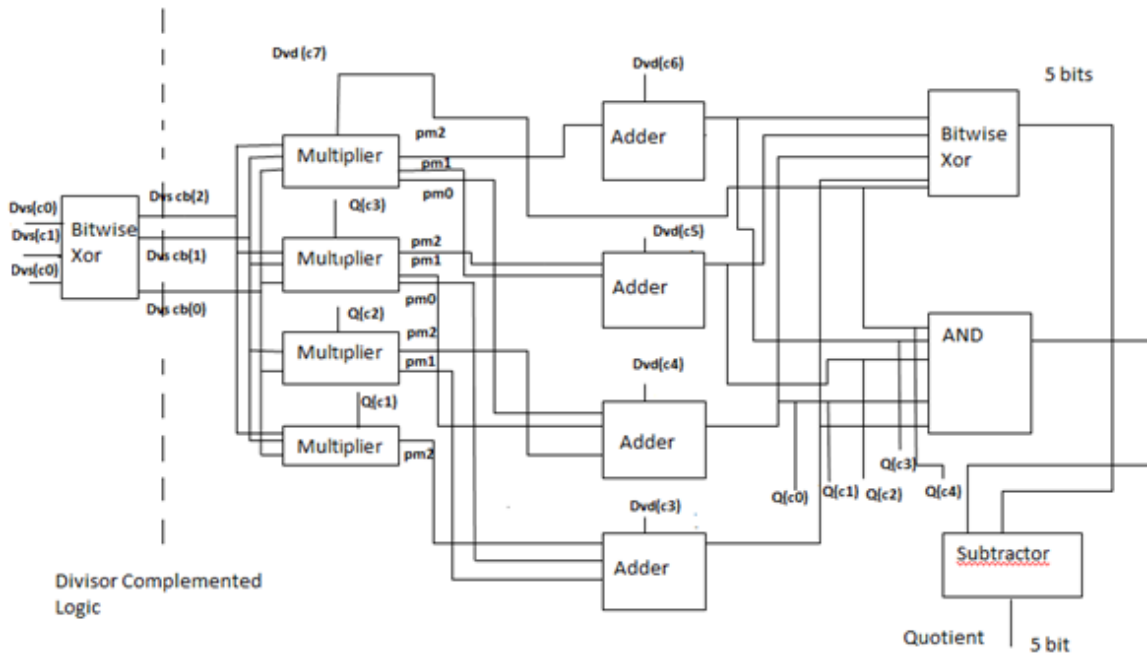


Figure 10. Modified Vedic architecture

IV. Radix-4 Modified Booth Multiplier

Modified Booth Multiplier is used in order to obtain fast multiplication. Booth multiplication can be used for faster and smaller multiplication circuits. Instead of adding and shifting the each column of the multiplier and the multiplying it by 0 or 1 directly multiply it by $\pm 1, \pm 2, 0$ to obtain the result. Grouping is based on starting from Least significant bit and two bit from the first block of the multiplier. Figure 11 shows multiplier bit used for booth encoding.

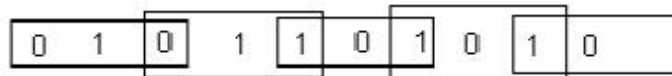


Figure 11. Group of multiplier bit used for booth encoding

The block is decoded in order to obtain correct partial product. The modified booth algorithm generates signed bits -2,-1,0,+1,+2 for encoding of the multiplier Y. Each encoded digit in the multiplier executes a certain operation on the multiplicand X as shown in Table 2.

Table 2. Coding Table

Block	Re-coded digit	Operation on X
000	0	0x
001	+1	+1x
010	+1	+1X
011	+2	+2X
100	-2	-2X
101	-1	-1X
110	-1	-1X
111	0	0

For partial product Radix-4 Modified Booth multiplier is used to reduce the number of partial products for roughly one half. Kogge stone adder is used by which delay power consumption can be reduced .

V. Implementation And Results

The stimulation results is obtained for the implemented design:

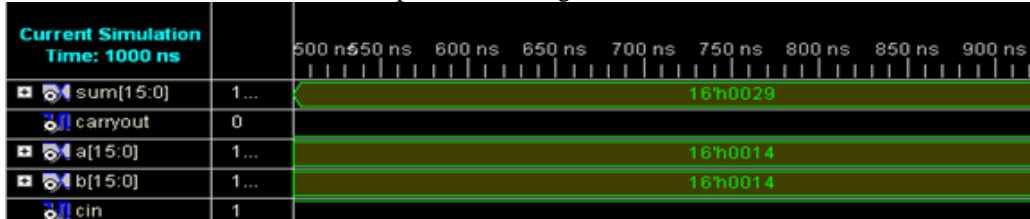


Figure12. 16 bit Kogge Stone adder

Figure 12 shows the stimulation result of 16 bit Kogge Stone adder where two 16 bit number is added to obtain the result and carry is stored in carryout.

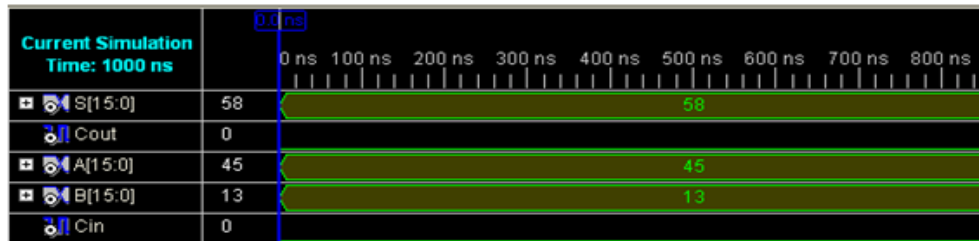


Figure 13. 16 bit Brent Kung adder

Figure 13 shows the stimulation result of 16 bit Brent Kung adder where two 16 bit number is added to obtain the result and carry is stored in carryout.

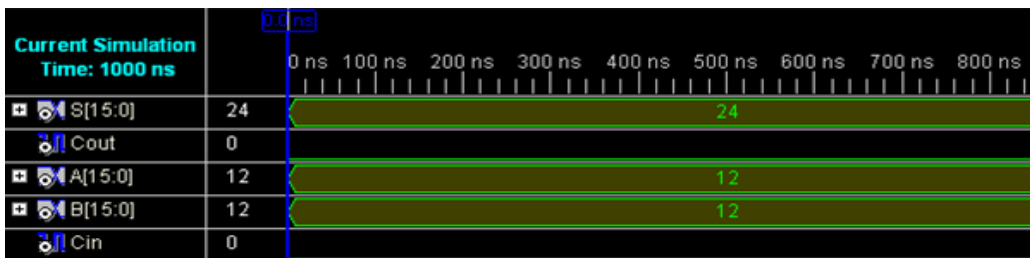


Figure 14. 16 bit Ladner Fischer adder

Figure 14 shows the stimulation result of 16 bit Ladner Fischer adder where two 16 bit number is added to obtain the result and carry is stored in carryout.

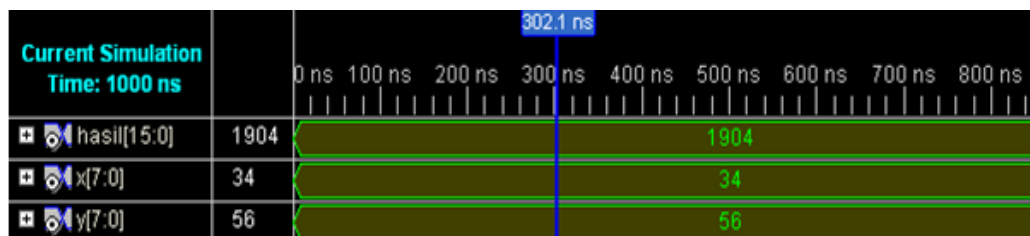


Figure15. Modified Booth multiplier

Figure 15 shows the stimulation result of Modified Booth multiplier where two 8 bit number is multiplied to obtain the product.

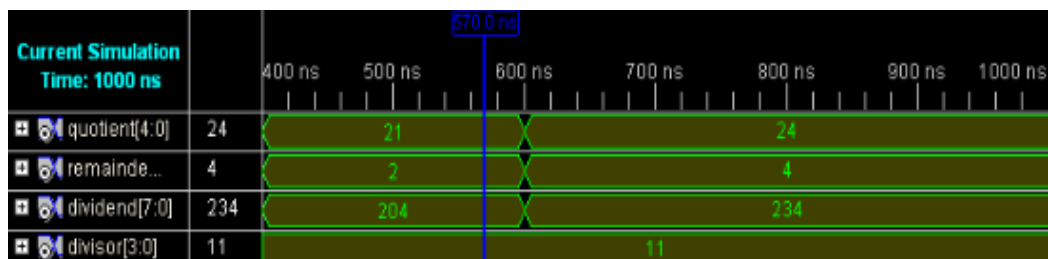


Figure16. 8 bit Vedic division

Figure 16 shows the stimulation result of 8 bit Vedic division where two 8 bit number is divided to obtain the quotient and remainder.

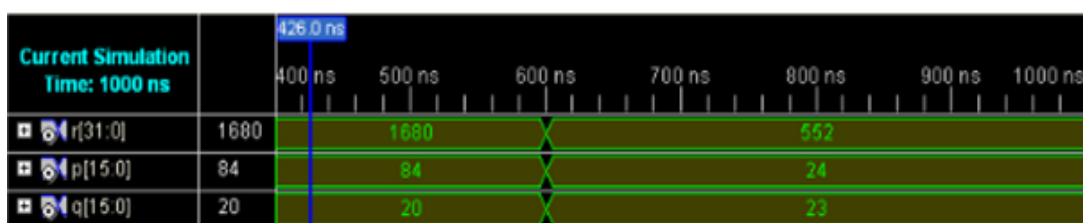


Figure 17. 16 bit Vedic Multiplier

Figure 17 shows the stimulation result of 16 bit Vedic Multiplier where two 16 bit number is multiplied to obtain the product.

Table 3. Design Summary of Adderes,Vedic multiplier,Vedic division,Modified Booth multiplier

	Kogge Stone adder	Brent Kung adder	Ladner Fischer adder	8-bit Vedic division	16-bit Vedic multiplier	Radix-4 Modified Booth Multiplier
No of Slices	35	23	22	36	63	148
No of LUT	69	40	38	64	121	263
No of IOB	75%	75%	75%	38%	75%	48%
Delay	9.566ns	16.440	16.447ns	15.67ns	29.004ns	15.795ns
Power	34mW	34mW	34mW	56mW	34mW	34mW

In TABLE 3 The comparison of adders vedic multiplier,vedic division and Modified Booth multiplier is shown where LUT,IOB,delay power is shown .According to this table kogge stone adder has less delay compared to other two adders.In 8 bit Vedic division it has delay of 15.67ns.

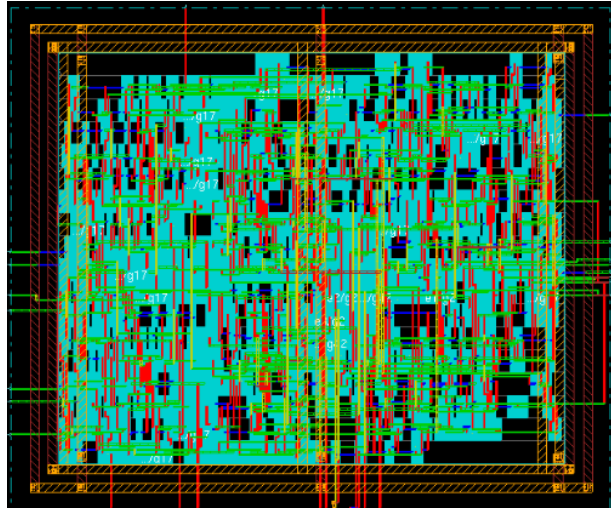


Figure 18.Physical layout of Modified Booth multiplier

In Figure 18 Physical layout of Modified Booth multiplier is shown.

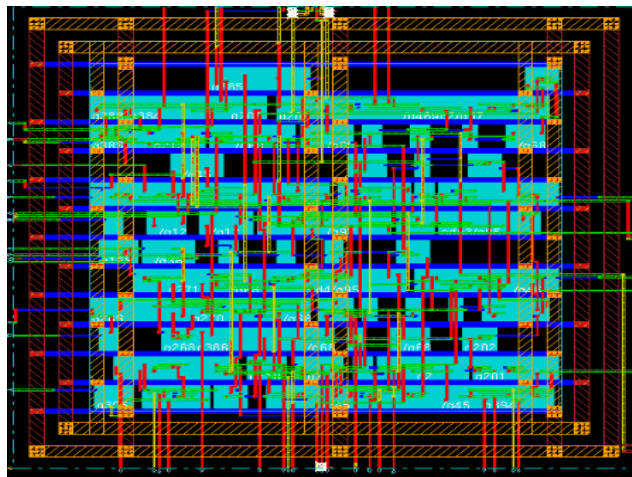


Figure 19.Physical layout of Vedic divider

In Figure 19 Physical layout of 8 bit Vedic division is shown.

VI. CONCLUSION

Depending on LUT Ladner Fischer has less area, and Ladner Fischer has less No of Slices, when comparing the delay Kogge Stone has less delay. In Vedic division when compared to the previous paper it has less delay of 15.67ns compared to other normal division method. Modified Booth multiplier has less delay in radix-4 when compared to radix-8 because Kogge stone adder is used. Vedic Multiplier has less area and delay when other multiplier is used.

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