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An Efficient VLSI Implementation of CDF 5/3 Architecture on FPGA For Image Processing Applications.

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Abstract: *Image Compression is basically defined as reducing the size of image without altering the picture quality of the original image. Various algorithms are currently available for compression of the images, among them the most prominent algorithms the wavelet transform. In recent technology Wavelet transform is named as cutting-edge technology for image processing applications. Discrete cosine transform (DCT) was previously used to compress the image. Due to the drawback of DCT i.e lower compression ratios and blocking artifacts we go for Wavelet transform which has higher compression ratios and PSNR compared to other compression algorithms. There are various types of Wavelets available. These wavelets can be broadly classified as lossy and lossless compression. Majority of Wavelets are lossy in nature. Only CDF 5/3 Wavelet transform is lossless in nature. Hence image processing application that is concerned on accuracy of the image can go for CDF 5/3 Wavelet transform. The proposed technique in this paper has efficient hardware architecture; the hardware is made simpler by eliminating the multipliers which was present in the existing system and replacing it with shifters. Also use of shifters in proposed system increases the frequency of operation of both 1D-DWT and 2D-DWT and also area is drastically reduced.*

Keywords: *CDF, DWT, LUT, DCT etc.,*

I. Introduction

Compression of images allows us to store image in available memory. It also minimizes the transmission time required to transmit images over the internet. Various methods are available for compression of images. For Internet use, the two most popular compressed graphic image formats are the JPEG format and the GIF format. The JPEG method is commonly used for photographs, while the GIF method is popularly used for line art and images in which geometric shapes are basically simple. Various techniques are available for image compression. Other popularly used are fractals and wavelets. Without introducing errors a text file can be compressed, but only up to a particular extent. This is called lossless *compression*. Beyond this point, errors are introduced. During compression of images, a minute loss in picture quality is usually unnoticeable. The discrete wavelet transform (DWT) is one of the most prominent techniques used for analysis of signal and image processing applications. Previously used Fourier transform doesn't have property of temporal resolution. Due to this drawback in Fourier transform we go for discrete wavelet transform (DWT) that has a capacity to operate in multiresolution signal analysis [1]. The DWT has well time–frequency characteristics compared to other transform techniques; JPEG 2000 previously used Discrete Cosine Transform (DCT) for compression of images, due to its low compression ratios currently JPEG 2000 uses DWT for image compression.

II. Proposed 1d And 2d-Dwt Architecture

The proposed 5/3 DWT is separable i.e. we can divide total 2D-DWT architecture into two separate 1D-DWT block as row processor and column processor. The proposed 1D and 2D-DWT is described below.

i) 1D-DWT

The basic block diagram of proposed 1D-DWT is shown in Fig. 1. The total 1D-DWT block is built by six shifters, five adder/subtractor, one FIFO and one clock divider. The clock divider mainly used to make decimation block. The down sampling will be done by clock divider, hence giving a compressed image at the output. The latency of 1D-DWT block is 4-clock cycle. In case of low pass filter five input samples are given with the delay. The figure 1 shows the proposed diagram of low pass filter. Here the first five input samples are given as input later left shift by one and two operation is done based on mathematical equations. The following outputs are then added and left shifted by three and passed to D-FF. The clock divider helps in down sampling the output samples using D-ff. Samething is done in case of HPF.

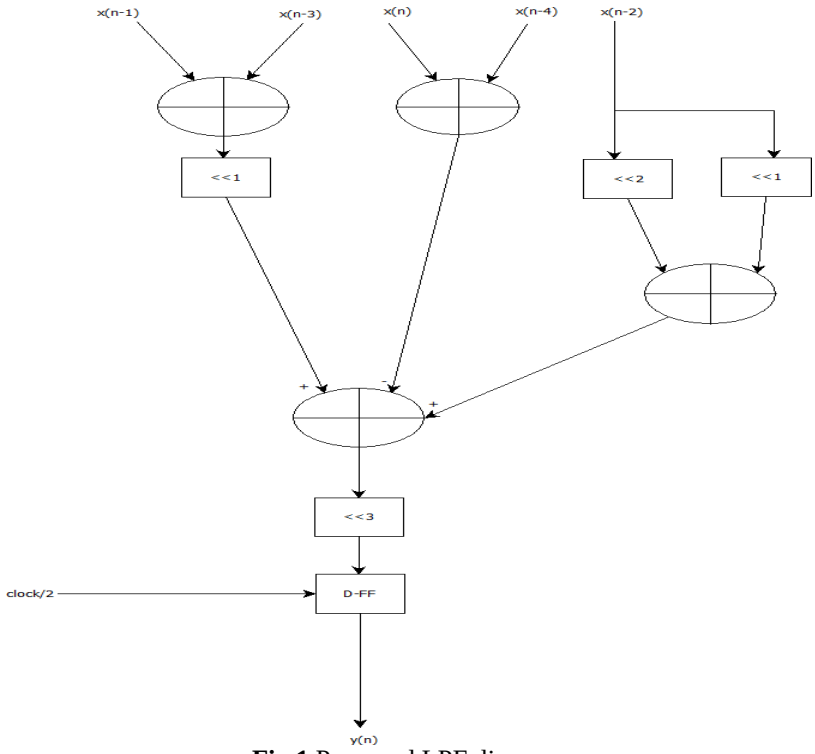

Fig 1 Proposed LPF diagram

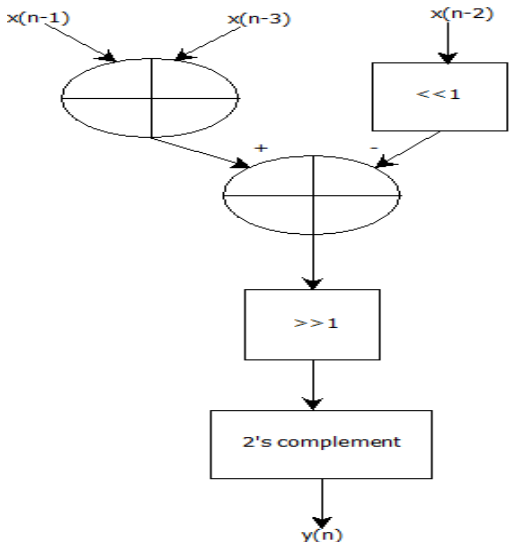

Fig 2. Proposed HPF diagram

ii). 2D-DWT

The 1D-DWT architecture is designed using 2D-DWT architecture along with memory units and controller units as shown in Fig. 2. The LPF and HPF coefficients from the 1D-DWT Block-1 are stored in parallel in the two inside memory block of 2D DWT architecture. Further these coefficients are processed at a time in parallel by using both 1D-DWT Block-1 and 1D-DWT Block-2 to obtain sub-bands of *LL, LH, HL, and HH* through multiplexer and Demultiplexer. The 1D-DWT Block-1 is used to obtain *HL* and *HH* sub-bands and 1D-DWT Block-2 is used to obtain *LL* and *LH* sub-bands. The controller unit is used to synchronization purpose of various blocks. The 2D-DWT architecture has high speed due to parallel processing of all sub-blocks compared to existing techniques.

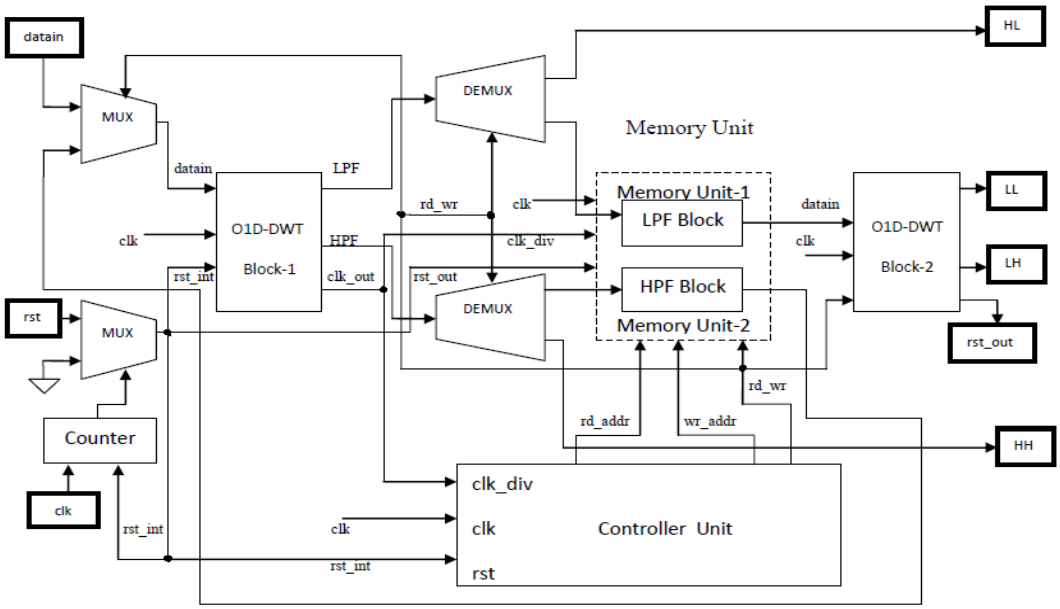

Fig. 3: Proposed 2D-DWT Architecture

III. Mathematical Formulation Of Dwt

The basic lifting schemes equations for cdf 5/3 are given by equations (1) and (2)

Y [2n+1] =x [2n+1]-[(x [2n] +x [2n+2])/2] **(1)**

Y [2n] =x [2n] +[y [2n-1] +y [2n+1]] **(2)**

The above equations on simplification we get the co-efficient for LPF and HPF:

Low pass filter= {-1/8, 2/8, 6/8, 2/8, -1/8}

High pass filter= {-1/2, 1, -1/2}

Proposed Equations for 1D-DWT Low Pass Filter:

$Y(n)=\{(-1/8\ x(n))+(2/8\ x(n-1))+(6/8\ x(n-2))+(2/8\ x(n-3))-(1/8\ x(n-4))\}$

On simplications we get,

$Y(n)=1/2^3[2^1\{x(n-1)+x(n-3)\}-\{x(n)+x(n-4)\}+(2^2+2^1)x(n-2)]$ **(3)**

Proposed Equations for 1D-DWT High Pass Filter:

$Y(n) = \{(-1/2\ x\ (n-1) +x\ (n-2)-(1/2\ x\ (n-3))\}$

On simplications we get,

$Y(n) = -1/2[x\ (n-1) +x\ (n-3)-2^1x\ (n-2)]$ **(4)**

IV. Results & Discussions

i). 1D-DWT:

The comparison of various 1D-DWT architecture is given in Table 1. The frequency of proposed architecture is much higher than existing [5, 6, and 11].

Table 1: Comparisons of 1D-DWT Architecture:

Parameters	Husain et al., [5]	Sowmya et al., [6]	Shriram Hegde., [11]	Proposed
No. of Slice Registers	373	823	53	40
No. of Flip Flops	------	634	85	18
No. of Multipliers	0	2	1	0
Frequency (MHz)	64	133.786	317	644.345

ii). 2D-DWT:

The comparison of various 2D-DWT architectures is given in Table 2. The frequency of proposed architecture is higher than existing with less area utilization.

Table 2: Comparison of Various 2D-DWT Architecture:

Parameters	Naseer and Mustafa., [7]	Shriram Hegde., [11]	Proposed
No. of Slice Registers	1299	422	301
No. of Flip Flops	767	235	301
Frequency (MHz)	62.797	181.283	273.149

The proposed 2D Dwt is implemented on Spartan 6 LX45 FPGA board using system generator as shown in Fig. 3. The 2D image id converted to 1D using frame serialization and applied to FPGA and the outputs are de-serialized and converted again from 1D to 2D to display the output compressed image.

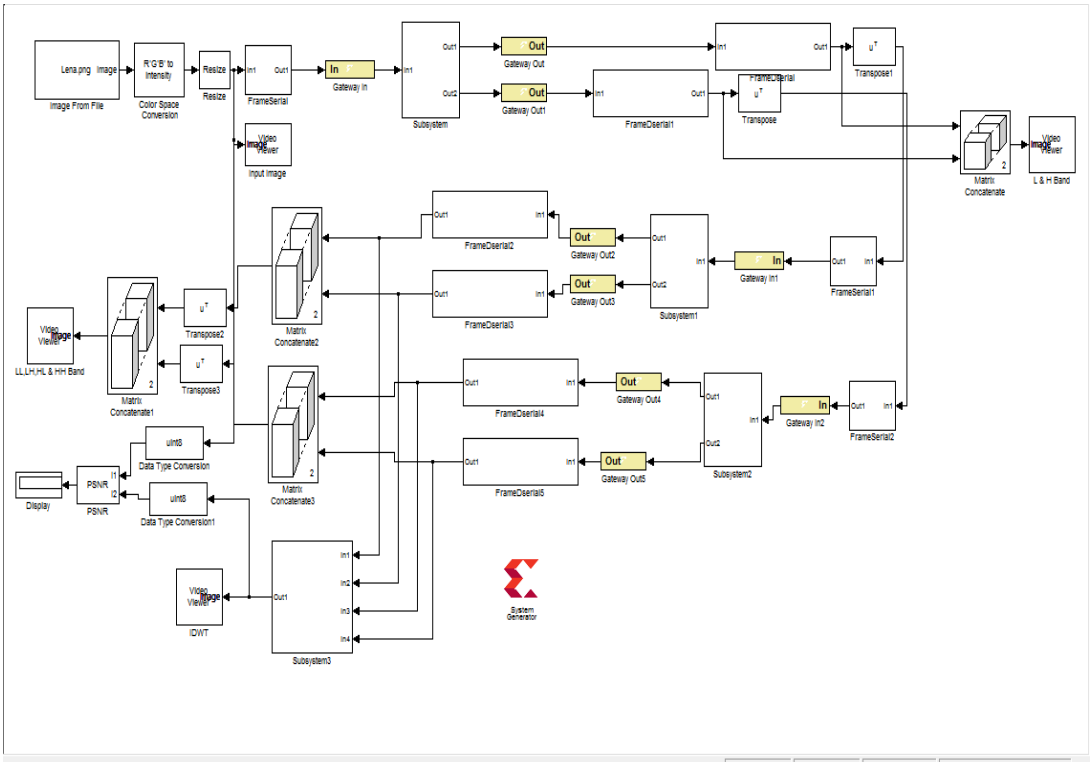

Fig 4. The software model design using system generator

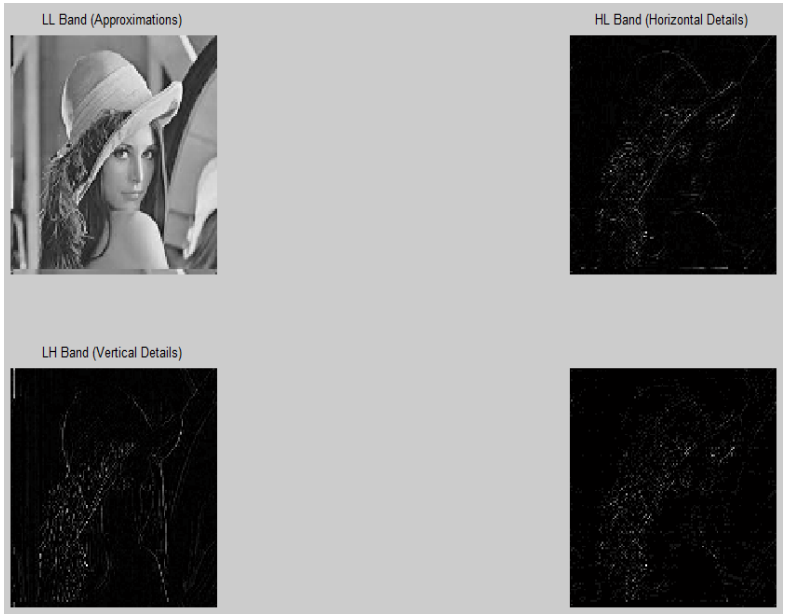

Fig 5. Output of software model with output as LL, LH, HL, HH bands

V. Conclusion

In this paper, we propose an efficient architecture for lifting based 5/3 DWT on FPGA. The proposed 1D-DWT is designed and used to design efficient 2D lift based DWT. The 2D lift 5/3 is further implemented on FPGA board to test the parameters such as LUT's, slices and delays. It is observed that the proposed architecture is better compared to existing architectures.

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