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PID Implementation on FPGA for Motion Control in DC Motor Using VHDL

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Abstract : *this paper presents the implementation of a proportional-integral-Derivative (PID) controller for motion control of a DC motor based on FPGA. This implementation technique used to avoid the problems which create during analog and digital interfacing system in real-time.the controller used in speed controller loop. The hardware implementation has been done on a Xilinx Spartan 3 FPGA chip and generates the PWM signal as an input of motor driver for controlling. The out of optically encoded data is decoded and give it to PID control loop. Proposed implementation is present through the VHDL algorithm*
Keywords: *PID controller, USB-6008, DC motor, FPGA, Xilinx Spartan 3.*

I. Introduction

The new and effective technology, theories and design methodologies are being continuously development in the control field reduce the coast even after it is not susceptible to environmental noise and very easy to re-configurable so that digital control system have become most popular. Field Programmable Gate Array (FPGA) has been selected .As there are many useful methods and tools that are available in FPGA. These are used for the remodelling of dedicated and reconfigurable hardware which use complex digital circuits at the wafer level. With the help of FPGA we can able to develop a circuit in digital form that involves high division of complexity. Due to this, FPGA technology is utilized so that to build up a digital circuit so to get an efficient, flexible and fast control system. Some errors which are related to the digital controller are quantization error, differential linearity error (DNE), integral linearity error (INE). This can be recovered by using embedded systems that are efficient to use in terms of the chip area, flexibility, speed and cost minimization. Therefore some hardware based solution implementation suitable for where the digital circuit is responsible for operation of specific application.

II. Literature Review

From the Observation most of the paper mentioned the different way controlling the system with efficient, flexible and good accuracy output. In [1-9] reports mainly engross on various ways to discern the system which is efficient, flexible .In [6], To curtail the calculation load of NURBS interpolation, a interpolation form encompassing two level is used. Parallel working of PC and FPGA system is subsumed ,whereas in [1], To find out the system uncertainties in the LIM, an modification method has been applied, is reliant on the FPGA only. In [7] to adjust the velocity of PMS drive, an FPGA supported adaptive controller with fuzzy technique is utilized. In this work employing a controller that is of digital form gives a adaptable way of introducing the digital controllers in system controlling motion effect that is permitted to be custom built and yet be adaptable for future requirements. In [9] reports implementation of PWM on FPGA, design & implementation of PWM on FPGA using HDL. In this work employing hardware description language (VHDL) and implementing it on FPGA because FPGA can process information faster, controller architecture, hardware flexibility, design reuse also explained the gradual building of modules towards implementing the DC Motor control application. This control loop is implemented on FPGA platform for VHDL beginner.

III. Proposed System Design And Methodology

3.1 Block Diagram Of Complete System:

The figure 1 shows the objective of this paper reviewed in bock diagram. In this, set point or reference signal is the preferred rapidity of the plant that is DC motor. This reference signal is transfer to detector. Detector is used to determine the difference among selected value input and the value of feedback element. At end stage it helps us to get the true estimated value or approximated value that is somewhat similar to selected value. Output of the error detector is feed to the PLL input. PLL is used here for generation of clock signals. In this project we use the controller as PID. The output of error detector is give to input of the controller. Output of error detector is the deviation among the reference signal and feedback element obtained that actuates the regulator elements. The control elements change the conditions in the plant so as to reduce the original error.

PWM generator is used in the controller to produce the PWM waveform which will be the input to the system which in this case is a DC motor.

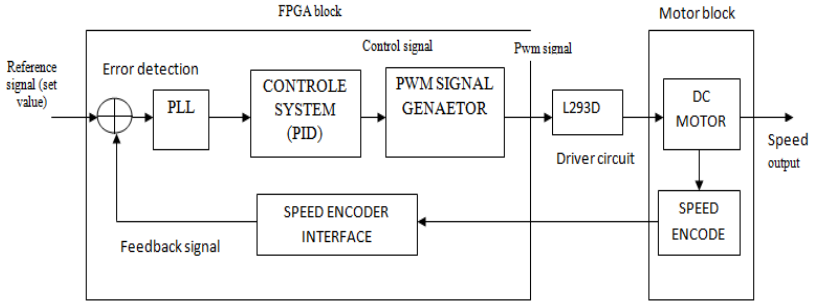


Fig 1. Complete system Block diagram

3.2 Modeling of the Dc Motor

The motor's mathematical model can be given as:
The voltage of the armature V_a has the following parameters:

$$E_b(s) + I_a(s)\,[R_a + s\,L_a] = V_a(s) \quad (1)$$

Now for a motor with PMDC,

$$T(s) = I_a(s)\,K_t \quad (2)$$

The motor's back emf can be defined as

$$E_b(s) = K_b s\theta(s) \quad (3)$$

The motor's mechanical model can be given as:

$$J\frac{d^2\theta}{dt} + B\frac{d\theta}{dt} = \tau(t) \quad (4)$$

$$T(s) = \theta(s)[Js + B] \quad (5)$$

$$I_a(s) = \frac{s[Js+B]}{K_t}\,\theta(s) \quad (6)$$

Placing (6) & (3) equations in (2) provides,

$$\frac{\theta(s)}{V(s)} = \frac{K_t}{s[(Js+B)(sL_a+R_a)+K_tK_b]} \quad (7)$$

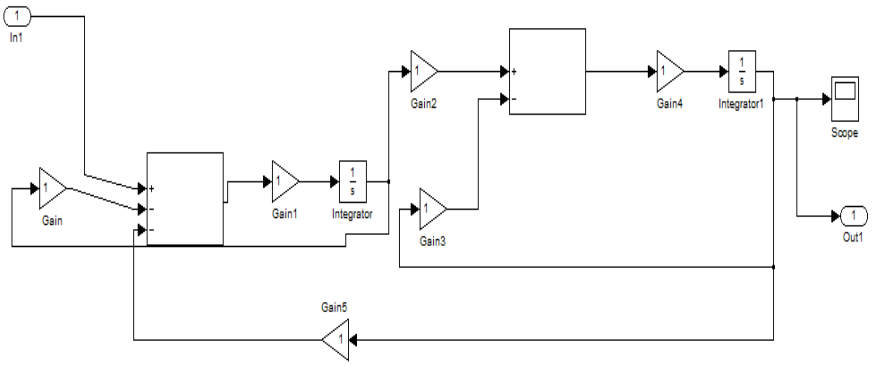


Fig 2. Pant model

The plant model has been given in Fig. 2. The motor output is encoded by using IR LED based speed encoder.The motor speed data has been obtained from the rate of pulses of the encoder. Figure 3 and figure 4shows the output of the plant model when it is in open loop and close loop.

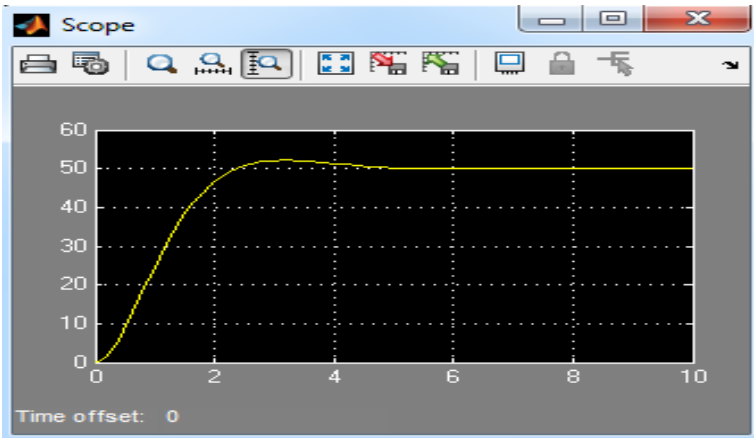


Fig 3. Unit step response of closed loop plant model

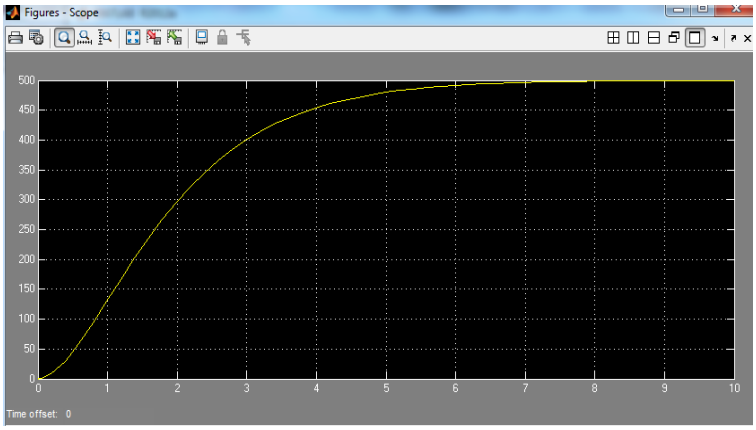


Fig 4. Unit step response of open loop plant model

3.3 Design of the Controller:

The PID based controller performs its operation very easy and simple manner like proportional, integral and derivative action in control system. This controller is in cascaded position form used in velocity and current loop to get flexibility and efficient dynamic and static response. The mathematical model of PID controller with respect to error e(t) is.

$$U(t) = K_p e(t) + K_i \int e(t)\,dt + K_d\left(\frac{d\,e(t)}{dt}\right) \quad (8)$$

$$U(s) = E(s)\left[K_p + \frac{K_i}{s} + s\,k_d\right] \quad (9)$$

P is used to determine the present error, I is used to know the accumulation of past errors, and future errors are predicated by D, based on current rate of change. We can tune the PID controller by using various methods but here the proportional (), integral (k_i) and derivative (k_d) gain are obtained from simulink PID tuner and system step response. The step response of tuned system as shown in figure 4. The controller has been designed with a filter and trapezoidal integral algorithm.

3.2 Pwm Signal Generator:

PWM is a technique to provide a logic "1" and logic "0" for a controlled period of time. It is a signal source involves the modulation of its duty cycle. Pulse Width Modulation is a very popular technique for delivering power to any circuit in a very precise and controlled manner. The above figure shows the block diagram of the PWM generator .the PWM contain N-bite data ward as a input .Corresponding to the actual PWM duty cycle. The register stores the input (set value). When load input is high then register gives the input

to output then this register output is compare with N-bite counter value by using comparator .when these two value become equal the comparator output is used to reset the R/S latch output. when counter overflows then load signal is high and latch output is set to high.

The duty cycle is given from the following equation:

$$Duty\ cyce = Data\frac{value}{2^N}$$

Where, Data Value is the N-bit input data value.

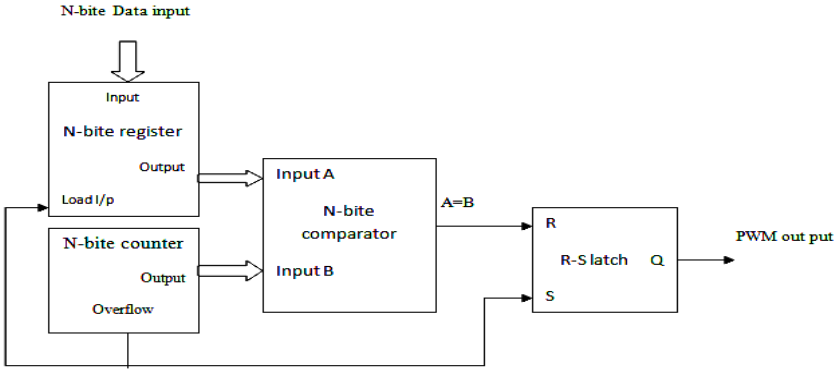


Fig 5. PWM pulse generator

3.4 Dc Motor Driver Circuit And Encoding:

Output of the PWM generator is given to the L293D Quadruple Half driver circuit for drive the dc motor. PWM output signal is a function of reference signal and it is used regulate the speed of the motor. The ON period of the PWM decides the motor ON period and the average voltage decides the speed of the motor. The IR LED based speed encoder generates the pulse depending upon the rotation of the motor. The speed encoder is made up of the wheel with N-holes. So that IR transmitter/receiver LED generates N-pulse per one revolution of the motor. This IR LED based sped encoder interface to FPGA and calculate the error signal and sampled by using system clock rate. One important factor is found in sped encoder pulse is noise at the edges due to the wobbling of encoded wheel so produces false counting of the sampled speed. So avoid such problem we us the debounce logic was introduced.

3.5 Phase Locked Loop:

PLL is a feedback system that indicates a VCO, Phase detector and low pass filter with in a loop. In my project PLL is used for clock generation application. When two inputs has same frequency and loop is locked then we get the output frequency twice of input frequency with cosine phase difference. Doubled frequency can eliminate by using low pass filter and phase difference is removed by VCO control tune value.

3.5 Error Signal:

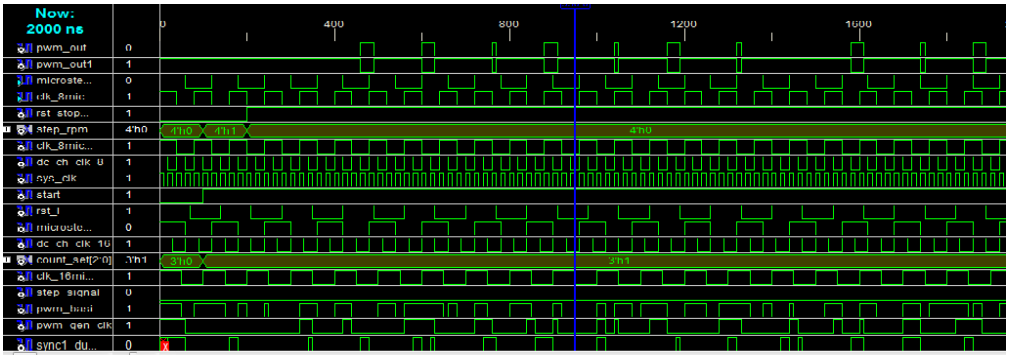
Error signal is generated by comparing the feedback value that is from encoded value with reference value. Actually here number of encoded pulse is converted hex decimal value with respect to PWM then subtract with set value the feed to PID controller as a input. If IR based speed encoder having N number of holes in a wheel so it generates N pulse in a one Revolution of the motor.

IV. Implementation And Result Details

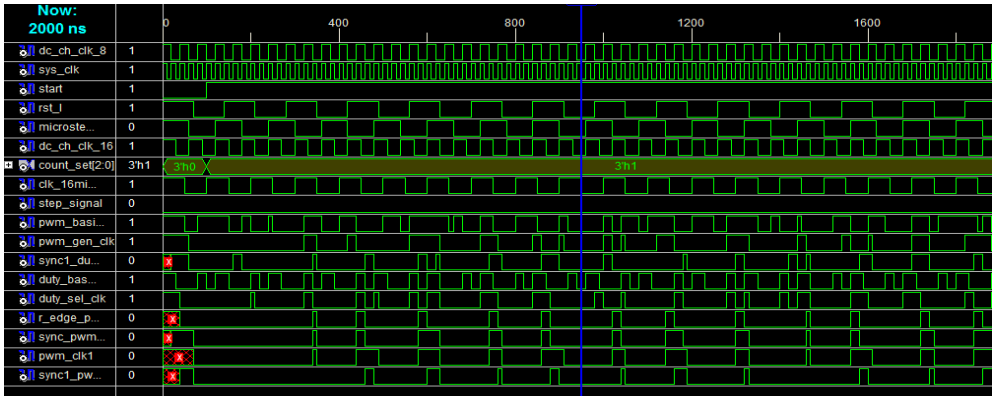
The proposed system is designed using Xilinx 9.1i design suite and its implemented in Spartan xc3s400-4tq144. The language used here is VHDL. Design utilization summary is shown in Table.1the proposed system simulation results as follows. The simulation shows control PWM output as shown in figure 8 (a) & (b).In this project controller operation was implemented in a Xilinx Spartan 3 FPGA , Control system modules includes controller, PLL, PWM generator, comparator, and encoder interface module. First connect supply to board and connect USB cable to laptop and to board then compile the code, assign the pins, select JTAG programming mode and download the program in to target device. Inputs are given feed through the switches present on FPGA board and we can observe the speed of the DC motor.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	262	4,896	5%	
Number used as Flip Flops	252			
Number used as Latches	10			
Number of 4 input LUTs	385	4,896	7%	
Logic Distribution				
Number of occupied Slices	336	2,448	13%	
Number of Slices containing only related logic	336	336	100%	
Number of Slices containing unrelated logic	0	336	0%	
Total Number of 4 input LUTs	392	4,896	8%	
Number used as logic	385			
Number used as a route-thru	7			

Table .1 Design utilization Summary



(a)



(b)

Figure 6 (a) & (b) shows the simulation output of the PWM. This signal is given to motor driver

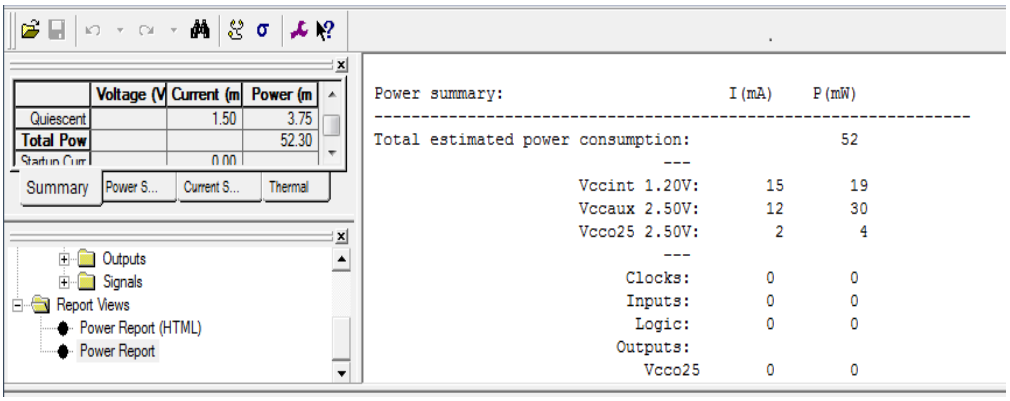


Fig 7. Power analysis of complete model. When compare to simple method used for motion control this method means PID controlling produce less power dissipation

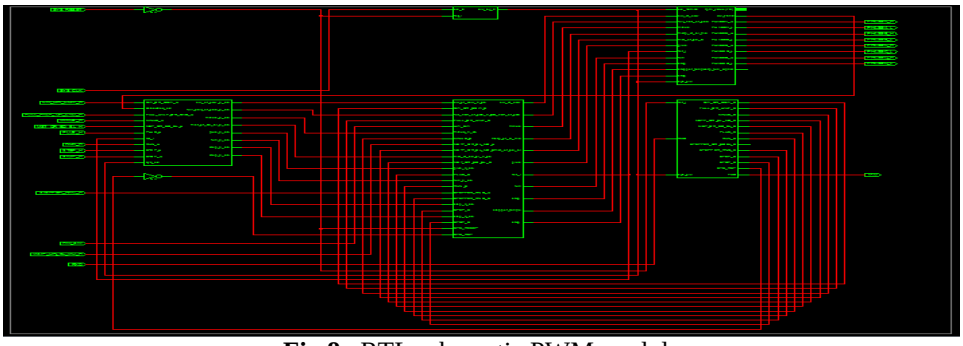


Fig 8. RTL schematic PWM module

V. Conclusions

The simulated waveform presented in the paper shows VHDL implementation of PID controller for motion control and the debounce logic control in order to reduce the wobbling of the encoder wheel. The design is synthesized using Xilinx 9.1i design suite and implemented in Spartan xc3s400-tq144.

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