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FPGA Based Prototype Designing of SOC for Vehicle

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Abstract: *Now a days the use of vehicle is increasing rapidly. The vehicle is a complex system having different controlling parameters such as wiper control, ventilation control etc. Many systems has been designed for controlling this parameters with different controllers. The system becomes bulky if different circuiteries are used for different controlling parameters. But the need of the hour is high performance with nano design. So to achive all these requirments SOC is designed.SOC is a Complete system which is able to achive all the requirments of the user on a single chip. This paper presents the design and implementation of SOC for vehicle which controls the parameters such as wiper and ventilation. The system proposed here is the integration of controller, memory, and I/O ports. This system is also responsible for detecting fluctuation in parameter and controling it. The system becomes efficient and user friendly as one single system is able to control the different functions. Xilinx is used for designing the complete system and ISE simulator is used for simulation purpose. This designed system is implemented on FPGA for testing the functionality of the system.*

Keyword: *FPGA (* Field Programmable Gate Array*), ISE* (**I**ntegrated **S**ynthesis **E**nvironment simulator), *SOC(*System On Chip*).*

I. Introduction

"System-on-chip is an incorporation of approximately all components of a computer into a single integrated circuit (chip)". The system on chip is useful in various ways as it utilizes less power. The design can be made at very small size, the system works with great accuracy. The cost of gate is also very less. As all the modules are present on the single chip the operating time of the system is also very less. The design of the system is also highly secure.

This design of SOC consist of Memory, controller, Shift registers and I/O ports. The memory block is designed here for storing data. The comparator is designed here for controlling the parameter. The data input is applied to the shift register. The designed shift register is serial in parallel out shift register.

FPGA (Field Programmable Gate Array) spartan6 is used for implementing the designed system. Input signals to the system are applied by FPGA kit. Fig.5 shows the implementation result.

II. SOC Design Methodology

1. The prototype schematic of the proposed system will be designed in RTL logic in Xilinx.
2. The designed circuit will be implemented and tested on FPGA kit.
3. After implementation the circuit operation will be verified for the operation such as ventilation and wiper control.

III. Literature Review

V. Usha Rani, et.all[1], Here the author proposed PIC microcontroller based module that controls the ventilation process autonomously as the vehicle can be utilize comfortably.

Fazel Elahi et. al[2],The author developed a microcontroller based Windshield controller .The dust sensor and sun visor are also present here to clear the dust on the screen and to protect the driver from direct sunlight respectively.

Mukul Joshi,et.al[3],The system proposed here is to control the wiper. The moment of wiper depends on electrical and mathematical model of sensors. A PIC microcontroller based system design here obtains motor speed variation depending on the sensors output.

Rajesvari.R1, et.al [4], In this paper the author developed a telecommand system on chip, in order to send signal from base station to the space. VHDL code is used to develop a system on chip. The system is implemented on FPGA kit.

Mr. TR. Parthasarthy [5] et.al In this paper on performance characteristic the partitioning between ARM and FPGA is discussed.

Dae Geun Lee, et.al [6] Here using system on chip designing technique embedded controller for car black box is designed. The car black box designed here collects various information related to vehicle so one can easily detect the location of vehicle after accident.

Huang Jin et .al [7],Here author developed the module for DRAM and implemented it on FPGA kit.

IV. Research Methodology

4.1 Design Of Memory

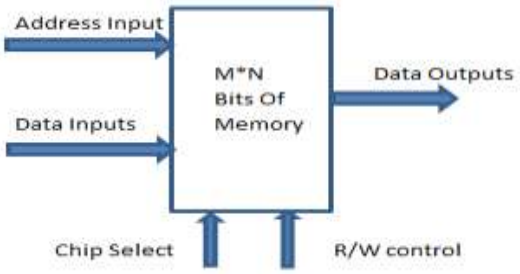

Fig.1 Basic block diagram of memory

The basic element of semiconductor memory is a flip flop. The information is stored in a binary form. There are a number of memory locations in a memory chip, each location being meant for one word of digital information. The size of memory chip is specified by two numbers M and N as M*N bits. The number M specifies the number of locations available in the memory and N is the number of bits at each locations. i.e M words of N bits each can be stored in the memory.

Fig.1 shows the block diagram of memory. Each of the M locations of the memory is defined by a unique address. For accessing any one of the M locations, P inputs are required, where $2^P = M$. This set of lines are referred to as address inputs or address bus. The address is specified in the binary form. The address input is applied to a P to M decoder circuit, which activates one of the M outputs depending on the address and ,thus, the desired memory location is selected.

The number of inputs required to store the data into or read the data from any memory location is N. One set of N lines is required for storing the data into the memory, referred to as Data inputs and another set of N lines is required for reading the data already stored in the memory, which is referred to as data outputs..

A number of control inputs are required to give commands to the device to perform the desired operation. Command signal R/W is required to tell the memory whether a read or write operation is desired. When W/R bar is high the data bus is used for writing the memory and when W/R bar is low the bus act as the output bus for reading the data from the memory. Commands such as Chip enable(CE),Chip select(CS) are also available.

To write a word into the selected memory location requires logic 1 voltage to be applied to CS and write terminal . After that the word to be stored is applied to the data input terminals. Then the address of the desired memory location is applied to the address input terminals. A write command signal is applied to the write control input terminal.

To read the contents of the selected memory location ,the write input and CS inputs must be at logic 1. And logic 0 is applied to the read input terminal. At first the chip select terminal is applied to the CS terminal. The word to be stored is applied to the data input terminals. After that the desired memory location is applied to the address input terminals. Then the read command is applied to the Read control input terminal. Fig. 5 shows the simulation results of 4 bit memory.

4.2 Design of SOC

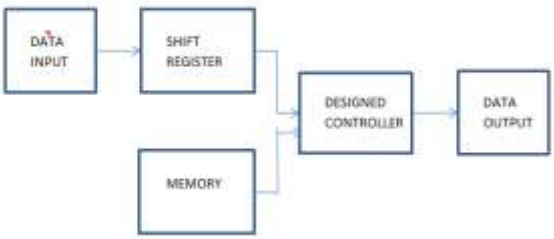

Fig.2 Block diagram of SOC design.

Fig.2 shows the block diagram of SOC for vehicle. The system on chip for vehicle consist of shift registers, memory , controller and input output ports. At first the data input is applied to the shift register. It is serial in parallel out shift register. The shift register gets the data serially and at the output of the shift register we get parallel data output.

According to the input conditions of the memory , particular memory location gets selected. This data present at the selected memory location reflects to the output of the memory where it is compared with the output of the shift register by controller. The controller designed here is nothing but Comparator.

Depending on the output of the comparator respective action will take place so as to control the parameter. The simulation results of the designed SOC is shown in Fig.3.In this designed SOC the comparator compares the predefined data stored in memory with data present at the output of the shift register. The system works on synchronous clock.Clock1 is the system clock.Clr1 is the clear signal applied to clear the data .Din1 and Din2 are the input data applied to the shift register.We1 is the enable signal applied to the memory.A0(3:0) are the address lines of memory used to select the particular memory location.

V. Result

Table I: Xilinx Device Utilization Summary

Logic Utilization	Available	Used	Utilization (%)
Number of .Slice Registers	18,224	8	1%
Number of. Slice LUT‘s	9112	8	1%
Number of fully used LUT-FF pairs	40	4	10%
Number of Bonded IOB‘s	232	26	11%

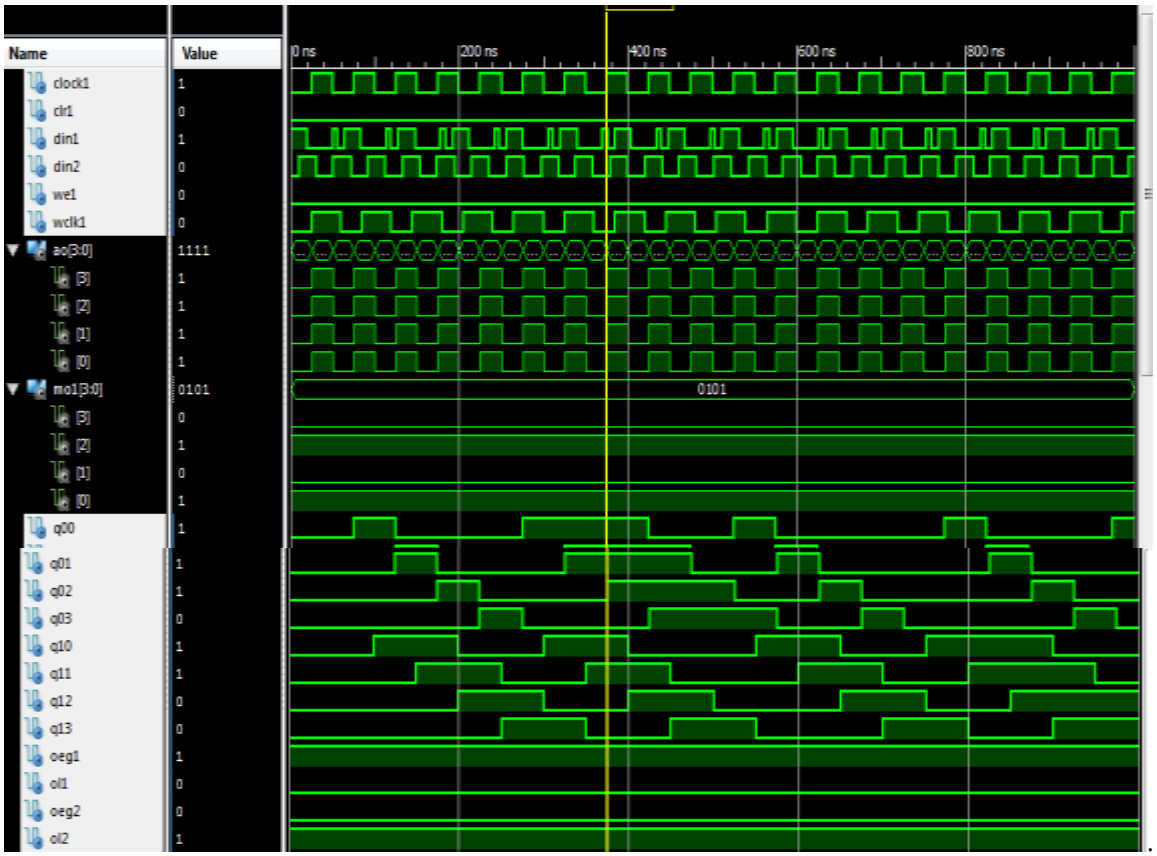

Fig.3 Simulation Result For SOC Design

Fig.4 Implementation Result of a System

Fig.5 Simulation results for four bit memory.

Table I shows synthesis report which gives information of the cell usage, device utilization constraint, timing Summary. The device utilization gives information of the total hardware utilized. In this integration of the memory, Controller, shift register, I/O ports is done. Here the data input is applied to the shift register. Shift register accepts the input serially and gives parallel output. Then this output is compared with the preset data present at the memory. Then the controller compares the data and gives the appropriate result at the output terminal. The output signal activates the dc wiper motor and dc glass door motor for wiper and ventilation control respectively.Fig.4 shows the result of a complete system when implemented on FPGA kit.

VI. Conclusion

In this paper the SOC for vehicle is designed. The SOC can also be designed for the different application such as telecommand, networking, communication. The system proposed here will consumes less power, the response time will be less. The system design will be small. The system will work efficiently. The implementation of the proposed system will be done using XILINX FPGA and the functionality of the proposed system will be verified using ISIM simulator.

With additional modification in the system design VANET, MANET can be added to the system. This addition can make the system more superior and it will decrease the accidents on the road. The system can also be interfaced with sensors.

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References

[1] V. Usha Rani, K. Omeswara Reddy "Microcontroller Managed Module For Automatic Ventilation Of Vehicle Interior" International Journal of Industrial Electronics and Electrical Engineering, ISSN:47-6982 Volume-3, Issue-6, June-2015.

[2] Fazel Elahi, Rahman "Intelligent windshield for automotive vehicles" Computer and information technology (ICCIT),2014 17th international conference on INSPEC Accession Number:15025783.

[3] Mukul Joshi1,2, Kaustubh Jogalekar2, Dr. D.N.Sonawane2, Vinayak Sagare3, M.A.Joshi2, "A Novel and Cost Effective Resistive Rain Sensor for Automatic Wiper Control : Circuit Modelling and Implementation". 2013 Seventh International Conference on Sensing Technology.

[4] Rajesvari.R1, Manoj.G2, Angelin Ponrani.M3 "System-on-Chip (SoC) for Telecommand System Design". International Journal of Advanced Research in Computer and Communication Engineering Vol. 2, Issue 3, March 2013.

[5] Mr. TR. Parthasarthy, Mr. N. Venkatkrishnan, Mr. K. Balmurugan, "Analysis of partitioning between ARM and FPGA on performance characteristics." ISBN NO.978-1-4673-2048-1/12/$31.00@2012 IEEE.

[6] Dae Geun Lee,Se Myoung Jung , Myoung Seob Lim "System on Chip design of Embedded Controller for Car Black Box" 2007 IEEE Intelligent Vehicles Symposium Istanbul, Turkey, June 13-15, 2007.

[7] Huang Jin "Embedded memory in system-on-chip design: architecture and prototype implementation"4-7 May 2003, ISSN : 0840-7789.