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Design & Performance Analysis of Low Power Reversible Carry Skip Adder

[1]Ankush, [2]Amandeep Singh Bhandari
[1]*M.Tech (Research Scholar) Department of ECE Punjabi University, Patiala*
[2]*Assistant Professor Department of ECE Punjabi University, Patiala*

Abstract: *Now a day's reversible logic is an attractive research area due to its low power consumption in the field of VLSI design circuit. This paper presents reversible carry skip adder using various reversible logic gates. The classical set of gates such as AND, OR & EX-OR are not reversible. Reversible logic circuits provide low power dissipation as well as zero fan out. In this paper carry skip adder is designed using Modified HNG & Modified FRGgates, thus provided low quantum cost and power dissipation. The comparative result shows that the proposed design is much better in terms of power.*
Keywords:*Reversible logic, Reversible gates, Quantum cost, Power dissipation*

I. Introduction

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. The loss of information is associated with laws of physics describing that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system [2]. Reversibility in computing implies that information about the computational states should never be lost. The reversible logic is either physical reversible or logical reversible. Reversibility in computing implies that no information about the computational states can never be lost, so it can be recover any earlier stage by computing backward or un-computing the results. This is known as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no heat in terms of wastage of energy [1]. Various parameters of reversible logic gates are observed while designing the work.

Reversible logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. A reversible gate is also defined as a bijective Boolean function from n to n values. Let the input vector be Iv, output vector Ov and they are defined as follows,

Iv = (Ii, Ii+1, Ii+2 …In-1, In) and Ov = (Oi, Oi+1, Oi+2 … On-1, On). For each particular i, there exits the relationship **Iv = Ov** [13]

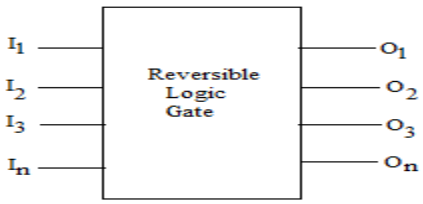

Fig.1 Symbol of Reversible logic gate with n*n input and output

Inthe design of reversible logic circuits the following points must be considered to achieve an optimized circuit.

- Garbage outputs must be minimum.
- Minimum delay.
- Loops or feedbacks are not permitted.
- Minimum quantum cost.
- Fan-out is not permitted.

II. Families Of Reversible Logic Gates

The various families of reversible logic gates used commonly are explained below

2.1 Feynman Gate

Fig 2 shows the Feynman gate which is a 2*2 gate and is also called as Controlled NOT gate and it is widely used as a copying gate because fan-out is not allowed in reversible logic. It has Quantum cost one.

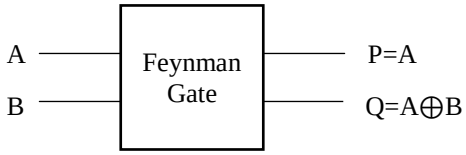

Fig.2. Feynman Gate – 2*2 gate

2.2 Toffoli Gate

Fig 3 shows a Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C. It has Quantum cost five.

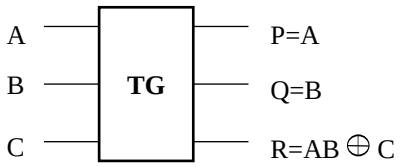

Fig. 3 Toffoli Gate – 3*3 gate

2.3 Fredkin Gate

Fredkin gate is 3x3 gate with input vector is I(A,B,C) and the output vector is O(P,Q,R).The output is P=A,Q=A'B+AC and R=A'C+AB. Quantum cost of Fredkin gate is 5.

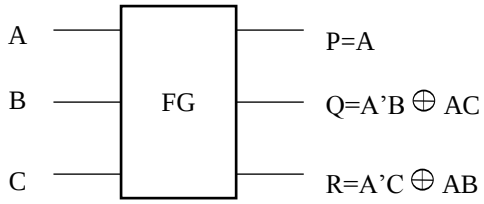

Fig. 4. Fredkin Gate – 3*3 gate

2.4 Peres Gate

Fig 5 shows a Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A, Q = A XOR B, R = AB XOR C. it has the Quantum cost of four.

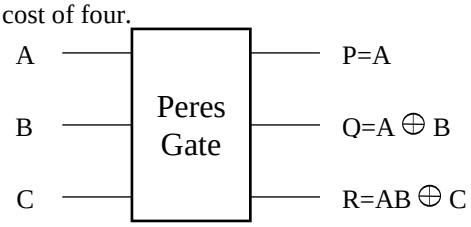

Fig. 5 Peres Gate – 3*3 gate

2.5 Inventive0 Gate

Inventive0 gate is a 4x4 gate. The utility of this gate is that it can operate individually as a reversible full adder as well as reversible full subtraction and it requires lesser hardware complexity also. The quantum cost of Inventive0 gate is 10.

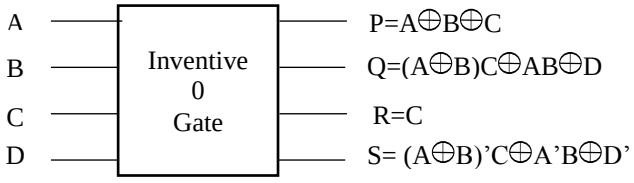

Fig.6 Inventive0 Gate - 4*4 gate

2.6 HNG Gate

It's a Haghparastnavi gate. It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost 6. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

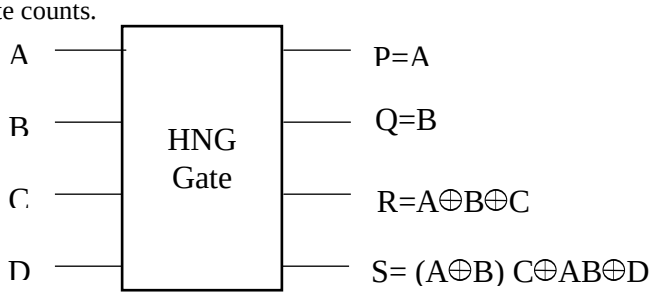

Fig.7HNG Gate - 4*4 gate

2.7 MHNG Gate

MHNG gate is a 4x4 reversible gate with following input and output vectors, Iv = (A, B, C, D) and Ov = (P = A, Q = D, R = A⊕B⊕C, S = (A⊕B).C⊕AB⊕D. One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit. The quantum cost of MHNG gate is 5.

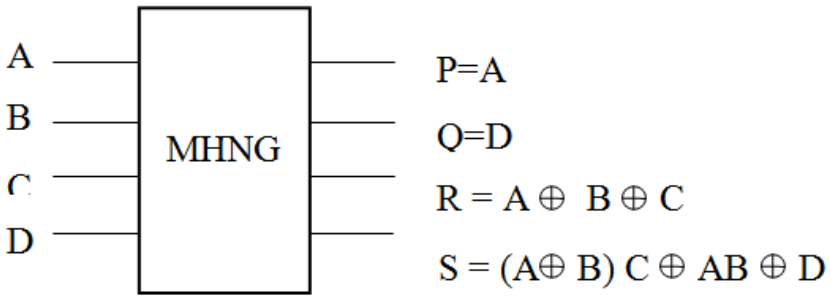

Fig. 8MHNG Gate - 4*4 gate

2.8 Modified Fredkin Gate

Modified Fredkin gate is 3x3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R).The output is P=A, Q=AB'⊕ AC' and R=A'C⊕AB. Quantum cost of Fredkin gate is 4.

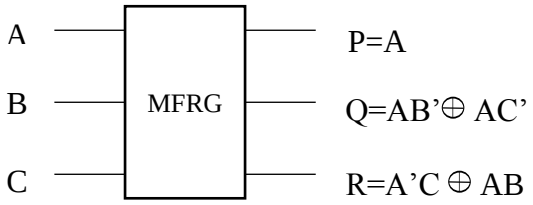

Fig. 9 Modified Fredkin Gate – 3*3 gate

III. Parameters For Determining The Peformance Of The Circuit

3.1 Gate count: The number of reversible gates used to realize the function.

3.2 Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.

3.3 Quantum cost: This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Quantum gates have some property given in equation 1, 2 and 3.

1. V*V=NOT
2. V*V+ =V+*V=1
3. V+*V+=NOT

3.4 Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.

3.5 Garbage Output: Unwanted output of reversible gate is called garbage output. Fig. 10 shows an example of reversible function of f = x1x2 ⊕ x3, the two unused pins are the garbage outputs.

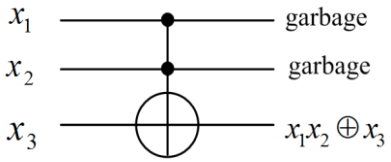

Fig.10 Garbage Output

IV. Proposed Work

Carry Skip Adder: Carry skip adders reduce the carry computation delay. Carry skip adder basically used to propagate Cin (Carry input) to the Cout (Carry Output) in faster way [12, 14, 15, and 16].

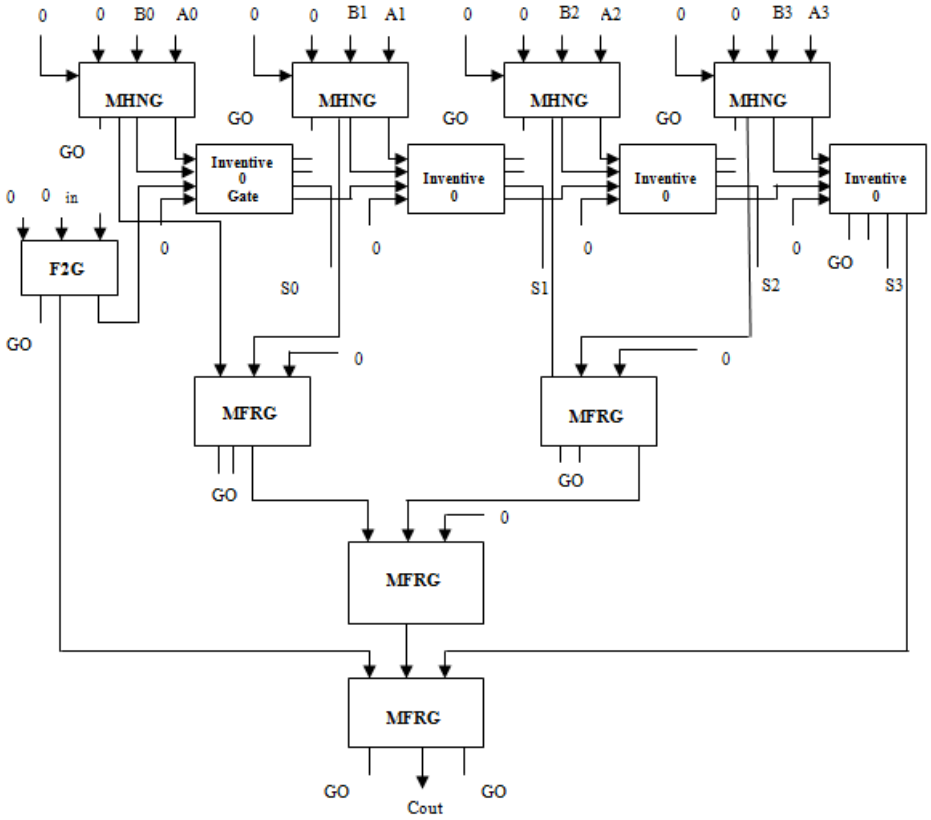

Fig. 11 Design of 4-bit Proposed Reversible Carry Skip Adder

A full adder with a propagate signal is used as a building block in carry skip adders. In a full adder, if either input is a '1', the carry input is propagated to the carry output. Therefore, the carry input Ci to the ith full adder will propagate to its carry output Ci+1 when $p = a \oplus b = 1$; such an adder is called a carry skip compatible adder. The proposed design used 4 MFRG gates as shown in fig. 11. The carry out of the circuitis obtained at the fourth gate (MFRG) output. The number of garbage outputs of this design is 21. A 4-bit carry skip adder can be constructed by using four carry-propagate compatible full adders. In our proposed design Inventive0 gate acts as full adder circuit. The propagate signals generated by each adder are ANDed. The resulting output is ANDed with carry inputCi. The corresponding output is ORed with carry output of the fourth full adder to get the carry output. The same implementation can also be implemented using the reversible logic gates shown in Fig 11.

Algorithm: For construction of carry skip adder circuit
Input: A= (A0, A1, A2, A3) and B= (B0, B1, B2, B3) and Cin
Output: S= (S0, S1, S2, S3) and Cout
Begin
Level 1: For all i in (0, 1, 2, 3)
Compute Pi = Ai ⊕ Bi from MHNG gate and also copy Ai and Bi

Level 2: Compute S= (C4, S0, S1, S2, S3) from inventive0 gate. Where Si = Ai ⊕ Bi ⊕ Ci
Level 3: Compute carry skip- logic bit Cout = PCin ⊕ P'C4 from MFRG gate.
End

V. Implementation & Results

Table1: Comparison of Proposed work with Existing work

Carry Skip Adder	Quantum Cost	Power Consumption
Proposed Design	78	3.349 W
Existing Design[17]	86	4.058 W

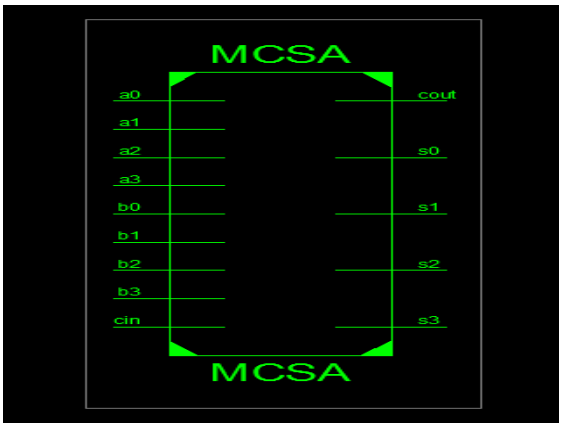

Fig. 12 Symbol of 4-bit Carry Skip Adder

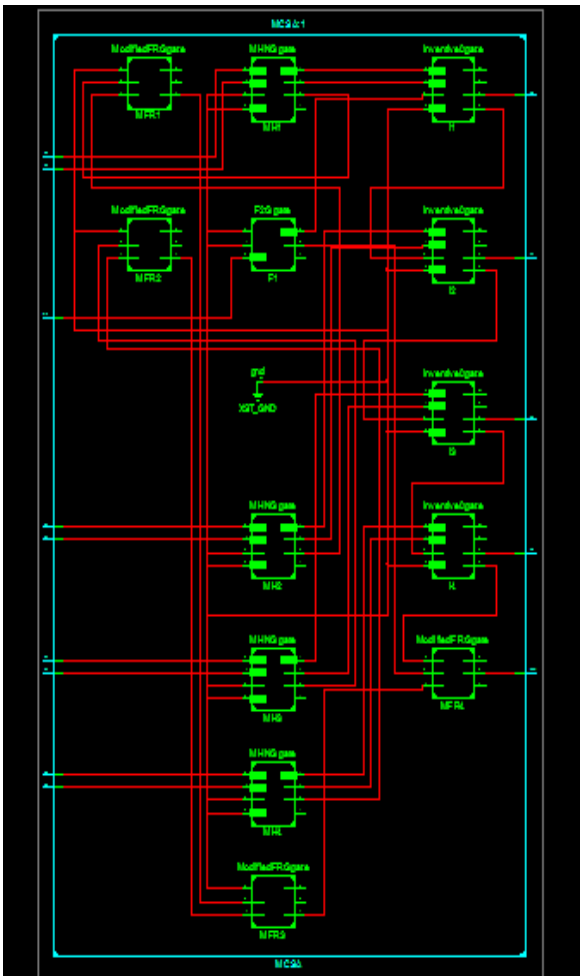

Fig.13 RTL view of 4-bit Carry skip adder using MHNG gates, F2G gate, Inventive0 gates and MFRG gates

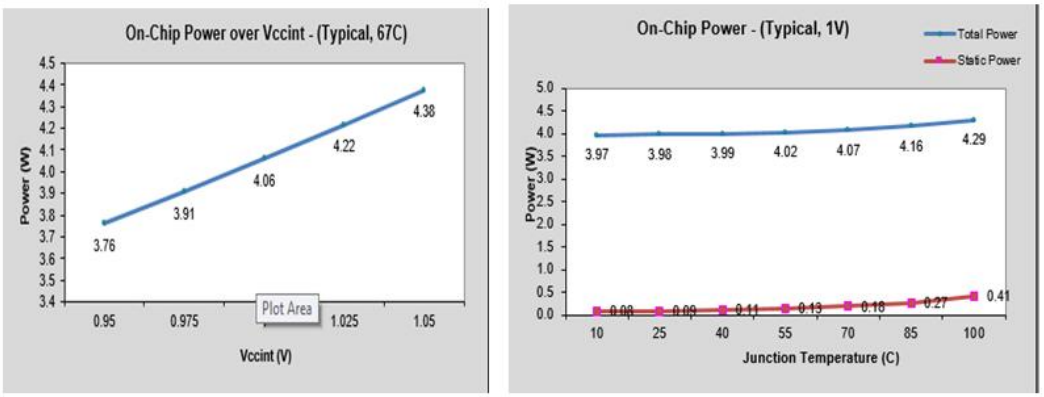

Fig. 14 Power Dissipation Graphs for Carry Skip Adder using reversible gates [17]

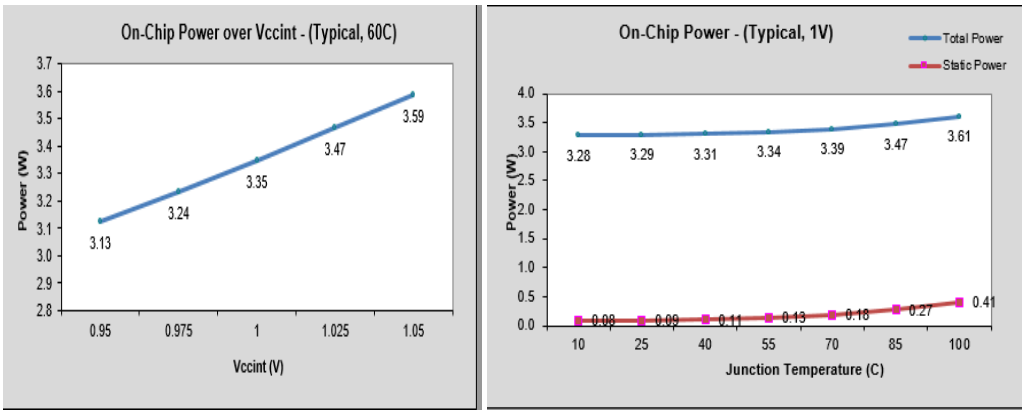

Fig. 15 Power Dissipation Graphs for Carry Skip Adder using reversible gates

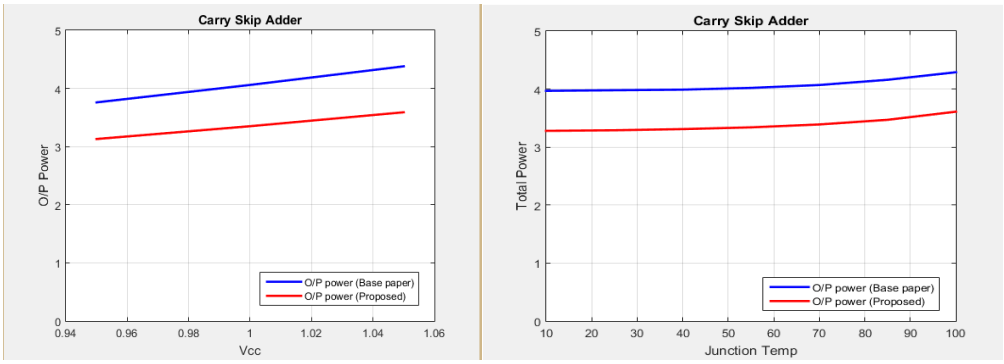

Fig. 16 Comparative results of Power dissipationforproposedCarry Skip Adder using reversible gates And existing results [17].

The proposed reversible carry skip adder is more efficient than the existing carry skip adder presented in [17].Evaluation of proposed circuit can be comprehended easily with the help of the comparative results in Table 1. Therefore, the proposed carry skip adder is better than the existing adder in terms of quantum cost & power dissipation.

V. Conclusion & Future Work

Reversible computing has its great significance in diminishing the complexity of the digital circuits. In this paper, we presented reversible carry skip adder using MFRG gates, MHNG gates, inventive0 gates & F2G gate. Table 1 demonstrates that the proposed reversible carry skip adder is better than the existing designs in terms of power dissipation and quantum cost. Our proposed reversible carry skip adder can be applied to the design of complex systems in nanotechnology.

References

[1]. Landauer.R "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2]. Bennett C H "Logical Reversibility of Computation", IBM J.Research and Development, pp. 525-532, November 1973.

[3]. Majid Mohammadi, Mohammad Eshghi, Abbas Bahrololoom,'' Behavioral Model ofV and V+ Gates to Implement the reversible Circuits Using Quantum Gates'', IEEE, 2008.

[4]. D. Michael Miller and Zahra Sasanian,'' Lowering the Quantum Gate Cost of Reversible Circuits'', IEEE, 2010.

[5]. Prashant .R.Yelekar,Prof. Sujata S. Chiwande, "Introduction to Reversible Logic Gates & its Application", 2nd National Conference on Information and Communication Technology (NCICT) 2011.

[6]. B.Raghu Kanth, B.Murali Krishna, M.Sridhar, V.G.Santhi swaroop,''A Distinguish between Reversible and Conventional logic Gates, International journal of engineering research and applications, vol.2, issue2, April 2012.

[7]. Mr. Devendra Goyal, Ms. Vidhi Sharma, ''VHDL Implementation of Reversible Logic Gates'', International Journal of Advanced Technology & Engineering Research (IJATER), ISSN NO: 2250-3536 volume 2, issue 3, may2012.

[8]. Raghava Garipelly, P.Madhu Kiran, A.Santhosh Kumar,''A Review on Reversible logic gates and their Implemantation'', International journal of emerging and advanced engineering, March2013, volume3, Issue3.

[9]. Neeta Pandey,Nalin Dadhich, Mohd. Zubair Talha,''' Realization of 2:4 reversible decoder and its applications, International Conference on Signal Processing and Integrated Networks (SPIN).IEEE, 2014.

[10]. Ashima Malhotra, Charanjit Singh, Amandeep Singh,'' Efficient Design of Reversible Multiplexers with Low Quantum Cost and Power Consumption'', International Journal of Emerging Technology and Advanced Engineering, Volume 4, Issue 7, July 2014.

[11]. Ashima Malhotra, Charanjit Singh, Amandeep Singh," Efficient Design of Reversible Multiplexers with Low Quantum Cost", Int. Journal of Engineering Research and Applications, Vol. 4, Issue 7(Version 4), July 2014.

[12]. Himanshu Thapliyal and Nagarajan Ranganathan. 2011. A New reversible design of BCD adder. In proceeding of the design Automation and test in Europe (DATE). Grenoble. France. 1180-1183.

[13]. Sukhjeet kaur, Amandeep Singh, " Design and Performance Analysis of Encoders using Reversible logic gates" International Journal of Scientific & Engineering Research, Volume 6, Issue 6, June-2015.pp.327-332

[14]. Biswas, A. K., Hasan, M. M., Hasan, M., Chowdhury, A. R., & Hasan Babu. 2008. A novel approach to design BCD adder and Carry Skip BCD adder, 21st International Conference on VLSI Design, 566-571.

[15]. Zhou, Rigui, Manqun Zhang, Qian Wu, and Yang Shi. 2012. Designing novel reversible BCD adder and parallel adder/subtraction using new reversible logic gates, International Journal of Electronics. v (99), no. 10, 1395-1414.

[16]. Krishnaveni, D., and Geetha Priya, M. 2010, A Novel Design of Reversible Serial and Parallel Adder/Subtractor, International Journal of Engineering Science and Technology, vol 3, 2280–2288.

[17]. Neeraj Kumar Misra, Mukesh Kumar Kushwaha, Subodh Wairya and Amit Kumar, (2015) "Cost Efficient Design of Reversible Adder Circuits for Low Power Applications", International Journal of Computer Applications, 117(19), pp. 37-45.