IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 5, Ver. II (Sep. - Oct. 2016), PP 01-06
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Level Converting Retention Flip-Flop for Low Standby Power Using LSSR Technique

Harati V L Devi. Bhupati[1], M. Lakshmi Prasanna Rani[2]
[1]*M.Tech ECE department, MVGR college of engineering (VZM), India*
[2]*Assistant professor ECE department, MVGR college of engineering (VZM), India*

Abstract: *In VLSI we have an exponential increase of leakage power due to scaling of threshold voltage. We have both active power and standby power dissipation. It is important to reduce standby leakage in case of small battery operated devices. A flip-flop will hold the logic only in the active mode of operation. But a retention flip-flop will hold the data even in the standby mode of operation, with continuously given supply exclusively for the retention latch. A level converting retention flip-flop is used to turn off the voltage regulator in the standby mode of operation, to reduce standby power dissipation.The proposed retention flip-flop will reduce the standby power dissipation, in which the retention latch was designed using LSSR (LECTOR (LEakage Control transistor) Stacked State Retention) technique. The slave latch of the proposed retention flip-flop constructed by using thick oxide transistors, i.e. the length of the transistor has taken as 350nm. The architecture of retention flip-flop depends on $V_{DD,IO}$ scheme, in which $V_{DD,core}$ and $V_{DD,IO}$ are two different voltages.$V_{DD,IO}$ is higher than the $V_{DD,core}$. The level up conversion from $V_{DD,core}$ to $V_{DD,IO}$ is achieved by NMOS pass transistor level conversion scheme, which is based on an always low signal transmission technique. The proposed retention flip-flop reduces the standby leakage compared to LECTOR based retention flip-flop, with small increase in area. The proposed retention flip-flop was designed in 130nm technology with 1.2V and 2.0V for core latch and retention latch respectively. The operating frequency is 20MHz, and the standby power is 255.8619pW.*

Keywords: *standby leakage, retention flip-flop, level conversion scheme, forced stack technique, LECTOR & LSSR technique.*

I. Introduction

To get high performance and low power dissipation and optimized area CMOS technology has been scaled down. We have total power dissipation as $P_D=V_{DD}^2*f*C_L$. V_{DD} is the supply voltage, f is the frequency of operation, and C_L is the load capacitor.in VLSI chip designing f is limited to 4GHz and we cannot vary the frequency more than that. Coming to the C_L, if number of stages are increased the parallel combination of capacitor becomes an impractical value. So to reduce the total power dissipation we need to scale down the supply voltage, by following the lithographic techniques. The secondary effect for scaling of supply voltage is the sub threshold leakage current. So the threshold voltage scaling should done in such a way that to achieve high current density and good performance. We have both active power dissipation and standby power dissipation. Major part of the total power dissipation is contributed by standby power dissipation, because most of the battery operated devices occupies most of the system time in the standby mode of operation. So to reduce the standby power dissipation, and to save the data without any change in the standby mode, a level converting retention flip-flop is used.

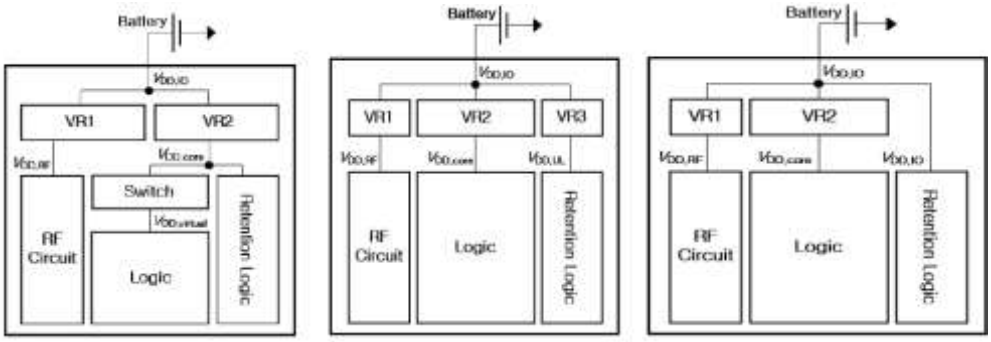
In this paper we propose a level converting retention flip-flop which has both master latch and slave latch with supply voltages $V_{DD,core}$ and $V_{DD,IO}$. The $V_{DD,IO}$ is higher than the $V_{DD,core}$. Thelevel conversion between these two voltage levels is achieved by using NMOS pass transistor logicscheme connected between master latch as well as slave latch. The slave latch or retention latch in the proposed retention flip-flop is designed based on a technique called LSSR technique, which is the combination of forced stack and LECTOR technique. The LSSR based retention flip-flop will reduce the standby power and total power dissipation, compared to the retention flip-flop designed using LECTOR technique.

The remaining ofthis paper is arranged as follows. The retention architectures used for the retention flip-flops is explained in section II. The NMOS pass transistor level conversion scheme is explained in the IIIrd section. . In the IVth section we explain about inverters used in the design of both LECTOR and LSSR based retention flip-flops. The working, schematic diagram, timing diagramsof both LECTOR and LSSR based retention flip-flops and layout of proposed flip-flop is given in Vth section. Results Comparison table has given in VIth section.

II. Different Retention Architectures of Retention Flip Flops

There are three types of architectures for retention flip-flops for reducing standby power.

1. MTCMOS (Multi Threshold CMOS) scheme.
2. Ultralow supply voltage scheme ($V_{DD,UL}$).
3. I/O supply voltage ($V_{DD,IO}$).



(1) **(2)** **(3)**

MTCMOS: This is a power gating scheme in which the retention logic get the supply from $V_{DD,core}$ and computational or core logic is supplied with $V_{DD,virtual}$. This is a power gating scheme, in which multi threshold voltage usage reduces the standby power [1], and also the computational logic is power gated to optimize standby power.

The power reduction is limited due to the voltage regulator VR2. The VR2 should remain continuously on during the standby mode, due to which the retention logic is always turned on. For power gating large switches are used, due to which the area overhead and power overhead problems are increased. Therefore area overhead and power overhead are the two drawbacks of MTCMOS scheme.

Ultralow supply voltage scheme: Ultralow voltage scheme is another one for reducing the standby mode power. In this scheme the leakage power is reduced by using an ultralow supply voltage, in the standby mode. The sub threshold leakage is reduced, since the transistors in retention logic are operated in weak inversion region, with low drain to source voltage. The voltage regulator which generates ultralow voltage is used only for the retention logic, with some area overhead and with active power overhead problem. It also has the same problem as that of the MTCMOS scheme, because of the on state of the voltage regulator in the standby mode of operation. So there is a need of an architecture, which switches off the voltage regulator in the standby mode of operation.

I/O supply voltage: This scheme avoids the use of voltage regulator separately for the retention latch. This architecture will switch off the voltage regulator in the standby mode of operation to reduce the standby power. The standby power of a voltage regulator is higher than the standby leakage power of $V_{DD,IO}$. The $V_{DD,IO}$ is higher than $V_{DD,core}$.

Since there is a level difference between $V_{DD,core}$ and $V_{DD,IO}$ it requires proper level shifting between them. The level conversion is achieved by using NMOS pass transistor logic between core logic and retention logic.

III. NMOS Pass Transistor Level Conversion

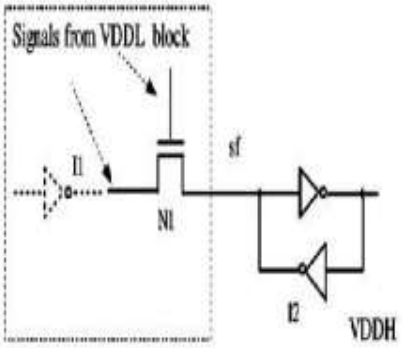


Fig: 4NMOS Pass Transistor Level Conversion

The signal from VDDL block has given to switch on the transistor N1. In this process of level conversion non-delicate paths are supplied with low supply voltage and speed delicate paths are supplied with high supply voltage. The transistor N1 is attached with low voltage input signal and level deviation point sf is hiked to VDDL-V_{th} of the NMOS transistor through N1. Associated I2 pulls the sf up to VDDH. The N1 and I2 are help in level deviation. As shown in fig: 4.[2]

IV. LECTOR Technique

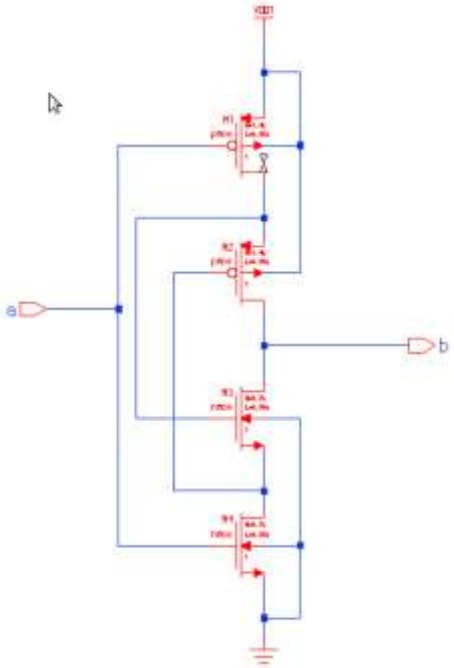


Fig 5: Schematic diagram of Inverter using LECTOR technique

LECTOR: in this technique two leakage transistors are used between pull up and pull down network. The gate terminal of one transistor is controlled by the source terminal of another transistor. The input is conveyed to the output in the inverting mode.

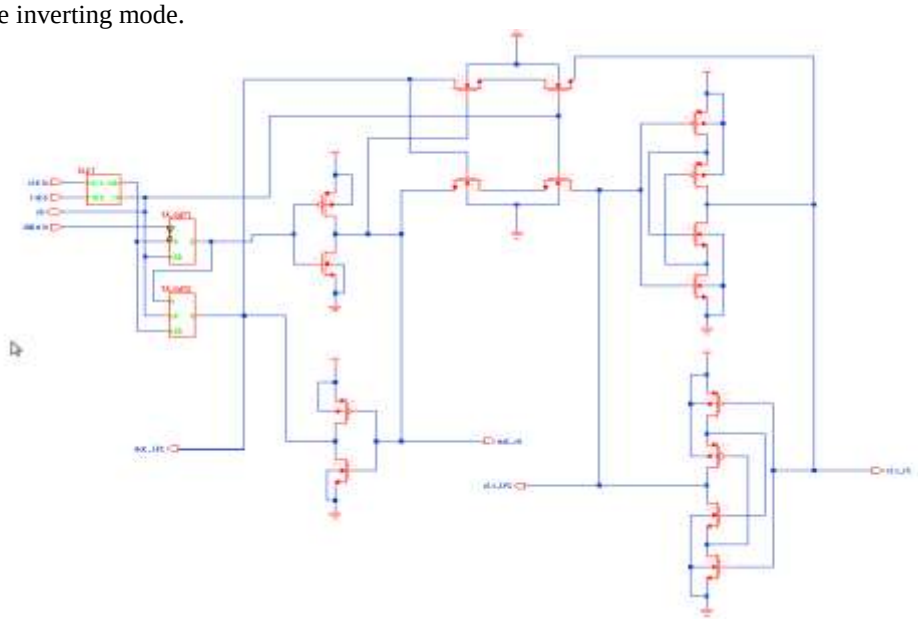


Fig 6: Schematic diagram of Level Converting Retention Flip-Flop using LECTOR

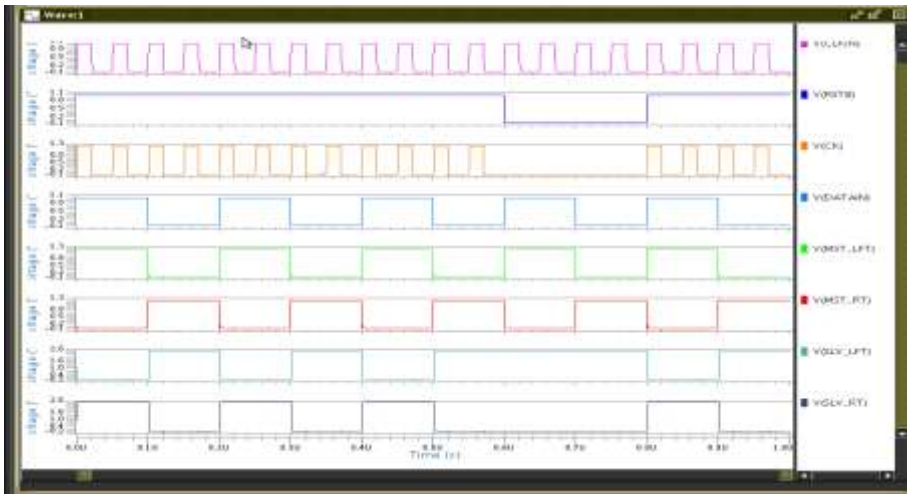


Fig 7: Timing diagram of Level Converting Retention Flip-Flop using LECTOR technique

Forced stack technique:

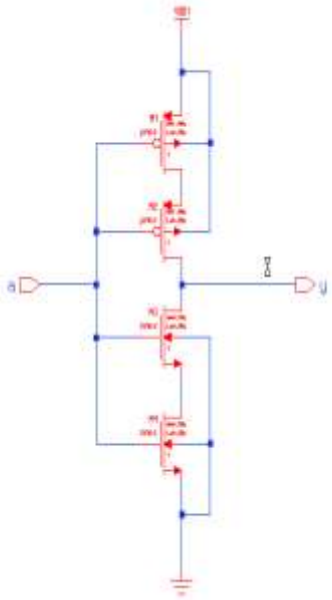


Fig 8: Schematic diagram of inverter using forced stack technique

LSSR technique: forced stack +LECTOR =LSSR technique.

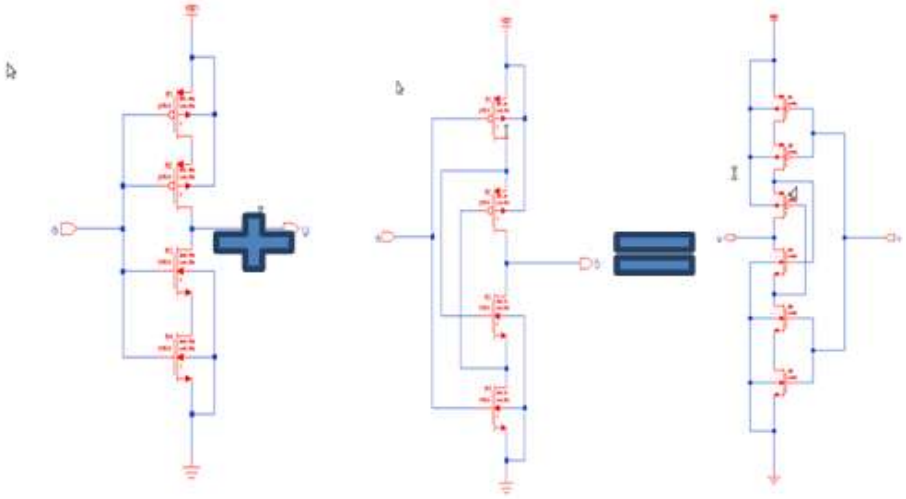


Fig 9: Schematic diagram of Inverter using LSSR technique

LSSR: The LSSR technique is the combination of forced stack and LECTOR technique. In this the leakage power is reduced due to the stacking of transistor in the pull up and pull down network. Each PMOS and NMOS are divided into two devices with half the width of the original device. Leakage control transistors are inserted between pull up and pull down networks.
Due to stacking technique the barrier height is increased so that it in turn increases the threshold voltage, thereby it reduces the leakage.

V. Working Of level Converting Retention Flip-Flop Using LSSR Technique

The proposed level converting retention flip-flop is composed of master latch and slave latch. The latches are cross coupled inverters. The MOS devices used in this flip-flops are thick oxide and thin oxide devices. Thick oxide devices are built using 350nm technology and thin oxide devices are built with 130nm technology. Master latch and slave latch are operated with different voltage levels. The level conversion between these two is achieved by NMOS pass transistor logic scheme.

Data is always transfers as low even the data is high or low. When mst_lft and mst_rt are low and high a transmission path is selected and it is transferred to the slave latch. In the standby mode of operation when the RSTb signal is low the ck becomes low then the clock connected NMOS transistors are switched off. Then the slave latch is detached to from the master latch.

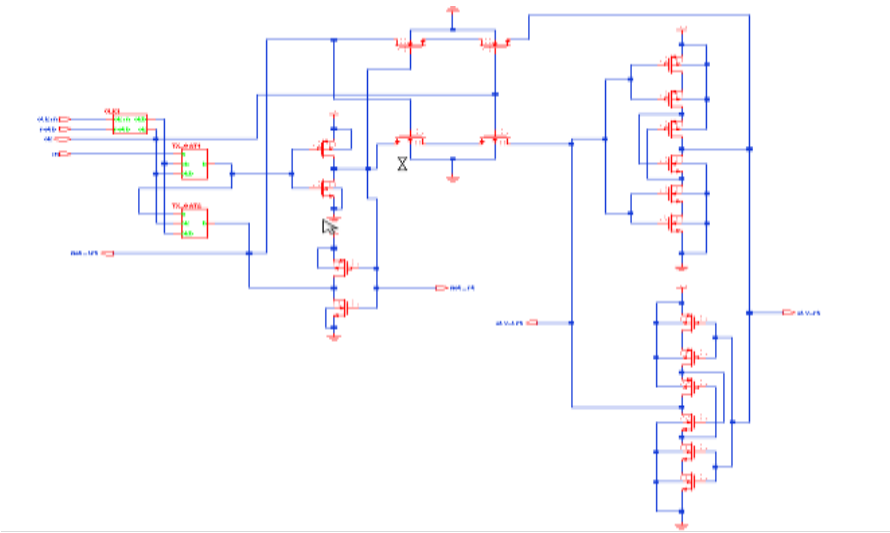


Fig 10: Schematic diagram of Level Converting Retention Flip-Flop

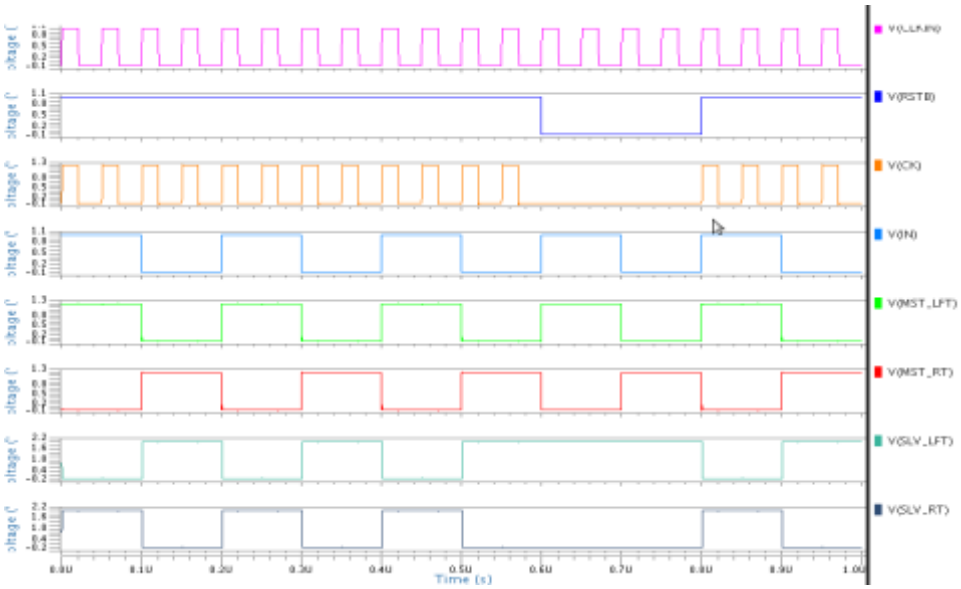


Fig 11: Timing diagram of Level Converting Retention Flip- Flop using LSSR technique

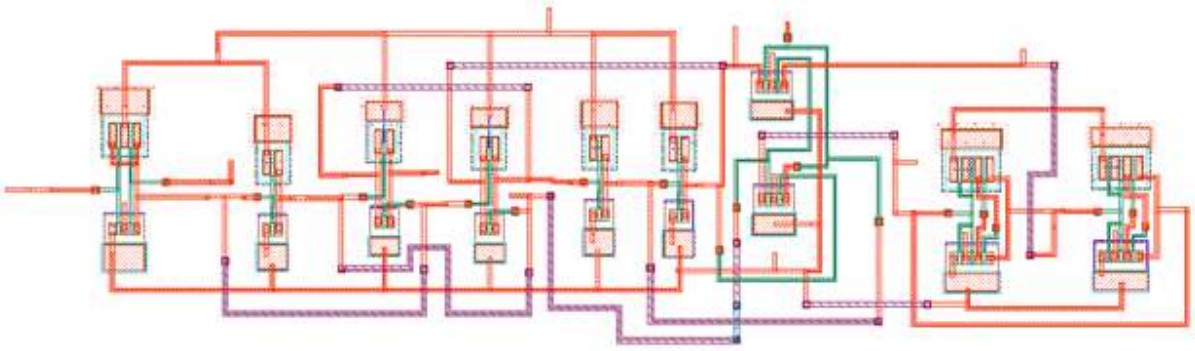


Fig 12: Layout of Level Converting Retention Flip-Flop using LSSR technique.

VI. Results

Technique	**LECTOR**	**LSSR (proposed)**
Process	**0.13µm**	**0.13 µm**
Supply voltage[V], $V_{DD, core}$, / $V_{DD, IO}$	**1.2/2.0**	**1.2/2.0**
Number of transistors	**24**	**28**
Power management scheme	**I/O V_{DD}**	**I/O V_{DD}**
Standby leakage power dissipation[pW]	**627.1119**	**255.8619**
Frequency (MHz)	**20**	**20**
Total power dissipation(µW)	**295.250**	**163.7959**

VII. Conclusion

A retention flip-flop which retains data using $V_{DD,IO}$ and performs level conversion using an embedded NMOS pass-transistor level conversion scheme employing a low only signal transmitting technique was proposed in which the retention latch is designed using LSSR technique.It gives low standby power of 255.8619pW, by turning off the voltage regulator in the standby mode of operation. The retention latch was built by 350nm technology to reduce the standby leakage power.The designed RFF will give low standby power compared to the RFFs designed by LECTOR technique. But the proposed RFF(LSSR) will have four extra transistors compared to LECTOR technique.

References

[1] Jung-Hyun Park, Heechai Kang, Dong- Hoon Jung, KyunghoRyu, and Seong-Ook Jung "Level – converting Retention Flip-Flop for Reducing Standby Power In ZigBee SOCs" IEEE, 2014.

[2] NamepalliMalathi, B.R.K. Singh. "Multi bit Retention Flip-Flop For ZigbeeSoC's" International Journal of Research in Computer and Communication Technology, Vol 4, Issue 11, November- 2015.

[3] Hamid Mahmoodi-Meimand and Kaushik Roy "Data-Retention Flip-Flops for Power-Down Applications".*IEEE,* december2008.

[4] Xiaohui Fan, Yangbo Wu, Hengfeng Dong, and Jianping Hu "A low leakage autonomous data retention flip- flop with power gating technique", journal of electrical and computer engineering, 2014.

[5] L. T. Clark, M. Kabir, and J. E. Knudsen, "A low standby power flip-flop with reduced circuit and control complexity," in Proc. IEEE CICC, Sep. 2007, pp. 571–574.

[6] H. Mahmoodi-Meimand and K. Roy, "Data-retention flip-flops for power-down applications," inProc.ISCAS , vol.2. May. 2004, pp. 677–80.