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Implementation of ultra-low power digital circuits using Sub-threshold adiabatic logic

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Abstract: *The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique and by applying sub-threshold logic. Behavior of adiabatic logic circuits in weak inversion or sub-threshold regime is analyzed in depth to make great improvement in ultra-low power circuit design. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and four bit carry look ahead adder using sub-threshold adiabatic logic. Post layout simulations show that sub-threshold adiabatic units can save significant energy compared with a logically equivalent static CMOS implementation. Results are validated through extensive simulations in 22-nm CMOS technology using TANNER EDA tool.*

Keywords: *Adiabatic logic, carry look ahead adder (CLA), leakage, low power, sub-threshold.*

I. Introduction

The demand for implementing ultralow-power digital systems in many modern applications, such as mobile systems, sensor networks, and implanted biomedical systems, has increased the importance of designing logic circuits in sub-threshold regime. These emerging applications have low energy as the primary concern instead of performance, with the eventual goal of harvesting energy from the environment. In sub-threshold logic, circuits operate with a supply voltage V_{DD} lower than the transistor threshold voltage V_T. Conventional CMOS logic circuits utilizing sub-threshold transistors can typically operate with a very low power consumption, which is mainly due to the dynamic (switching) power consumption and is quadratically dependent upon the supply voltage and load capacitance C_L.

Recently, adiabatic logic (or energy recovery logic) style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime. Since the performance requirements are quite relaxed in many of these energy efficient sub-threshold applications, so the adiabatic style can be used efficaciously used in a sub-threshold regime to make the circuit more energy efficient. Therefore, the attempt to realize the sub-threshold adiabatic logic (SAL) concept is a new endeavor. In general, the design of SAL requires a deep knowledge of the main features of the adopted logic style, such as power dissipation, leakage current, impact of temperature variation, operating frequency, and noise immunity. In this paper, the behaviors of adiabatic logic in sub-threshold regime are discussed in depth. To demonstrate the workability of the adiabatic logic circuits in sub-threshold regime, a 4-bit carry look ahead adder (CLA) unit is adopted as a reference circuit. Extensive experiments are carried out using TANNER EDA TOOL to ensure the high energy efficiency and design feasibility of the proposed logic in weak inversion regime compared with other conventional CMOS logic.

Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component. In conventional CMOS logic circuits (Fig.1), from 0 to VDD transition of the output node, the total output energy is drawn from power supply. At the end of transition, only energy is stored at the load capacitance. The half of drawn energy from power supply is dissipated in PMOS network (F). From VDD to 0 transition of the output node, energy stored in the load capacitance is dissipated in the NMOS network (/F).Adiabatic logic circuits reduce the energy dissipation during switching process, and reuse the some of energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the ramp or sinusoidal power supply voltage.

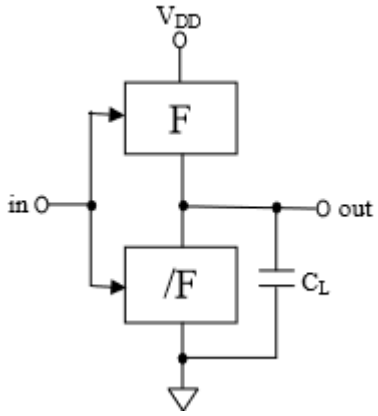

Fig.1. Conventional CMOS logic circuit.

II. Dissipation mechanisms in adiabatic logic circuits

Fig.2 shows, the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, C_L is the load capacitance.

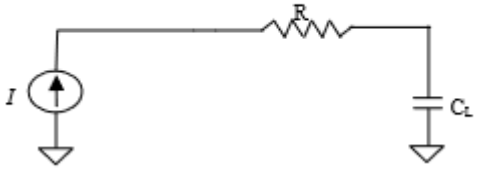

Fig.2 Equivalent model during charging process in adiabatic circuits.

The energy stored at output can be retrieved by the reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction.

III. Adiabatic logic families

There are the many adiabatic logic design technique are given in literature but here two of them are chosen ECRL and PFAL, which shows the good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation.

A. *Efficient Charge Recovery Logic (ECRL)*

The schematic and simulated waveform of the ECRL inverter gate is shown in Fig.3 and Fig.4 respectively. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to VDD, since F is on so output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, '/out' returns its energy to pck hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pck.

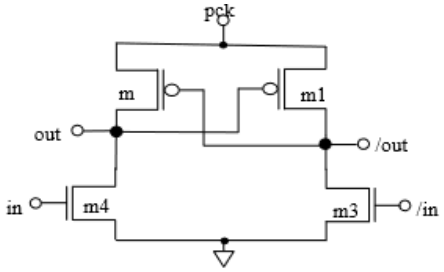

Fig.3 Schematic of ECRL inverter

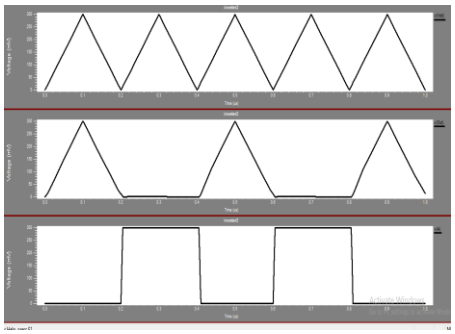

Fig.4 Simulated waveform of the ECRL inverter gate.

B. ***Positive Feedback Adiabatic Logic (PFAL)***

The schematic and simulated waveform of the PFAL inverter gate is shown in Fig.5 and Fig.6 respectively. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to VDD, since F and m4 are on so output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, '/out' returns its energy to pck hence delivered charge is recovered. PFAL uses four phase clocking rule to efficiently recover the charge delivered by pck.

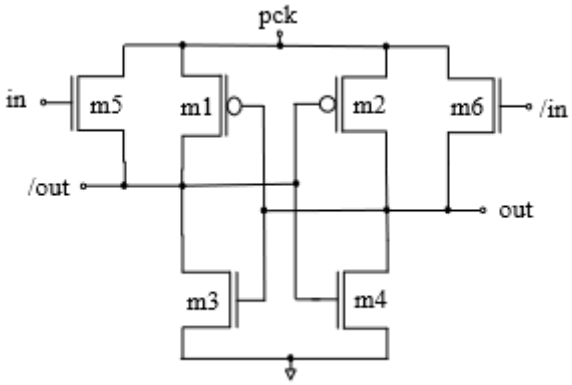

Fig.5 Schematic of PFAL inverter

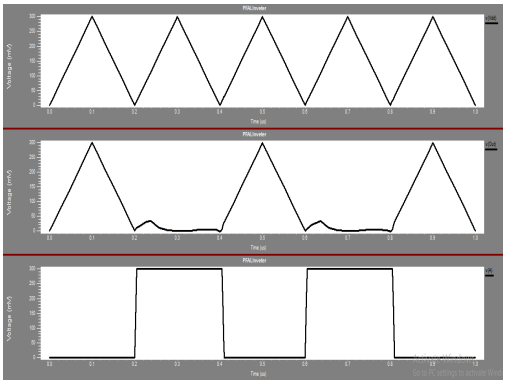

Fig.6 Simulated waveform of the PFAL inverter gate

IV. Delay calculation

As SAL(sub-threshold adiabatic logic) is efficacious where instead of performance, power dissipation is major concern. For example, in implanted biomedical systems, the circuits remain active for a very small span of time and remain idle for most of the time. In such operations, much lower frequency ranges are required. Therefore, in SAL, minimization of power dissipation is the pivotal issue. Hence, we address the delay in SAL though it would be few times larger than that in the conventional one. In SAL-based digital circuits, output nodes follow the supply clock very closely during the charging and discharging periods and the output waveforms get the same pattern as the supply voltage. In general, delay can be calculated between a change in an input (50% of VDD on input) and a low-to-high or high-to-low change in the output (50% of VDD on input). As the supply voltage ramps up and down linearly in between 0 and VDD, propagation delay would be roughly

T/2, where 2T is the width of total supply clock. Variation in delay is observed where the time period is 10 μs. Therefore, in worst case process variation of chip and die, delay would not be affected significantly. A 3% relative delay variation has been observed with three sigma variation on the path. Though process variations do not affect the propagation delay of SAL, increasing the frequencies can minimize the propagation delay. Increasing supply voltage also enhances the speed a bit. Simultaneously, power dissipation must increase with speed. However, we should keep in mind that minimizing power dissipations would be more important than decreasing the delay in SAL.

V. Sub-threshold adiabatic logic-based 4-bit CLA

In this section, design and analysis of SAL-based 4-bit CLA are given to show the workability and the feasibility of the proposed logics. Hence, 22-nm technology file is used in our transistor-level designs which guarantee the manufacturability of our designs under all normal conditions with favorable yields. The basic building block of 4-bit CLA is given in Fig. 7, using ECRL logic gates which is also very similar to the conventional structure . Hence, we implemented the sum (S_i) in three stages to avoid delay mismatching with the carry generation. In SAL-based 4-bit CLA, every stage will be controlled by the supply clock. Like the conventional approach, the expression of the ith sum and the (i +1)th carry output can be given as

$$S_i = A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_iB_i + (A_i \oplus B_i)\, C_i.$$

According to the synthesized gate level block, the SAL gate level structure of 4-bit CLA has been implemented using TANNER W-edit simulation tool.

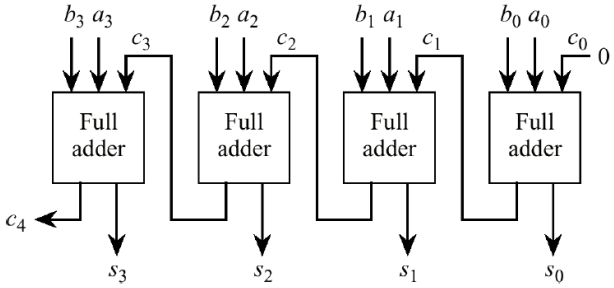

Fig. 7. Logic structure of 4-bit CLA

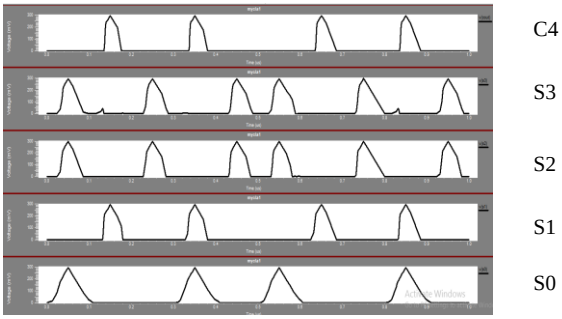

Fig. 8. Obtained output waveform of 4-bit CLA-based on SAL in post layout simulation.

In the post layout output waveform, given in Fig.8, four sum outputs, i.e., S0, S1, S2, andS3 along with the final carry output, C4, are given to show a better understanding and workability of the proposed logic. Hence, the inputs and outputs, i.e., A, B, and S are represented as, A= A3A2A1A0, B = B3B2B1B0, and S = S3S2S1S0, respectively. During the simulation, we set arbitraries A and B along with Cin. The values are A0 = 01010, A1 = 10101, A2 = 01010, A3 = 01010, B0 = 01010, B1 = 10101, B2 =01010, B3 = 10101, and Cin = 10010. Initially, carry is set to logic 1, i.e., C0 =1. Later arbitrary logic levels are assigned for Cin. Adding these A and B inputs, we get, S0 = 1; S1 = 0; S2 = 1; and S3 = 1. The carry output will be C4 = 0, as no carry will be generated. If carry is generated it would be forwarded to the next stage, as given in Fig. 7. Output waveforms are triangular as the charging and discharging of output nodes follow the supply clock, $\phi(t)$, very closely.

VI. Power gain

Here in this paper the supply voltage and input voltage are 300mv and load capacitance as 1.2F. In Fig.9, we observe that the power dissipation of SAL-based 4-bit CLA or conventional static logic-based 4-bit CLA increases with the supply voltage. The power dissipation due to switching depends on the square of the

supply voltage, V_{DD}, in both the conventional approach and in SAL. Power dissipation due to leakage will be a function of V_{DD} also in the case of both logic, yet that with increase in supply voltage, power dissipations due to leakage affect the conventional logic severely compared with SAL. Here, the conventional static CLA in sub-threshold regime consumes almost 1.3–1.6 times the total power dissipated by the SAL-based counterpart for the 300mV supply voltage range.

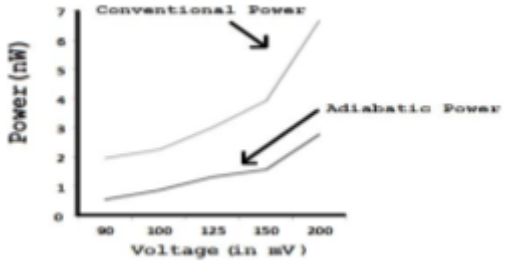

Fig. 9. Comparison of power dissipation of a 4-bit CLA between conventional static logic and SAL.

Table.1. Comparison between sub-threshold CMOS, PFAL & ECRL

Name of the circuit	inverter		4-bit CLA	
	Power(nw)	Delay(μs)	Power(nw)	Delay(μs)
CMOS	2.05	0.07	389.21	1.06
PFAL	1.95	0.30	306.59	2.13
ECRL	1.82	0.21	282.19	1.38

The variations in the atomistic nature, random doping fluctuations, and line edge roughness may affect the threshold voltage of nano-scaled devices. Fluctuation of threshold voltage would not affect the energy or power dissipation so much because the energy dissipation does not depend on threshold voltage directly. However, under a 300-mV supply voltage and a 1.2-F load in the output nodes, a **73%** of power gain is obtained by sub-threshold ECRL compared to conventional sub-threshold CMOS. Power dissipation does not vary so much (remains within 5% variation). This showed even with process variations, and we actually obtained proper waveforms and can claim that the proposed design can work commercially and would not affect the yield of the whole chip.

VII. Conclusion

Under sub-threshold logic the ECRL and PFAL can work better than the sub-threshold CMOS. SAL has been presented in this paper to advance the ultralow power research. SAL saves considerable energy compared with the static conventional logic. Post layout simulations using TANNER TOOL and the comparison with the static counterpart explain the workability of SAL. This proposed logic scheme can be used in future energy-saving embedded circuits and mainly for energy efficient devices where ultralow power and longevity are the pivotal issues.

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