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Design of Low Power Efficient CMOS Dynamic Latch Comparator

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Abstract: *High performance analog to digital converters (ADC), memory sense amplifiers, and Radio Frequency identification applications, data receivers with less area and power efficient designs has attracted a broad range of dynamic comparators.SAR-ADC is best suited for low power applications where power has a trade-off with speed.Comparator is one of the core components of SAR-ADC that introduces error voltage due to mismatch and consumes large power. This work presents the analysis of various dynamic latch comparators which are there in market and a new comparator has been designed which is optimized to achieve smaller size and less power. The proposed comparators have been designed and simulated using 130nm CMOS 1P2M technology by using mentor graphics tools with a supply voltage of 1V.*

Keywords: *Analog to digital converters (ADC), CMOS, Dynamic latch comparator, memory sense amplifiers, Radio frequency identification.*

I. Introduction

Due to high-speed, less-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators[1] are very attractive for many applications such as high-performance analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. A small input-voltage difference is converted into full-scale digital level in a short time by using the positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in conventional dynamic latched comparators. However, the accuracy and the performance of the dynamic latched comparators is restricted by the random offset voltage witch results from device mismatches such as threshold voltage V_{th}, current factor β ($=\mu_{Cox}W/L$), and internal-parasitic/external load capacitance mismatches [2],[3],[4]. The most important design parameter in designing dynamic latched comparator is offset voltage[5],[6] which shows a large effect on performance of the comparator. in Fig. 1, shows the block diagram of high speed comparator which consists of pre-amplifier and regenerative latch stage. The pre amplifier stage is used to decrease the latch offset voltage and it can also amplify a small input voltage difference to a large output voltage. This large output voltages to overcome the latch offset voltage which in turn reduces the kickback noise [7]. There will be large static power consumption for large bandwidths because of the pre-amplifier stage and the intrinsic gain also reduced due to the reduction of the drain-to-source resistance ($r_{ds)}$ due to the continuous technology scaling [8]. Therefore, for the high-performance CMOS applications, a dynamic comparator without pre-amplifier stage is highly desirable. The conventional comparators suffer a lot of accuracy issues like random offset errors and internal parasitic/external load capacitances mismatches [2],[3],[4]. To overcome this inaccuracy issues and to improve the performance dynamic latch based comparators without preamplifier stage are preferred [7]. For an analog to digital converter with a feature of high-performance, a comparator without the pre-amplifier is preferred since it suffers from high static power dissipation [9].

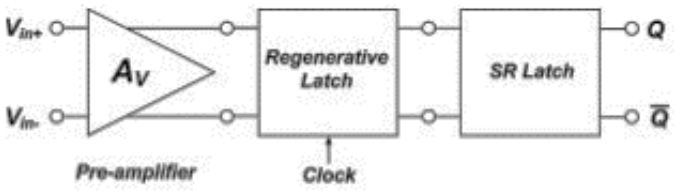

Figure 1 Typical block diagram of a high speed voltage comparator.

In this paper the sections are considered as follows: Section II offers an overview of the dynamic latch comparators and also discuss about their advantages and downsides, and Section III describes the proposed

dynamic latched comparator and their operation. Section IV discusses about simulation results and section V concludes the paper.

II. Dynamic Latch Comparators

The dynamic latch comparator is shown in fig. 2(a) is most widely used because it has many advantages such as high-speed, zero staticpower consumption, high input-impedance and full swing output [10],[11]. During the pre-charge phase both the output, nodes are charged to power supply voltage and during the evaluation phase the output of the comparator depends on the differential input. The main drawback of this comparator is it consists of only one tail current transistor M11 which is used to control the currents flowing through both the differential input pair (M10 and M5) and the latch (M3,M4,M8,M9). The size of the tail transistor M11 should be increased to increase the drive currents of the latch. But, if we increase the size of the tail transistor M11, the time duration of the input transistors which operate in the saturation region will be reduced. Because the transistors operate less time in the saturation region, full amplification of input voltage is not achieved.

To avoid these downsides, the comparator is designed using separate differential inputgain stage and outputlatch stage which are shown in Fig. 2(b) [12]. Due to this stage separation, the comparator will be operated at the low supply voltage (V_{DD}) and can also have stable offset voltage and increased speed. When the clock is low both the output nodes discharges to ground, and when the clock is high, the output depends on the differential input node voltages. The main pitfall of this comparator is it uses both clock(clk) and clockbar (clkb) signals, for proper operation of the circuit accurate timing relation must be maintained. Due to the effect of clock skew between Clkb and Clk signals the performance of the circuit is affected. In additional to the clock signal clkb signal is used which an additional inverter to generate the clock needs signal Clkb which leads to increase in area, power and delay. If Clkb is lagging the Clk, it leads to increased delay, and If Clkb is leading the Clk, it results in increased power dissipation.

The comparator 2 from [14] is shown in Fig. 2(c), where the Clk skew problem is eliminated by replacing Clkb with differential nodes. With the elimination of clock skew problem, the performance of the comparator is not affected, and the load due the clock is also reduced. Due to the presence of large differential nodes capacitance and double transconductance(g_m) the noise and input referred offset voltage are reduced. But the main drawback is increased delay due to the weak current driving capability of the output load due to the fact that the transistors M1 and M2 uses differential node voltage, which shows the slow exponential decaying shape. Since the single tailcurrent transistor (M1) in the comparator 1 of Fig. 2(b)is divided into two transistors (M1 and M2) in the comparator 2(c) of Fig. 2 the drive current of the output node is reduced to half.

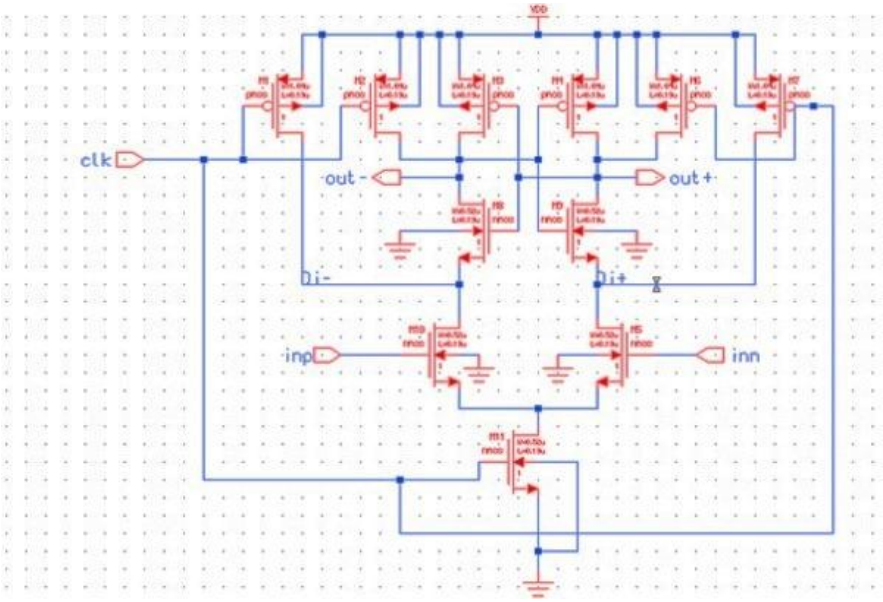

Figure 2 (a) Conventional dynamic latch comparator [10],[11]

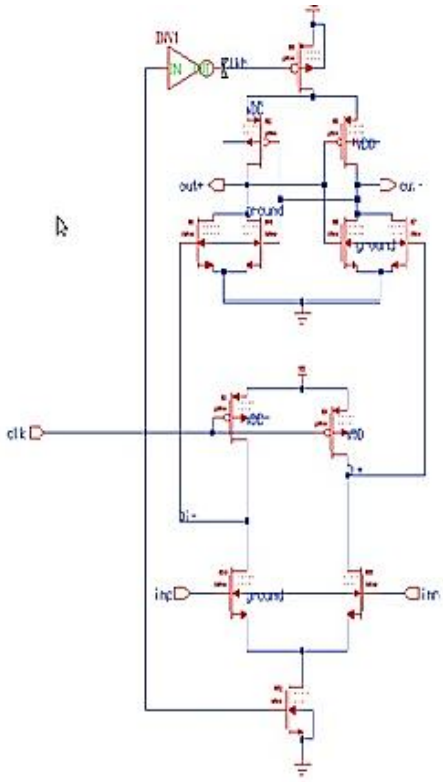

Figure 2(b) Comparator 1[12]

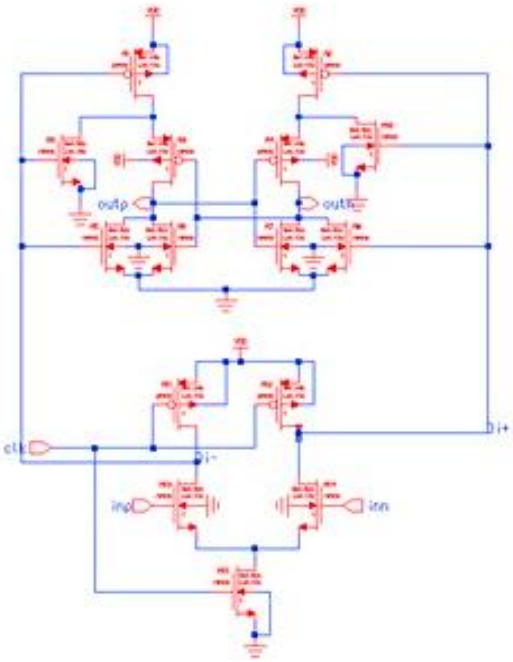

Figure 2(c) Comparator 2[7]

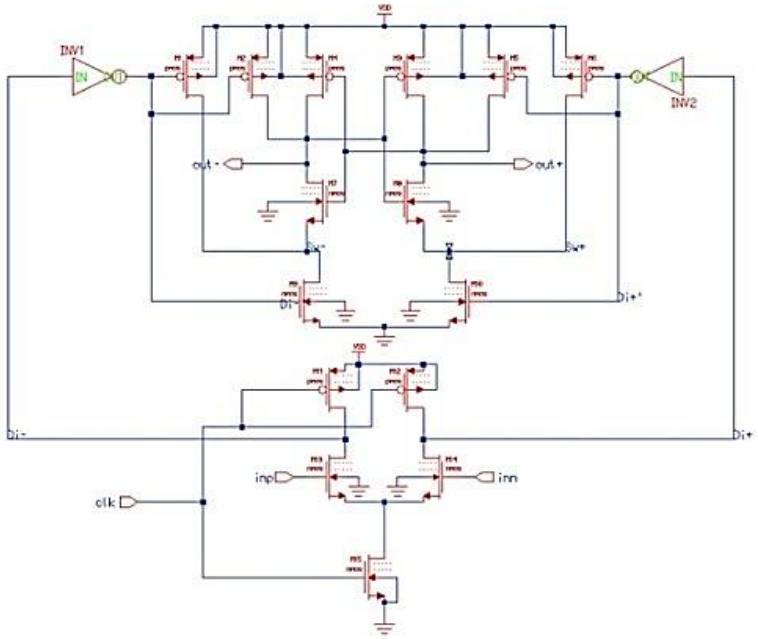

Figure 2(d) Comparator 3[1]

The comparator 3[1] provides less input offset voltage and used to attain high performance when compared with the previous comparators. The output nodes of the comparator are charged to V_{DD} during pre-charge (or reset) phase (Clk= 0 V). During the evaluation phase, comparison of the input voltage takes place, and the output depends on the magnitude of input voltage. The main advantage of the comparator3 is it can deliver bigger load currents and can also operate at lower power supply voltages. The main drawback of this comparator is it require more time to reset the output nodes to supplyvoltage which slower the process of comparison which in turn limits the speed of comparator.

III. Proposed Comparator

The proposed comparator is shown in Fig. 3(a). When the clock is low, the M7 pre-charges the nodes D+ and D- to V_{dd}-V_{gs}. This voltage drives the two inverters connected to it discharging the OUT+ and OUT- to ground potential.

When the clock goes high M12 becomes on, and the transistors M10 and M11 startdischarging the nodes D+ and D- proportional to the applied input voltage IN+ and IN-. When this voltage falls below V_{th} of M1 and 2, these transistors start switching on at a rate proportional to the rate at which the input voltage discharges the nodes Di+ and Di-.With the increasing input voltage difference M1 and M2 turn on one after the other and the cross-coupled nMOS pair made by M5 and M6 starts regenerating the small voltage difference transmitted from Di nodes into a full-scale digital level. Instead of applying clock directly to the latch, he latches regeneration phase and reset phase were set by the node voltages Di+ and Di-.

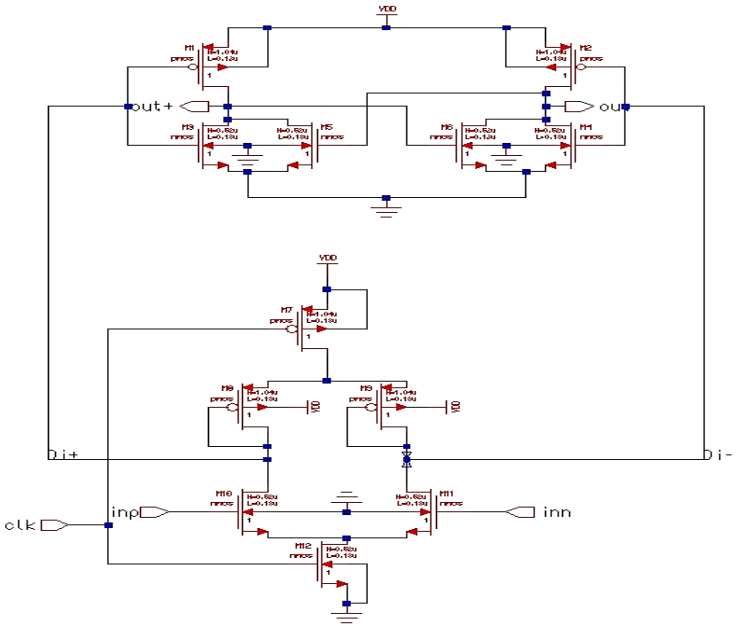

Figure 3(a). Proposed dynamic latch based comparator

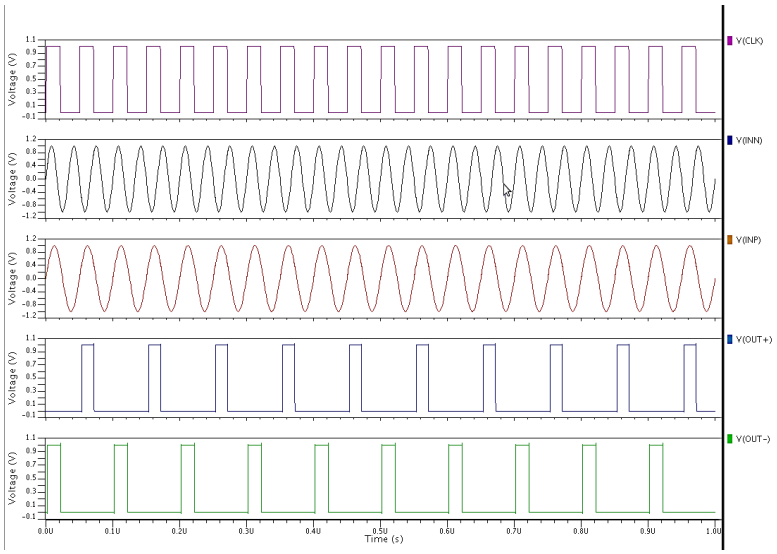

Figure 3(b). Transient response of the proposed comparator

Fig. 3(b) shows the transient response of the proposed comparator, the sinusoidal signal is given as input for both inputs INN and INP with variable frequency and the same amplitude. During pre-charge phase both the output nodes charge to V_{DD} and during evaluation phase the output depends on the differential input voltage.

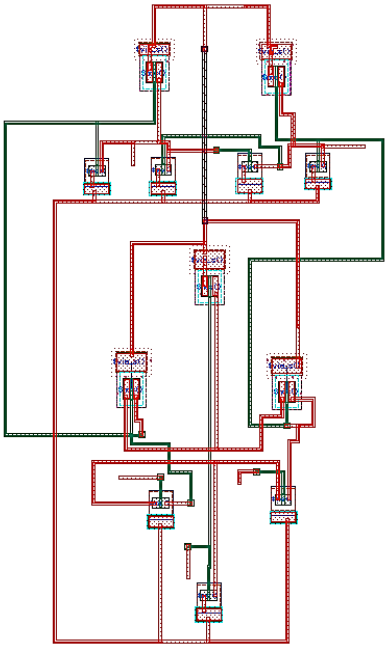

Figure 3(c). Layout of proposed dynamic latch comparator

IV. Simulation Results

In order to compare the proposed comparators with the modified comparator, all circuits have been simulated in 0.13µm CMOS technology with VDD =1V. TABLE 1 compares the performance of the proposed comparator with different comparators.

Table 1 Comparison of different comparators

Specifi-cation	Conventional dynamic latch comparator	Compar-ator1	Compar-ator2	Compar-ator3	Proposed comparator
Technology	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS
Supply voltage	1V	1V	1V	1V	0.8V
Number of transistors	11	14	15	19	12
Delay	21.09ns	1.9ns	2.5ns	31.93ns	37.24ns
Power dissipation	0.5nw	0.725nw	0.9nw	3.09nw	1.6nw
Area	17.36µm X 12.995µm	22.63µm X 26.045µm	24.72µmX 26.47µm	41.36µmX 36.56µm58	18.9µmX3 2.01µm

V. Conclusion

The proposed comparators are designed and simulated using 130nm CMOS 1P2M technology. Different architecture of comparators was studied and analyzed as per the power consumed, speed and size of the comparator. The proposed comparators can be used to drive large capacitive loads by using only one phase clock signal. The dead time required to reset the output nodes was also removed by the proposed designs in the input differential stages. The simulation results show that the proposed comparators achieve low power and less area when compared to the conventional comparators at the approximately same area.

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