

An Efficient PG Planning with Appropriate Utilization Factors Using Different Metal Layer

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Abstract: *In this paper the effects of choosing a proper Utilization Factor on total wire length, time to place & route and DRC violations have been explained clearly. In addition, how the number of metals layer used to route between the standard cells will affect total wire length, and number of DRC (Design Rule Constraints) violations and time to place and route at different utilization factors has been studied. It's observed that If the design has high utilization factor then power planning should be done on higher metal layers to avoid DRC violations and less time to place and route*

Keywords: *Floor Plan, PG planning, Place and Route, Utilization Factor. Time to Place & Route.*

I. Introduction

In VLSI Physical Design (PD), one of first and most fundamental step is floor planning. The rest of the PD, mainly placement of standard cells, congestion and timing are as good as our floor plan. An important step in floor planning is to specify appropriate core area to place standard cells and macros also to decide appropriate metal layers to do Power and Ground planning. In general floor plan can be specified in terms of 1. Aspect ratio (height / width) and dimensions of the core 2. Utilization Factor (UF) 3. in terms of die area

In this paper, how to choose the best utilization factor for a design, which metals are generally preferred for Power and Ground planning and situations where PG planning is done on lower metal layers, but still making the design routable are discussed. Here a timing driven of standard cells placement is done and a 6 layer metal process is used.

Here the experiments are mainly classified into two phases: **Phase 1** is the Lower metal layers (M1 and M2) used for PG planning. **Phase 2** is the Top metal layers (M5 and M6) used for PG planning. Here all the simulations are done on Cadence ® Soc-Encounter RTL-to-GDS II system, Version 9.1

II. Phase 1: Using Lower Metal Layers

In this phase we use lower metal layers such as Metal1 (M1) and Metal 2 (M2) for Power and Ground planning. For Core power rings (VSS and VDD) we use M1 and M2, where the top and bottom rings are placed on M1 (Horizontal Layer) and the right and left rings are placed on M2 (Vertical Layer) with a width of 4.8 microns and a spacing of 1.8 microns. Vertical power stripes are placed on M2 with a width of 4.8 microns, spacing of 1.8 microns and a set to set distance is 33 microns. Special route for follow pins to connect VSS and VDD pins of all the standard cells is done on M1. Fig.1a. shows the PG planning of phase1 for a particular Utilization Factor.

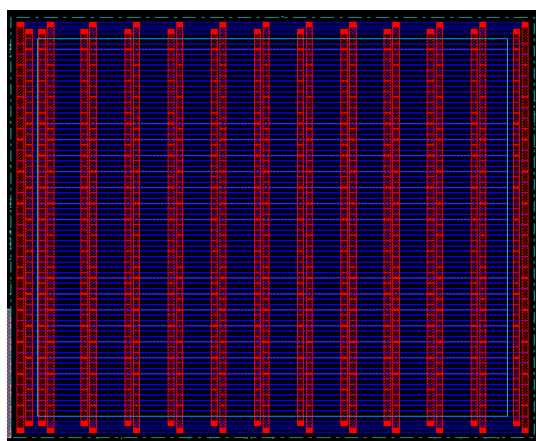


Fig.1a. Chip with PG planning done on M1 and M2 layer

Power planning Lower and metal layers(M1& M2) max routing layer 5					
Utilization Factor	0.3	0.4	0.5	0.6	0.7
	0.8				
Total Wire length (μm)	161061	136943	133734		
	126403	101744	96500		
Total No. Of DRC	1	8	12	14	
	3759	5479			
Runtime (SEC)	13	13	17	43	88
	154				

III. Phase 2: Using Higher Metal Layers

Power planning with higher metal layers (M5 & M6) and max routing layer 5					
Utilization Factor	0.3	0.4	0.5	0.6	0.7
	0.8				
Total Wire length (μm)	140088	127415	113203		
	105964	97614			
		95757			
Total No. Of DRC	0	0	0	0	0
Runtime (SEC)	7	8	7	10	7

Power planning with higher metal layers (M5 & M6) and max routing layer 6					
Utilization Factor	0.3	0.4	0.5	0.6	0.7
	0.8				
Total Wire length (μm)	141615	131639	116759		
	106360	98094	99250		
Total No. Of DRC	0	0	0	0	0
Runtime (SEC)	10	8	8	7	8

In this phase we use top metal layers such as Metal 6 (M6) and Metal 5 (M5) for Power and Ground planning. For core power rings (VSS and VDD) we use M6 and M5, where the top and bottom rings are placed on M5 (Horizontal Layer) and the left and right rings are placed on M6 (Vertical Layer) with a width of 4.8 microns and a spacing of 1.8 microns each one. Vertical power stripes are placed on M6 with a spacing of 1.8 microns width of 4.8 microns, and a set-to-set distance is 33 microns. Special route for follow pins is done on M1 layer. Fig.1b. shows the PG planning of phase 2 for a particular Utilization Factor. Fig.1c. shows a place and routed chip with filler cells added.

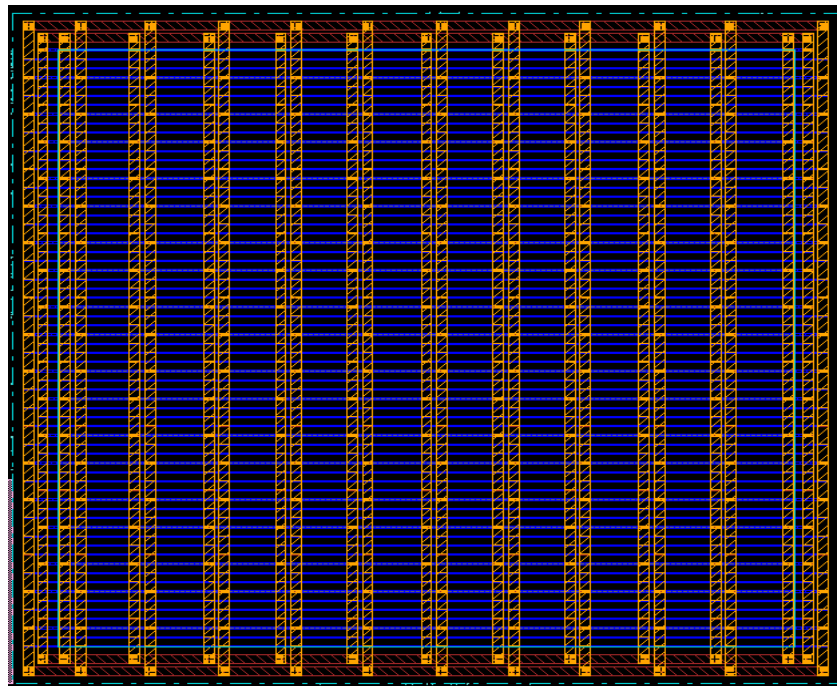
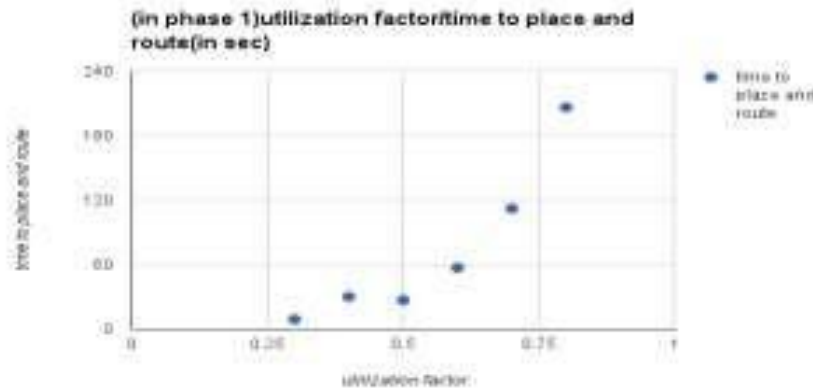


Fig.1b. shows the PG planning of phase 2



Utilization factor VS time to Place & route (phase1)

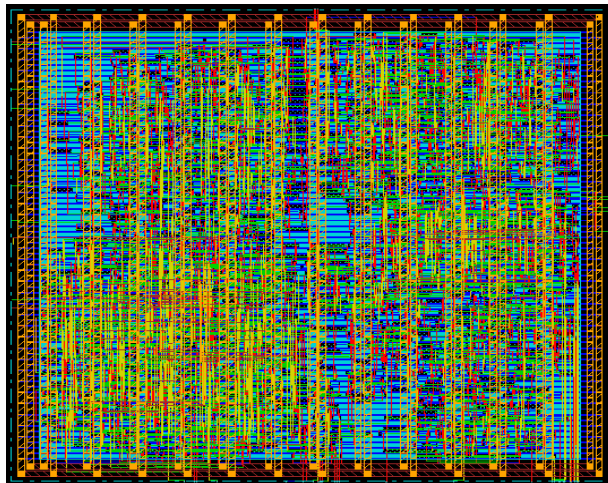


Fig.1c. Place & Routed chip with filler cells added

IV. Experimental Results

These experiments are performed on Cadence® Soc Encounter RTL-to-GDS II system. For each phase, three parameters were observed (1) Utilization Factor versus Total wire length with number of metal layers fixed at 5.(2) Utilization Factor versus total wire length with no of metal layers fixed at 6 (3) Number of Metal layers versus Total wire length with different Utilization factors Also Number of DRC violations, and Time to do Place and Route were also studied.

Utilization factor (UF) is defined as $UF = (1)$

Here the UF is varied from 0.8 to 0.3 and the total wire length used for each value is tabulated. When we say the UF is 0.8, it means we allocate an area of times of the standard cells area, for the tool to place macros, standard cells and do routing between them. Here the number of metal layers used is fixed to M5. Fig. 1d shows the variation of total wire length used for routing for different values of UF.

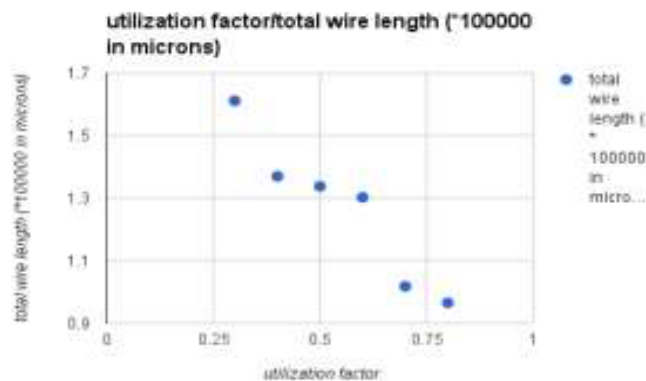
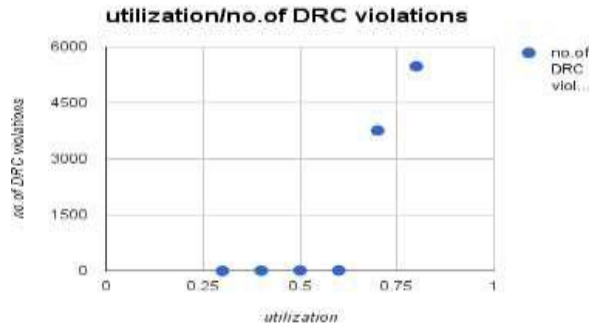
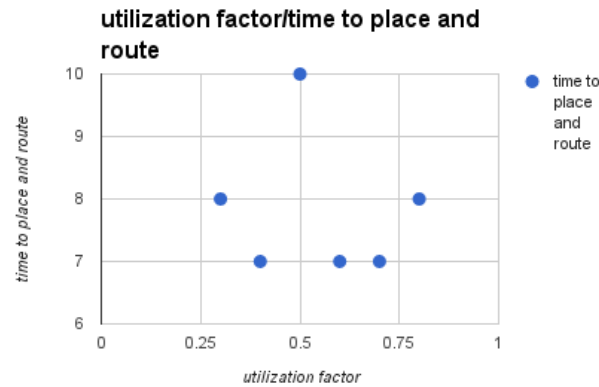


Fig.1d. Utilization factor /total wire length (phase1 & max route layer 5)



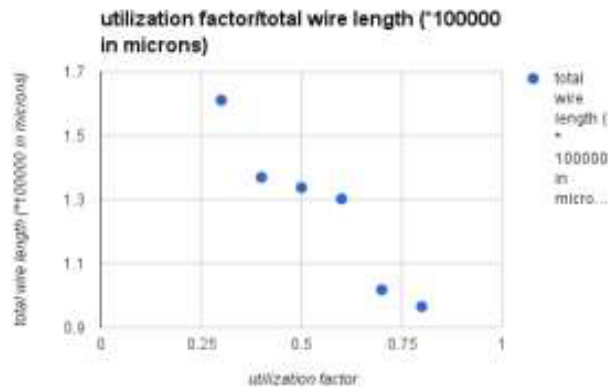
Utilization factor VS total no. DRC in phase1



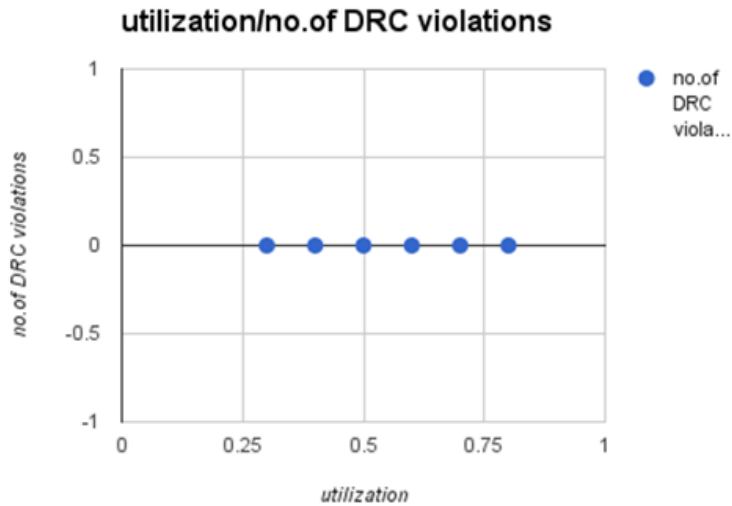
Utilization factor / time to place and route (Phase 2 & max route layer 5)

We observe that for Phase 1 for a UF = 0.8 the wire length is the maximum, gradually decreases till UF = 0.6, increases till 0.4 and then starts decreasing again. This is because in Phase 1 the PG planning is done on M2 and M1 layers and for UF = 0.8 the area allocated is less, so in order to avoid shorts with M1 and M2, minimum amount of routing is done on M1 and M2. Also as the cells are placed very close to each other and in order to avoid min. spacing violations, shorts (DRC violations) between the nets, the tool does a complex, long de-tour routing on M3, M4 and M5 with a preference to M3 (Optimal Metal Layer). As the UF decreases to 0.6 (Optimal distance), the area to place cells increases therefore the tool starts routing the cells with normal routes. As the UF increases to 0.4, the standard cells are unclosed with large distances (more than the optimal distance), so they are routed with longer routes and care is taken to avoid maximum DRC violations for which top layers are used. For UF of 0.3 and beyond, even though the tool has a lot of space to place the standard cells and route between them, it prefers not to do so, to meet timing (as it is a timing driven placement).

In Phase 2 as the PG planning is done on M5 and M6, the tool does majority of the routing on below layers and as the routing is done on lower layers, complex de-tour routing is not needed between the cells. As Utilization Factor increases to 0.4, the separation between standard cells also increases, therefore longer routes are done (on M2 and M3). For UF of 0.3 and more, even though the tool has a lot of space to place the cells and routed between them, it prefers not to do so, to meet timing. In phase2 M5 and M6 layers used for power planning And max routing layer 5.

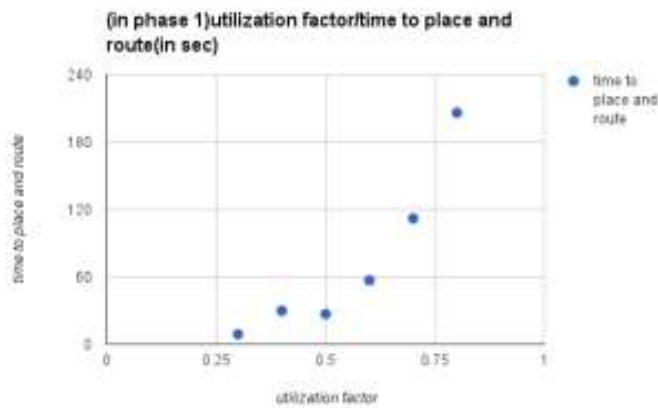


Utilization factor /total wire length in phase 2 and max route layer

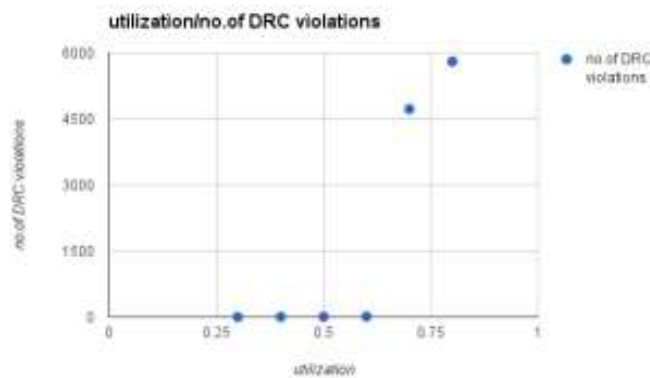


Utilization factor vs. no of DRC violations in phase2 (max route layer 5)

Utilization vs. No. of DRC violations maximum numbers of DRC violations in Phase1 and none in Phase 2. It's because as the power and ground planning is done on lower metal layers (M1 and M2) in Phase 1, there is a lot of minimum spacing violations and shorts, where as in Phase 2 as the PG planning is done on top layers no such problems exist. Also in Phase 1 as the UF decreases, we have more space to place and route the standard cells, therefore lesser the violations.

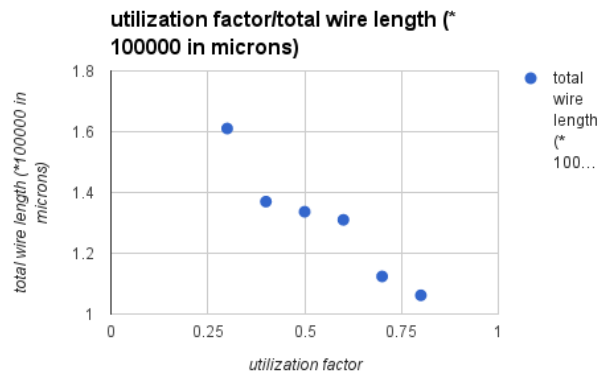


Utilization vs. time to place and route (phase1 & max Routing layer 6)

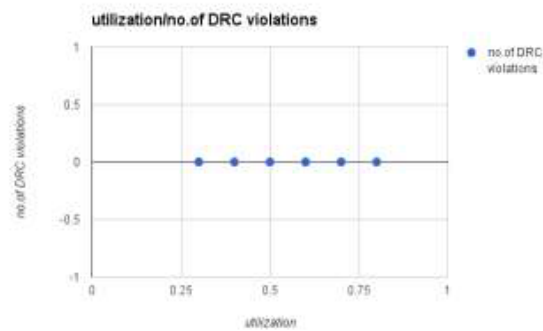


Utilization factor vs. no of DRC violations (Phase 1 & max route layer 6)

From following figures we can see that the time to route between the standard cells is very large when compared to time to place the standard cells, this is because in Phase 1 the tool does complex de-tour routing in order to minimize the DRC violations. But in Phase 2 as power and ground planning is done on top metal layers and as there are no DRC violations the tool can place the standard cells very easily.

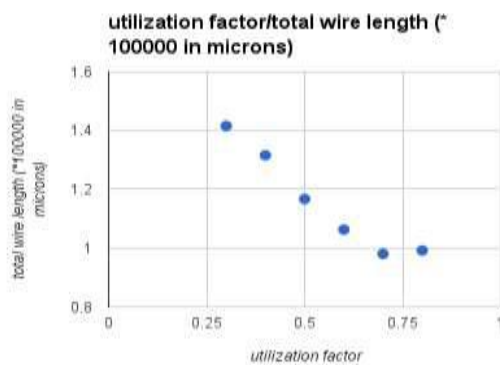


Utilization factor /total wire length (phase1 & max route



Utilization factor vs. no. DRC violations (Phase 2 & max route layer 6)

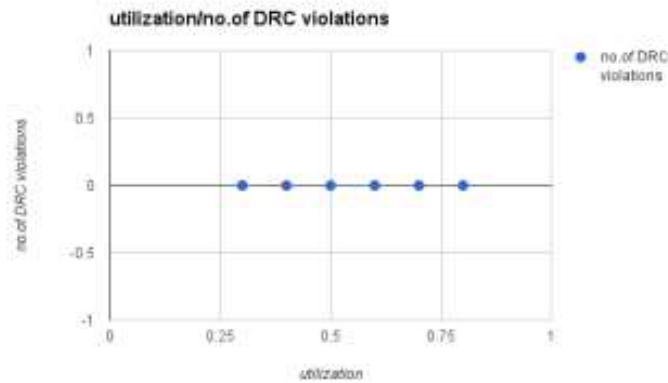
Here we use all 6 metal layers to do routing. From Figures, we observed the Utilization Factor decreases i.e. as the Available area increases the amount of metal 6 used for decrease the routing area in both Phase 1 and Phase 2. By this we can say that the tool uses higher layers for routing only when required (as in Phase 1 with Utilization factor is 0.8, to avoid DRC violations higher layers are used) and prefers the and middle and lower layers for routing between the standard cells. The same can be observed from the later two figures it is also noticed that M1 is sparsely used for routing as it is mostly used within the standard cells.



Utilization factor vs. total wire length (phase2 and max route layer 6)

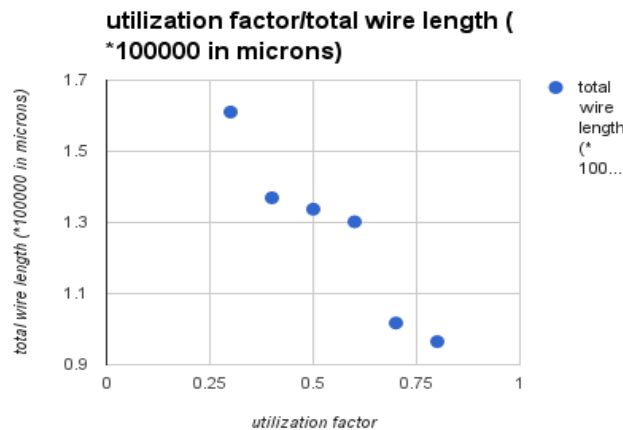
Total wire length versus no. of metal layers used

From the experimental results we can infer that by using fewer number of metals to route between the standard cells placed across the core area the tool has to do complexes de-tour routing i.e. used long nets, to avoid DRC violations. But when more number of metal layers are at the tools disposal, it can route between far away cells by switching to top metal layers instead of a long nets, same metal layer routing. In this way it can also avoid DRC violations. The same can be observed. We can observe that when less numbers of metals are used the tool tries to move to the highest possible layer to avoid DRC violations for every route, therefore we see more number of vias when we use only 2 metal layers. But as the metal layers increase the tool tries to balance between higher metal layer switching and same metal layer routing, therefore the number of vias reduce. Also when more number of layers are available for the tool, it tries to use all layers, (but to the minimum extent possible) therefore the via count increases.



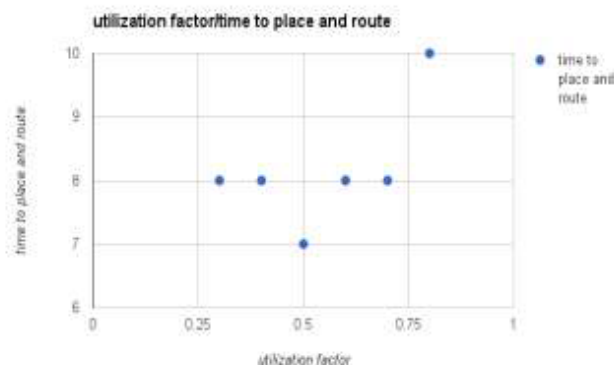
Utilization factor VS no. of DRC Violations (Phase 2)

From above figures it can be observed that with fewer number of metals layers available for the tool it's not possible for it to avoid DRC violations, but as the number of layers increase it has the option of moving to higher metal layers and avoiding DRC violations, therefore these Violations decrease with an increase in the number of metal layers used for routing.



Utilization factor VS total wire length

From above figures it can be observed that as placement of standard cells is independent of the number of metal layers that are used for routing, time taken to place the cells is almost constant in Phase 1 and Phase2. In both these phases when two metal layers are used for routing, time taken is more as complex detours routing is done to minimize DRC violations. But in case of detailed routing for Phase 1 the time taken to do increase the routing with an increase in the number of metals. The reason for this is, in order to avoid DRC violations with M2 power stripes an optimal usage of M2 and M3 metals must be done, which results in more time. In case of Phase 2 as PG planning is done on higher layers, the routing time between the cells decreases. In both phases the sudden decrease in the time taken to route using metal layer 5 is strange and will be explored in a later paper.



Utilization factor vs. Time to do PNR (Phase 2)

V. Conclusion

Choosing with an appropriate Utilization Factor, power planning with appropriate metals and sufficient number of metal layers to route between the standard cells is very important. If the number of DRC violations more than time to PNR (place and route) more. DRC violations should be clear to decrease the DRC violations the PG planning should be perform on higher layers only at higher utilization factors .if the DRC violations less then time taken to place and route also less.

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