IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 6, Ver. III (Nov. – Dec. 2016), PP 45-51
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Dual Port 5T SRAM with High Read Stability

Pooja Saha

UG Student, Dept. of ECE Banasthali University, Jaipur Rajasthan, India

Abstract: *This paper is based on design and analysis of proposed 5T SRAM which consumes low power and occupies less area compared to conventional designs. Proposed design consumes less power as dedicated bit line is charged for write and dedicated bit line for read operation. To ensure stability of the cell and reduce flipping of the contents during read operation, dedicated circuit is used with separate discharge path for read bit line. Proposed design is stable for read, write and hold. Conventional 6T SRAM also shows good stability, proposed design has been analyzed for read/write delay and Write Noise Margin (WNM). The simulated results for read 0, write 1, write 0 are 0.30 ns, 0.17 ns and 0.41 ns, respectively. This design is highly stable for read operation as WNM is found to be 0.79 V which is more than conventional 6T SRAM for same size. The minimum WNM is found to be 0.79 V at an width of pull up =240 nm and pull down=180nm.*

I. Introduction

Scaling factor is a major issue with the moving of technologies to nanometer scales, such as 28 nm, 16 nm, and 10 nm etc. Along with this scaling factor, achieving or maintaining performance, power, and area also gained as a major issue for VLSI Engineers. Especially, a high density design, which consumes more power, then increases the temperature of the circuit. Due to this high dense circuits, obtaining the low power is a major issue for designers. Low power VLSI circuits are in demand because of the growth of battery powered portable devices such as smart phones, tablets, etc., without or with less trade-off for performance and area.

For every digital CMOS circuit, memories constitute a major portion for storing the information. Memory cell is the basic building block of memory. Memory cell consumes power when it is in active mode, leakage and dissipates more power; memory bit cell is designed using transistors for low power and high reliability and less noise susceptibility. SRAM is the random access memory which retains the data contents as long as the power is applied. SRAM is the most popular memory used in digital circuits. Conventional 6T CMOS SRAM, feature very low noise and read signatures, can be designed to have extremely low standby power consumption for hand-held devices. In general, low power memory cell uses transistors (6T) SRAM to reduce power consumption. Low power 6T SRAM cell has been used in [1] and [2] for low power applications. Conventional 6T SRAM also shows good stability at very small feature size with low power supply. During the read operation, the stability drastically decreases due to the voltage division between the access and driver transistors. Read stability can be improved by using dedicated circuit for read operation. Write ability is mentioned, either of a bit-cell can change from '0' to '1' or vice versa. During the write operation, one of the bit line is charged either for write '0' or write '1' [1]. This paper proposes new architecture to replace 6T SRAM, which has less no. of transistors compared to 6T with reduced bit line capacitance. The proposed design also increases the read stability. Proposed design consumes less power as single bit line is charged for write and read operation. This design is developed using CMOS 130 nm technology to keep low power consumption.

II. Background

A. Literature review:

The traditional 6T SRAM is composed of two cross coupled CMOS inverters with two pass NMOS transistors connected to complementary bit-lines. Pass transistors are connected to Word line (WL) and control the access to bit-cell.

Figure 1 Conventional 6T SRAM

Both *read and write* operation is desired through bit line capacitor. A 5T bit cell has two bit lines and hence energy requirement to charge the bit lines capacitance is more. During charging and discharging of capacitor, half of energy is dissipated as heat as ½ CV^2. Since it uses 6 transistors more power is consumed during its switching, which increases dynamic power consumption of the circuit. Hence, reduction in the number of transistors and bit lines involved in read and write operation reduce power consumption and area occupied by the cell. Hence, 5T SRAM is preferred over 6T SRAM.

Stability during read '0' is another major issue for conventional 6T design. Driver transistors are made stronger than access transistors to maintain stability and avoid flipping of stored bit. Maintaining cell ratio for 6T SRAM is a major issue. Cell ratio is the ratio of pull-down transistor to access transistor. Alteration can severely impacted by device variations, thus degrading the stability and noise margin [2].

Many design techniques have been proposed to reduce the bit lines and transistors used in the bit cell and improve stability during read and write operation. In 5T SRAM, the number of bit lines and transistors used in the bit cell are reduced. Read '0' and '1' both have different power consumption as bit line is not discharged during read '1'. Balance between access transistor and pull-down transistor is inevitable because access transistor is used for both read and write operation. Pull-down transistor is made stronger than access transistor to sink and pull-down transistor is strong. Reverse is the case during write operation, access transistor is strong and pull-up is strong for higher stability. 5T SRAM functions same as 6T SRAM but this design is advantageous in terms of area and power consumption. Area consumption reduces by one transistor and one bit cell and similarly reducing the case of pre-charge circuits. In 5T transistor, read and write are separate.

B. Fully depleted silicon-on insulator

The basic bulk devices are facing following limitations in nanotechnology devices:

- Short channel effect
- Carrier reduction because of impurity scattering in substrate that leads to variable performance of same transistor and increase in threshold voltage
- Increasing leakage or junction
- DIBL effect
- High speed can be achieved by increasing the operating voltages, but, that may result in hot carrier effect

Many researches are taking place in universities and R&D development center's all over the world to overcome the above mentioned limitations and Silicon-on-Insulator (SOI) is the one of the promising solution to overcome such limitations.

In Silicon-on-Insulator technology, active regions are electrically isolated from the substrate through buried oxide layer of about 400 nm thick, which results in less capacitance, reduced sub zero-rate, increase in speed, reduced power consumption, and higher density. SOI technology offers unique solution to the field of low voltage, low power, and high speed designs. SOI is classified as:

- Partially depleted SOI (PDSOI)
- Fully depleted SOI (FDSOI)

In FDSOI devices, a layer of insulator is used to isolate the body and transistor region. This reduces the formation of depletion region and hence, the capacitance. The thickness of the silicon layer is very low, which increases the performance of the device. Since no carrier exist in depleted region, gate fully controls the sub threshold current and exhibits steep sub-threshold characteristics. There is no floating body effect in FDSOI

Figure 2 FDSOI transistor [4]

In FDSOI devices, a layer of insulator is used to isolate the body and transistor region. This reduces the formation of depletion region and hence, the capacitance. The thickness of the silicon layer is very low, which increases the performance of the device. Since no carrier exist in depleted region, gate fully controls the sub threshold current and exhibits steep sub-threshold characteristics. There is no floating body effect in FDSOI

devices since the impurities are not added in channel and class channel effects. For FDSOI (Fully Induced Device Scattering) are also reduced compared to CMOS circuits. SRRC refers to sub threshold cutoff due to high effect of drain electric field. Considering FDSOI devices, there is negligible charge sharing between drain and body because body is fully depleted and drain no longer effects threshold voltage [5].

Although FDSOI offer several advantages, it has some disadvantages like self-heating, series resistance, and floating body effect. Self-heating occurs because of the BOX layer. Since BOX layer is thicker in FDSOI for 28 nm, 14 nm, and 7 nm technology to reduce the issues present in conventional FDSOI. UTBB technology uses thin layer of buried oxide of about 25 nm, this offers the advantage for the heat to dissipate and reduce self-heating. Also, the floating body effect is less in FDSOI because drain are reduced and height is increased, this reduces series resistance and allows the positioned 5T variability.

III. Proposed Design

C. Proposed 5T SRAM

The proposed 5T SRAM cells uses dedicated bit line for read and write operation. Data is stored in single bit line and access transistor is used for pulling out data from the storage node.

For stable read operation, one additional access transistor (T3) is used, one transistor (T2) and another is, driver transistor (T1) which provide separate discharge path for the read bit line while reading and does not affect the storedbit in the bulbs. Major advantage of the architecture is safe read without flipping the read value using 5 transistors.

Figure 3 Proposed 5T dual port SRAM cell

D. Memory Cell Operation

HOLD: Write value at node 'A' is '1', T2 remains ON and value at node 'B' is '1' (B= Vdd). T1 remains OFF and blocks the discharging path for B to the ground (GND). Since NMOS (T2) has large value of electron mobility than PMOS, it drives more current and '1' is fetched up till power is supplied. If the value at node 'A' is '0', T2 is OFF and T1 is ON and value stored at node 'B' is '0'(B=GND).

WRITE: When WL = 1, access transistor T3 is enabled and bellow (WBL) voltage is discharged to node A, which turns on T2 transistor. Since T2 is on, node B will be connected to supply voltage and it retains 1.

Similarly, when WL = 1, WBL is charged to Vdd, which turns on node A, which turns on T1 transistor. Since T1 is on, node B will be connected to ground (GND) and it retains 0.

READ: During read '0' or read '1', RBL (Read Bit Line) is pre-charged to Vdd using precharge circuit and removed when RL (Read Line) is enabled.

During read '1', RBL is precharged, RL is enabled. T5 is ON and T4 is OFF and no path exists for the RBL to discharge to GND. Since T5 is ON, RBL is not discharged and it shows '1' after a particular read time.

During read '0', value stored at B is '0', it turns ON PMOS (T4) and RL is enabled that turns on T5 transistor. Since T4 and T5 is turned on while reading '0', RBL is discharged to GND through T4 and T5 and it does not affect the value or storage node B. RBL is discharged and then, it reads '0' after a particular read time.

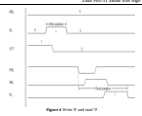

WL
BL
QT
PE
BL
BL
1
0
1
0
1
0

Table 2 Stability of PMOS Pull-downs (180 nm, Vdd = 1 v)

Pull-down width (nm)	SNM (Read Stability) (mV)
300	200
350	200
400	200
450	200
500	200

Considering the above analysis for SNM, Width of the pull-up is chosen to be 200 nm and width of pull-down to be 300 nm for better stability results.

IV. Simulation Results

F. Delay calculation

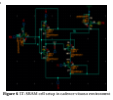


Figure 6 ST SRAM cell array in cadence vision environment

A delay in SRAM bit cell is due to switching time taken by the bit cell to process the input. In the proposed design, writing involves switching the storage node and reading involves discharging the read bit line. Delays in SRAM are mainly consistent:

- Write delay
- Read delay

Write delay: Delay between the assertion of word line and the time when data is actually written on the storage node (B as shown in **Error! Reference source not found.**). It is calculated when word line reaches 50% of its peak value and B1 (Storage Node Line) reaches 50% of its peak value.

Read delay: Delay between application of read line (R1) and the time taken by the read bit line to discharge during read 'ST' operation. It is calculated as the time delay between Read Line (R1) reaching 50% of its peak value and RB1 (Read Bit Line) is discharging 50% of its peak value.

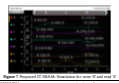


Figure 7 Proposed ST SRAM: Simulation for write '0' and read '0'

Figure 8 Proposed ST SRAM Simulation for write '1' and read '1'

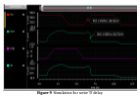


Figure 9 Simulation for write '0' delay

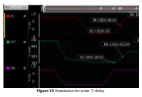
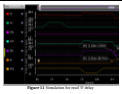


Figure 10 Simulation for write '1' delay


Name
Value
Cursor 1
Cursor 2
Delta
BL
BLB
WL
Q
QB
RBL
RWL
0.000
1.000
0.000
0.000
0