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Programmable Pseudorandom Test Pattern Generator For BIST Implementation

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Abstract: *This paper describes a low-power (LP) programmable generator producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in-self-test(BIST)-based pseudorandom test pattern generators. It is comprised of a linear finite state machine driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. State of the development in the semiconductor manufacturing process, integrated chip design methodology, availability of thousand plus pin integrated circuit packaging options and efficient IC test techniques have contributed immensely towards the integration of entire system on a chip. The System-On-Chip (SOC) devices can have multiple microprocessors, various types of memories such as SRAM, Flash, Digital Signal Processors, many IP blocks and user defined logics. Numerous SOC test techniques have been innovated in the last decade to test complex mixed signal systems on a chip in a cost effective manner. Test industry has made complete strides in developing new automated test equipment which can analog components, test logic, memory of the chip through external interface to the IC. Here with the experimental results with presence of switching activity in PRESTO, Fully operational PRESTO power comparison is performed with LP Decompressor.*

Keywords: *PRESTO, Switching activity, LFSR,BIST, Scain Design, LP Decompressor*

I. Introduction

Whereas over the next years, the primary goal of manufacturing test will remain essentially the same to undergo a significant evolution ensure reliable and high quality semiconductor product conditions and consequently also test solutions. The design process, semiconductor technology and design characteristics are among the key factors that will impact this evolution. One will have to provide the desired test quality for the next technology nodes such as 3-D with new types of defects, it is appropriate to pose the question of what matching design-for-test (DFT) methods will need to be deployed. Test compression, introduced a decade ago, has rapidly become the main stream DFT methodology. However, it is unclear whether test compression [1]will be able of coping with the rapid rate of technological changes over the next decade. Logic built-in self-test (LBIST), basically developed for board, system, and in-field test, is now gaining accession for production test as it avails very robust DFT and is used increasingly often with test compression. This approach seems to be the next evolutionary logical step in DFT. It has potential for improved test quality; it may augment the abilities to run at-speed power aware tests. It can reduce the manufacturing test cost while preserving all LBIST and scan compression advantages.

Attempts to overcome the congestion of test data bandwidth between the tester and the chip have made the concept of combining test data compression a vital research and development area of LBIST. In particular, several hybrid BIST schemes store determined top-up patterns (to detect random pattern resistant faults) on the tester in a reduced form, and then use the existing BIST hardware to attain back these test patterns [6],[7]. Some solutions embed deterministic stimuli by using compressed weights or by disturbing pseudorandom vectors in various fashions[12],[3],[4],[5] .If BIST logic is used to deliver reduced test data, then basic encoding schemes typically take advantage of low fill rates, as originally proposed in LFSR coding , which subsequently developed first into static LFSR reseeding [10],[15],[16] and then into dynamic LFSR reseeding[2]. In the process of conventional scan-based test, hybrid schemes, due to the high data activity associated with scan-based test operations, may consume more power than a circuit under- test was designed to function under. With overstressing devices beyond the mission mode, minimization in the operating power of ICs in a test mode have been of concern for years [8],[9],[13],[14]. Full-toggle scan patterns may draw many times the typical functional mode power, and this trend continues to grow, especially over the mission mode's peak power. This power induced over-test may result in voltage noise, power droop, or excessive peak power, thermal issues, over several cycles which, in turn, cause a yield loss due to instant device damage, shorter product lifetime.

Several schemes for power reduction during scan testing have been devised. There are certian solutions proposed for BIST to put the power power below a present threshold. For example, the test power can be reduced by checking transitions at memory elements from promoting to combinational logic during scan shift. This is achieved by including gating logic between scan cell outputs and logic they drive .The logic remains transparent during normal operations and capture. Gated scancells are also proposed A synergistic test power reduction method of uses available on-chip clock gating circuitry to selectively block scan chains while scheduling test and planning to further decrease BIST power in the Cell processor. This brief is organized as follows. Section II introduces PRESTO generator, its operation. Section III introduces fully PRESTO generator and its operation. Section IV proposes the test patterns generation with LP decompressor. Section V summarizes the experimental results, power report, synthesis report VI conclusion,references.

II. Prpg Operation

Fig.1 shows the basic structure of existing system (PRESTO generator). An n-bit PRPG connected with a phase shifter feeding scan chains forms a core of the generator producing the corresponding pseudorandom test patterns. A linear feedback shift register or a ring generator can carryout efficiently a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Individually each hold latch is controlled via a corresponding stage of an n-bit toggle control register. As long as its enable input is claimed, the given latch is transparent for data going from the PRPG to the phase shifter, and it is toggle mode. When the latch is disabled, it tracks and saves, for a number of clock cycles, the respective bit of PRPG, is thus feed into the phase shifter (and possibly some scan chains) with a stable value. It is now in the hold mode.

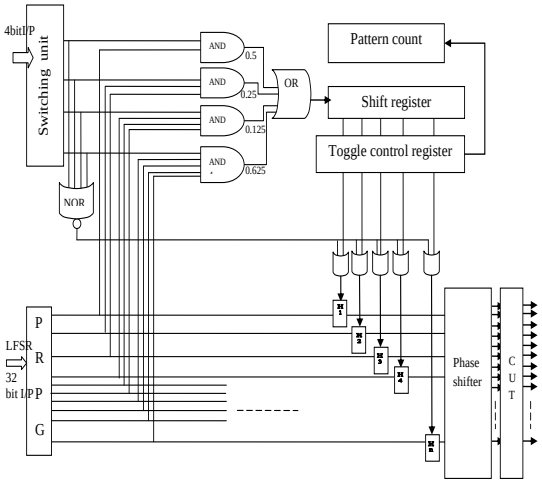

Figure 1 Block diagram of PRPG Operation

It is worth noting that each phase shifter output is attained by XOR-ing outputs of three different hold latches. Hence, each scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output. As mentioned previously, the toggle control register well supervises the hold latches. Its content consists 0s and 1s, where 1s signifies latches in the toggle mode, thus transparent for data entering from the PRPG. Their fraction regulates a scan switching activity. The control register is restored once per pattern with the content of an additional shift register. The enable signals inserted into the shift register are generated in a probabilistic fashion with a programmable set of weights by using the actual PRPG. The weights are determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively.The OR gate allows selecting probabilities beyond simple powers of 2. A 4-bit register Switching is assigned to activate AND gates, and allows choosing a user-defined level of switching activity. For example, the switching code 0100 will set to 1, on the average.25% of the control register phases, and thus 25% of hold latches will be enabled. Given the phase shifter architecture, one can assess then the amount of scan chains receiving stable values, and thus the expected toggling ratio. An additional 4-input NOR gate detects the switching code 0000, which is used to switch the LP functionality off. It is worth noting that when working in the weighted random mode, the switching level selector ensures statistically stable content of the control register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the LP mode, though a set of actual low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable.

III. Existing Work

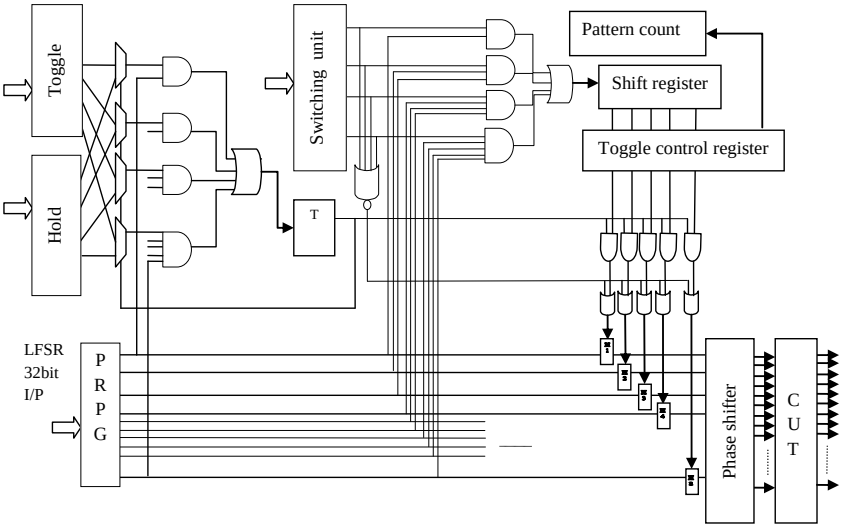

Figure 2 Block diagram of existing work

Section III presents additional features that make the PRESTO generator fully operational in a wide range of desired switching rates.Much higher flexibility in generating low-toggling test patterns can be achieved by deploying a scheme presented in Fig.2. Basically, while preserving the operational principles of the basic solution, this approach splits up a shifting period of each test pattern into a sequence of alternating hold and toggle intervals. To move the generator to and fro between these two states, we use a T-type flip-flop that switches whenever there is a 1 on its data input. If it is enabled to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is well-accomplished by placing AND gates on the control register outputs to allow blocking all phase shifter inputs. This property can be vital in SOC designs where only a single scan chain crosses a given core, and its unusual toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods.If the T flip-flop is fixed to 1 (the toggle period), then the latches enabled through the control register can elapse test data moving from the PRPG to the scan chains. Two additional parameters put in 4-bit Hold and Toggle registers determine how long the entire generator remains respectively either in the hold mode or in the toggle mode. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted logic used to feed the shift register is generated in a manner similar to that weighted pseudorandom signal .The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows choosing a source of control data that will be used in the next cycle to possibly change the operational process of the generator. When it in the toggle mode, the input multiplexers observe the Toggle register, for example. Once the weighted logic output attains 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will stay in this state until another 1 occurs on the weighted logic output. The random result of this occurrence is now compared to the topic of the Hold register, which determines when to terminate the hold mode.

IV. Proposed Work

In order to facilitate test data decompression while storing its actual functionality, the circuitry of Fig.2 has to be rearchitected. This is shown in Fig.3 block diagram of LP Decompressor. The main principle of the decompressor is to disable both weighted logic blocks (V and H) and to place deterministic control data instead. In particular, the data of the toggle control register can now be choosed in a deterministic manner due to a multiplexer placed in front of the shift register. Furthermore, the Toggle and Hold registers are utilized to alternately preset a 4-bit binary down counter, and thus to establish durations of the hold and toggle phases. When this circuit attains the value of zero, it originates a dedicated signal to go high in a way to toggle the T flip-flop. The same signal enables the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flipflop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the down counter, further referred to as an offset, determines that mode's duration.

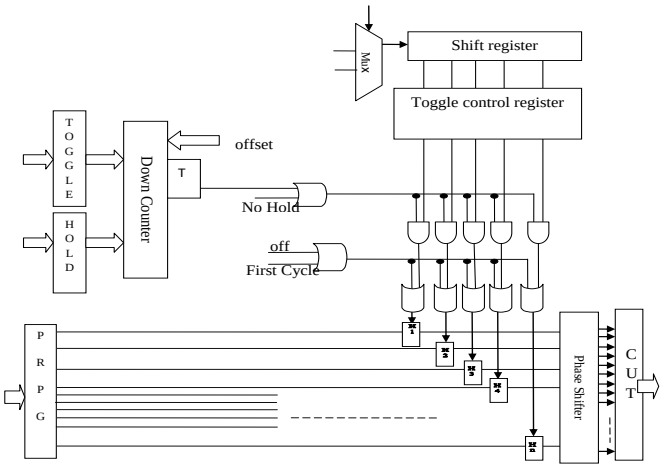

Figure 3 block diagram of Low Power Decompressor

In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle produced at the end of the ring generator initialization phase reloads all latches with the current content of this part of the decompressor. Finally, external ATE channels (feeding the original PRPG) allow one to implement a continuous flow test data decompression paradigm such as the dynamic LFSR reseeding.Given the size of PRPG, the number of scan chains and the corresponding phase shifter, the switching code, the offset, as well as the values kept in the Toggle and Hold registers, the entire decompressor produce deterministic (decompressed) test patterns having a desired level of toggling provided the scan chains are balanced.This LP decompressor is checked with circuit under test c1908.The Phase Shifter 32bit output is feeded into cut.

V. Results

This section presents simulation results obtained for the PRESTO generator shown in Fig.5, Fully operational PRESTO generators shown in Fig.6, LP Decompressor shown in Fig.7. Designs are verified with Benchmark circuit C1908.Involves signalsprpg_out[31:0] prpg input is 32-bit LFSR,switch[3:0] 4-bit switching register, shifter_register[31:0] shifts 32-bit data in parallel in parallel out, toggle_control_reg[31:0]32-bit controlled data istoggled with 1- bit,hold_toggle[31:0]holds the data,ps_out[31:0]a 3-bit e-xored data is phase shifter output,out[24:0]by 32-bit phase shifter output is sent to c1908 benchmark circuit.Hence the power report for all the individual designs is mentioned below in Fig.4. The synthesis report for the designs is shown in Fig.5.

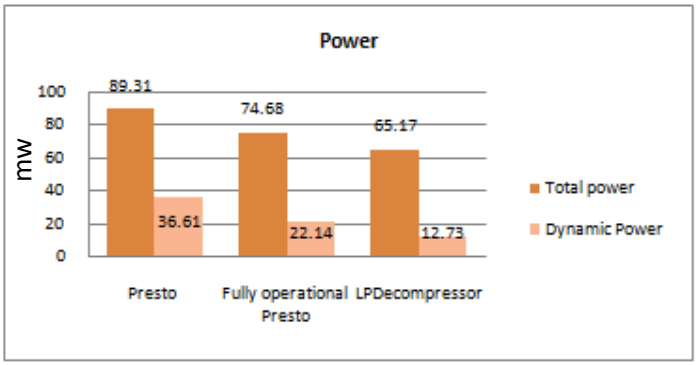

Figure 4 Power analysis of three various designs

Table 1 Synthesis report of three different design

Parameter	Basic PRESTO	Fully PRESTO	LP Decompressor
Number of slices	86	89	89
Number of flipflops	101	110	112
Number of 4input luts	150	158	157

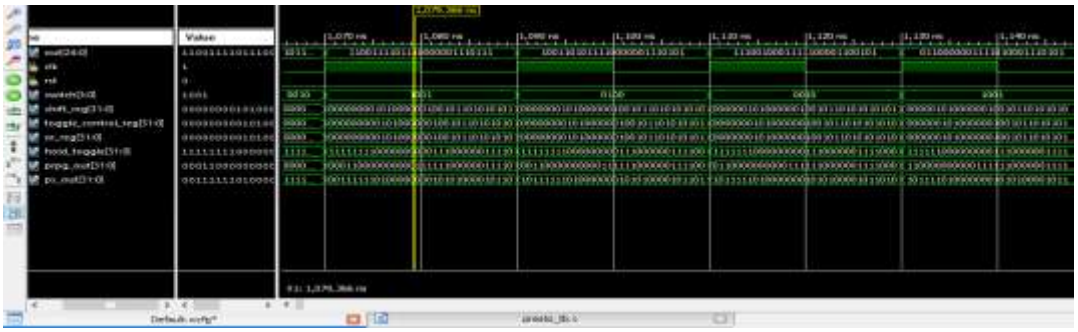

Figure 5 Simulation result of basic PRESTO with switching

Figure 6 Simulation result of fully operational PRESTO with switching

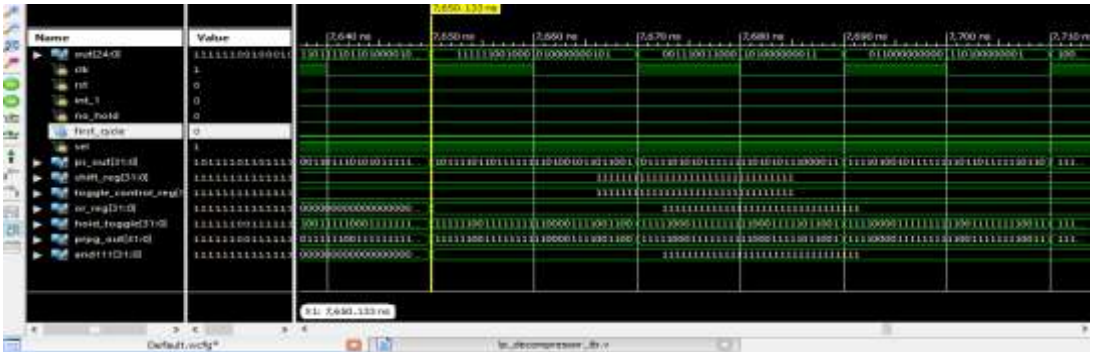

Figure 7 Simulation result of LP Decompressor

VI. Conclusion

PRESTO—the LP generator can produce pseudorandom test patterns with scan shift-in switching activity precisely selected through automated programming. This LP PRPG is also capable of acting as a fully functional test data decompressor with the ability to control scan shift-in switching activity through the process of encoding. The proposed hybrid solution allows one to efficiently combine test compression with logic BIST, where both techniques can work synergistically to deliver high quality test.The same features can be used to control the generator, so that the desired test vectors can either yield a required fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels, or they can offer visibly higher coverage numbers if run for comparable test times.In future application this can be utilized for logic bist test pattern generator with transition controller and multiplier.

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