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Design of 64 bit SRAM using Lector Technique for Low Leakage Power with Read and Write Enable

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Abstract: *In complementary metal oxide semiconductor (CMOS) the power dissipation predominantly comprises of dynamic as well as static power. Prior to introduction of "Deep submicron technologies" it is observed that in case of technology process with feature size larger than 1micro meter, the consumption of dynamic power out of the overall power consumption of any circuit is more than 90%,while that of static power is negligible. But in the present deep submicron technologies in order to, reduce the dynamic power consumption in VLSI circuits, the power supply is being scaled down, keeping in view the principle that the dynamic power dissipated is directly proportional to the square of the supply voltage (Vdd).The threshold voltage also needs to be reduced since the supply voltage is scaled down. Overcoming the inherent limitations in the existing method for leakage power reduction, The Lector (Leakage controlled transistor) technique which works efficiently both in active and idle states of the circuit and results in better leakage power reduction is now proposed. The proposed system presents the analysis of power on "64-bit SRAM array using leakage controlled transistor technique".*

Keywords: *Deep submicron, Low power, Sub-threshold leakage current, Power Gating, Threshold voltage , Transistor stacking.*

I. Introduction

1.1 Preamble

In case of battery powered applications high power consumption results in reduction of battery life, increasing cooling costs and affects reliability and packaging. As such, the power dissipation has become a factor of paramount importance to be considered in the design of CMOS VLSI circuits.

1.2 Main types of power dissipation and sources:

- Dynamic power dissipation: Due to charging and discharging of load capacitance.
- Short Circuit power dissipation: Due to existence of conducting path between voltage supply and ground for a brief period during which logic gate makes transition.
- Static power dissipation: It is the leakage current which consists

(a) Reverse bias diode currents: Due to the stored charge between drain and bulk of activity transistor.
(b) Sub Threshold currents: Due to carrier diffusion between source and drain of the OFF transistors.

1.3 Different concepts of power dissipation:

The short circuit power dissipation can be reduced to 10% of total power dissipation by designing the circuit to have equal input and output rise/fall edge times [1]. Power dissipation due to the switching activity can be reduced by keeping the ratio between the supply voltage and the threshold voltage shall be at least, in order of not affecting the performance of CMOS circuit [2]. This also provides better noise margins and helps to avoid the hot carrier affects in short channel devices [3]. Scaling down threshold voltage threshold voltage results in exceptional increase in threshold leakage current [4].

Need for efficient leakage current power reduction technique: It can be referred from the same concepts that the leakage power dissipation will be equal to the active power dissipation within few generations. Hence the efficient leakage power reduction techniques are very critical in designing deep submicron and nanometer circuits.

II. Existing Techniques

2.1 Power Gating:

A technique for leakage control is power gating, which turns off the devices by cutting off their supply voltage. This technique makes use of bulky NMOS and/or PMOS device (sleep transistor) in the path between the supply voltage and ground [5]. The sleep transistor is turned on when the circuit is active and turned off when the circuit is in idle state with the help of sleep signal. This creates virtual power and ground rails in the circuit. Hence, there is a significant detrimental effect on the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware

capable of predicting the circuit state accurately [6]. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors.

2.2 Sleep Technique:

State-destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors (Fig 1). this technique is Multi-Threshold voltage CMOS (MTCMOS), which adds high-Vth sleep transistors between pull-up networks and Vdd and between pull-down networks and ground while logic circuits use low-Vth transistors in order to maintain fast logic switching speeds[7]. By isolating the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. However, the additional sleep transistors increase area and delay[8]. Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values significantly impact the time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

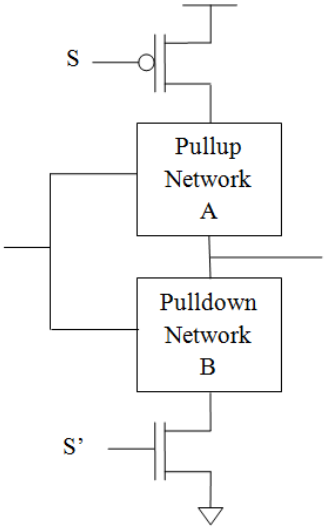

Fig 1: Sleep Transistor Technique

2.3 Zigzag Technique:

To reduce the wake-up cost of the sleep transistor technique, the zigzag technique is introduced [9]. The zigzag technique reduces the overhead by choosing a particular circuit state (e.g., corresponding to a "reset") and then, for the exact circuit state chosen, turning off the pull-down network for each gate whose output is high while conversely turning off the pull-up network for each gate whose output is low[10].

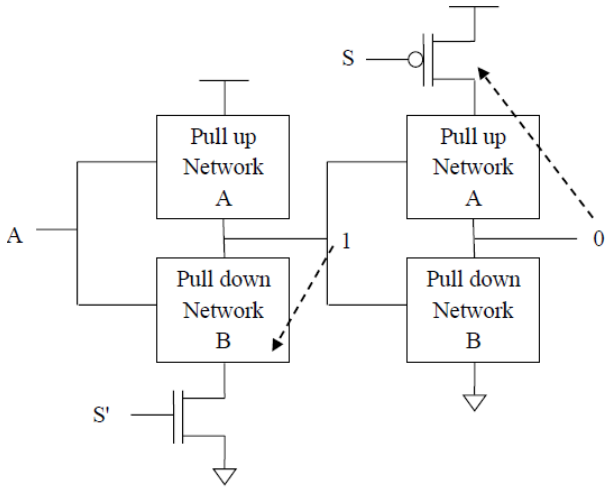

Fig 2: Zigzag Approach

For example, the zigzag technique in Fig 2 assumes that the input 'A' is asserted such that the output values result as shown in the figure. If the output is '1,' then a pull-down sleep transistor is applied; if the output is '0,' then a pull-up sleep transistor is applied. By applying particular input pattern chosen prior to chip fabrication, the zigzag technique can prevent floating. Although the zigzag technique retains the particular state chosen prior to chip fabrication, any other arbitrary state during regular operation is lost in power-down mode. Although the zigzag technique can reduce wake-up cost, the zigzag technique still loses state. Thus, any particular state which is needed upon wakeup must be regenerated somehow. The technique may need extra circuitry to generate a specific input vector (in case reset values are not used for sleep mode input vector).

III. Related Work

Modern technologies are suffering from a dramatic increase in leakage current. Constant scaling dictates that the supply voltage has to be reduced [11][12] when downsizing the technology feature size. Low threshold voltage devices are used to maintain the required current drive and to satisfy performance specifications. Low threshold devices have caused a dramatic increase in leakage current. A direct and live solution for that is to utilize low threshold devices in the critical path and high threshold devices elsewhere. The threshold voltage can be controlled utilizing the well bias of the device in the so called Variable Threshold CMOS (VTCMOS).

3.1 Proposed Technique:

In the present paper, a new leakage power technique [13] called LECTOR is used for the designing "64-bit SRAM array using LCT technique" and different experimental results are analyzed and the conclusions drawn are presented and the future scope of work on this technique is elaborated.

3.1.1 Lector Technique:

Generally lector is abbreviated as leakage control transistor, which means that a transistor can control leakage current occurred in CMOS circuits without increasing the dynamic power dissipation. In this technique we introduce two leakage control transistors between power supply and ground [14]. The gate terminal each transistor is controlled by source of other. So, one of LCT is always near to its cutoff voltage. The main principal behind the lector technique in[15],[16] "A circuit with more than one transistor is off between power supply to ground having less leaky than a circuit with only one transistor is off between power supply to ground"[17]. We illustrate our LECTOR technique with the case of a CMOS inverter. A CMOS inverter with the addition of two leakage control transistors is shown in fig.3

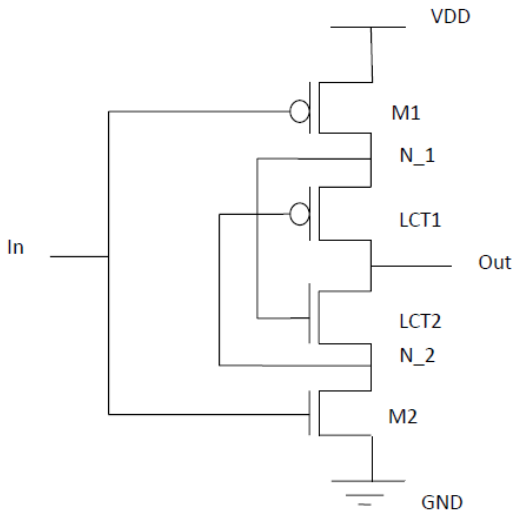

Fig3: Not gate based on LCT

TABLE 1: State matrix of NOT gate

Transistor Reference	Input '0'	Input '1'
M1	ON	OFF
M2	OFF	ON
LCT1	Near cut off	ON
LCT2	ON	Near Cut-Off

It has two leakage transistors (LCT1-PMOS) and (LCT2-NMOS) introduced between node N1 and N2. The gate terminal of one LCT is connected to the source terminal of other LCT. When the input applied is low (in=0) then transistors M2 and LCT1 are turned off, thus we get a stacking of two series connected transistors. When the input applied is high then the transistors M1and LCT2 are turned off and thus increasing the off resistance of supply voltage to ground path. So reduction in leakage power is obtained.

3.1.2 Applying Lector to 64-Bit SRAM

The conventional architecture of SRAM Cell has 6-transistors. At deep sub-micron scale the leakage power of SRAM circuit is comparatively high as compared to the other operational circuits. The concept of SRAM architecture is based on the stabilization of logic values to maintain its existence against any current or power loss with the ease of data modification using two feedbacks coupled CMOS Inverters. The output terminals of the two inverters act as internal load lines of the SRAM cell to store the memory data bit value on one of the internal load line and its complement logic value on the other internal load line.

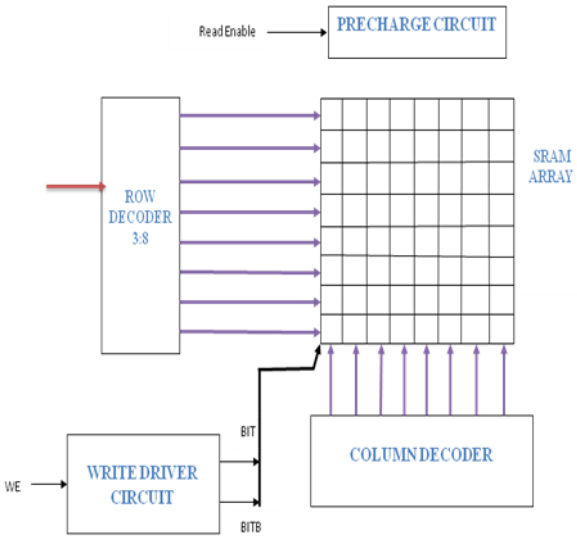

Fig 4: Block diagram of 64-bit SRAM

IV. Experimental Results

4.1 Experimental Results of Inverter:

In our present paper we started applying the LECTOR technique starting from basic CMOS circuits. Fig 5 and 6 shows the schematic diagrams of inverter in both conventional and also using the lector mechanism. The tabular form 2 shows that the power dissipation is reduced from conventional to lector technique.

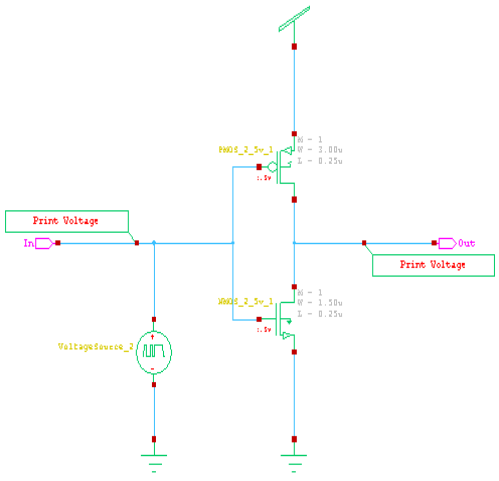

Fig 5: Schematic of conventional CMOS inverter in tanner

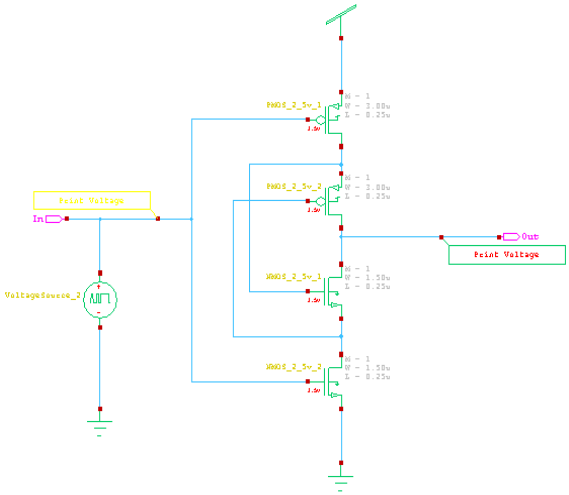

Fig 6: Schematic of CMOS inverter using lector in tanner

Table 2: Comparison of power dissipation results of CMOS inverter in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	**Lector**	
250nm	1.288508e-004	1.155602e-004	10.31%
180nm	1.2274e-005	1.094572e-005	10.8%
90nm	2.1824e-006	1.243852e-006	43%

4.2 Experimental Results of Nand:

Figures 8 and 9 shows the schematic diagrams of NAND gate in both conventional and lector technique. The tabular form 3 shows that the power dissipation is reduced from conventional to lector technique.

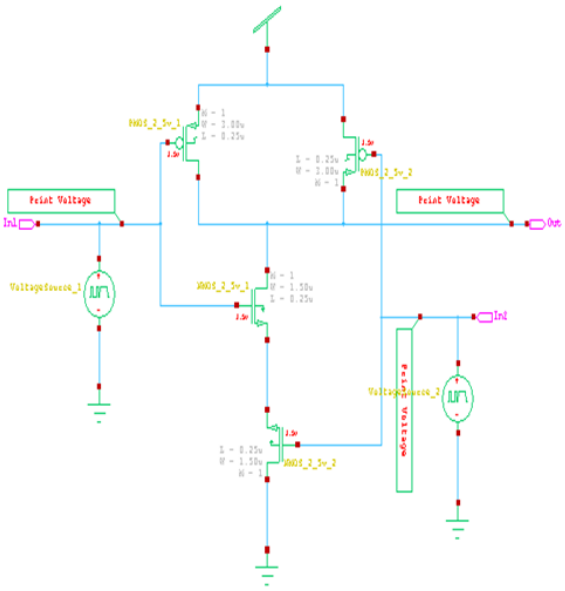

Fig 8: Schematic of conventional CMOS NAND gate in tanner

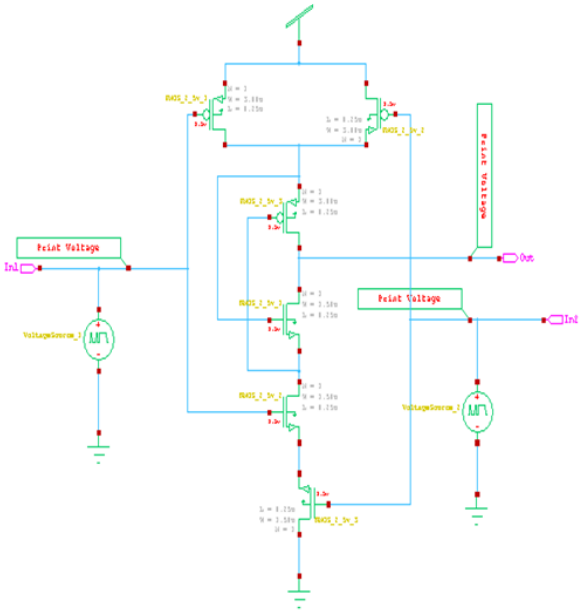

Fig 9: Schematic of CMOS NAND gate using lector in tanner

Table 3: Comparison of power dissipation results of CMOS NAND gate in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	**Lector**	
250nm	1.403209e-004	1.015146-004	27.6%
180nm	1.7643e-005	1.507218-005	14.5%
90nm	3.6431e-006	1.736292-006	52.3%

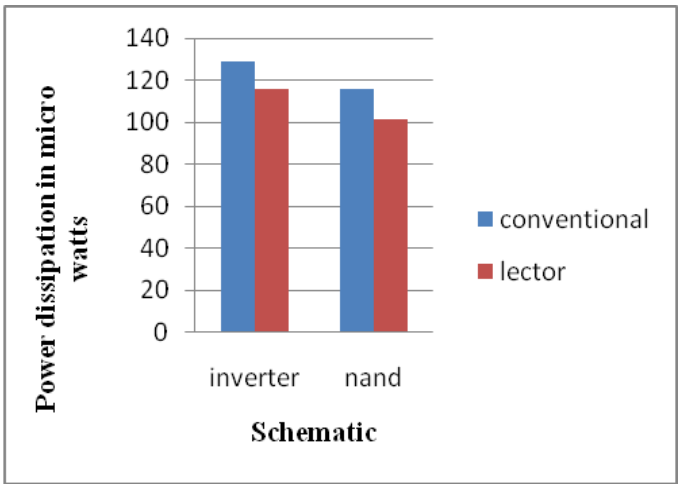

Fig 11: Bar Graph showing reduction in power dissipation in inverter and NAND

4.3 Experimental Results of Decoder:

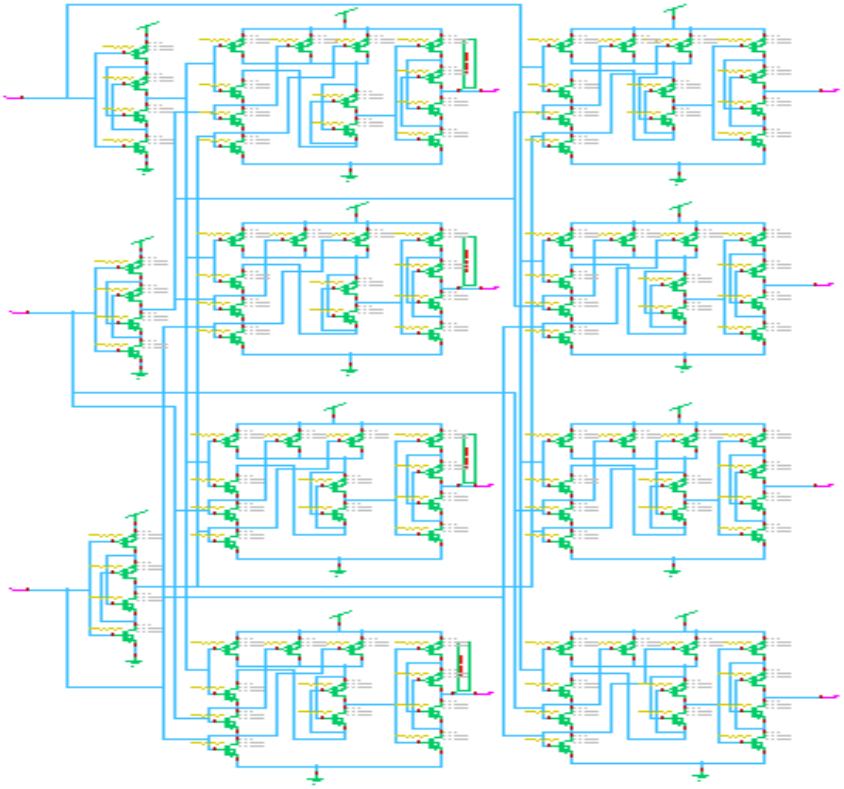

Fig 12: Schematic of conventional 3:8 decoder

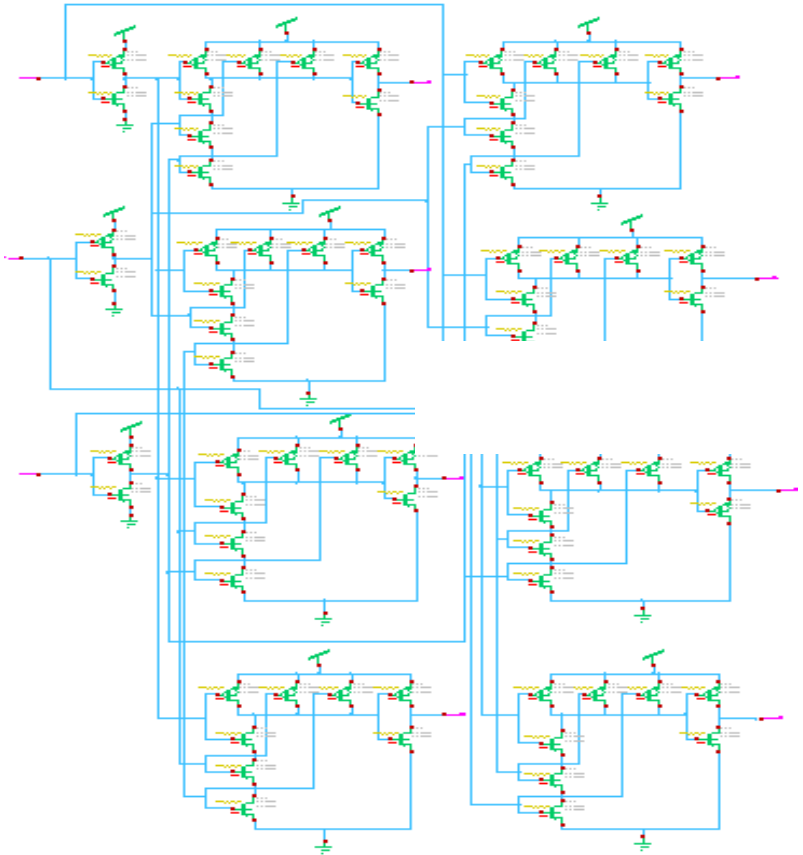

Fig 13:3:8 decoder using lector

Table 4: Comparison of power dissipation results of 3:8 decoder in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	Lector	
250nm	1.738197e-003	1.184681e-003	31%
180nm	9.564609e-005	4.939357e-005	48.3%
90nm	1.565999e-006	8.546299e-007	45%

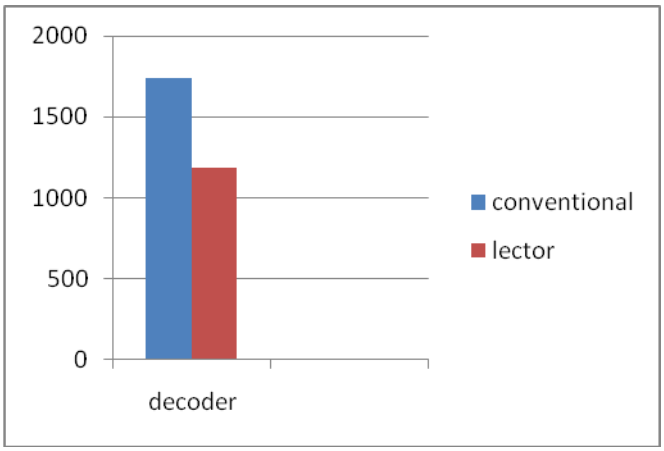

Fig 15: Bar Graph showing reduction in power dissipation in 3:8 decoder

4.4 Experimental Results of 1-Bit 6T SRAM Cell:

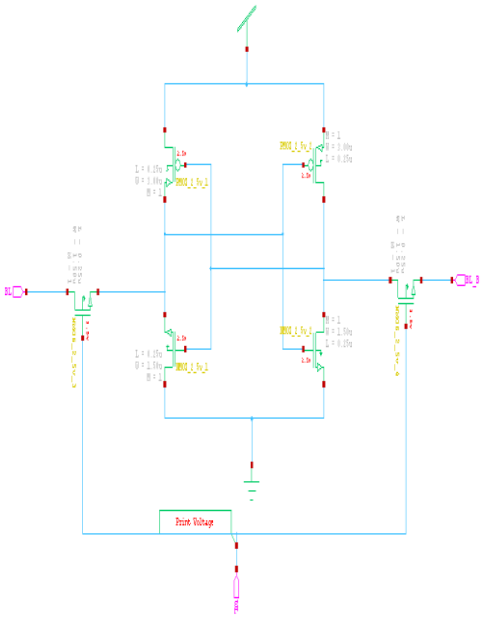

Fig 16: Schematic of conventional 1-bit 6T SRAM cell in tanner

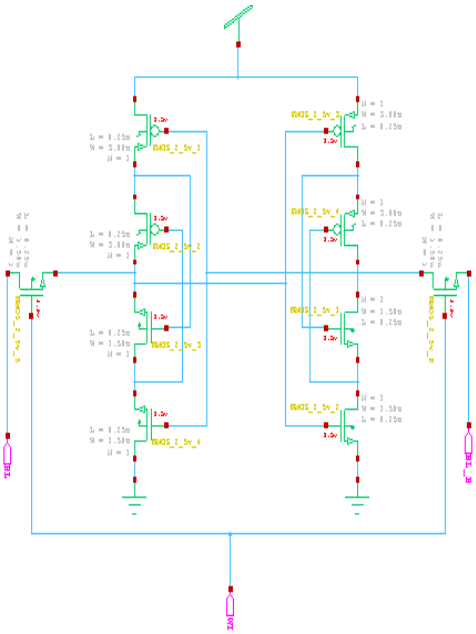

Fig 17: Schematic of 1-bit 6T SRAM cell using lector in tanner

Table 5: Comparison of power dissipation results of 1-bit 6T SRAM cell in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	Lector	
250nm	7.507245E-003	6.355988E-003	15.33%
180nm	1.702321E-004	1.40610E-004	17.4%
90nm	1.333432E-004	9.70455E-005	27.2%

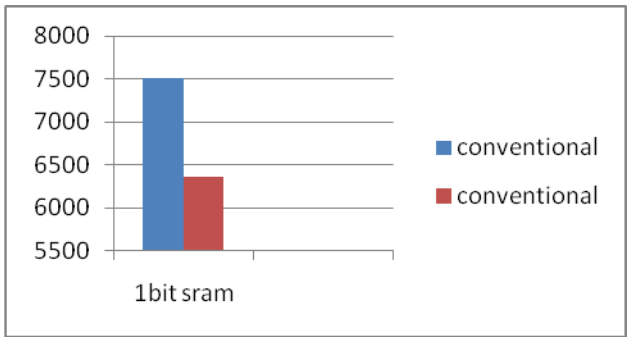

Fig 19: Bar Graph showing reduction in power dissipation on 1-bit SRAM

4.5 Experimental Results of Write Driver Circuit:

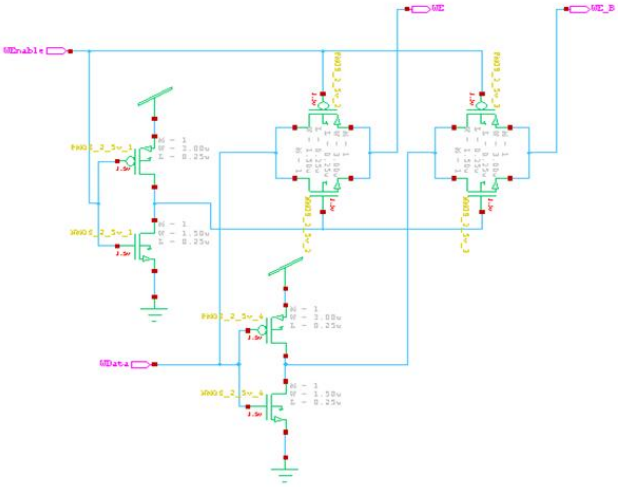

Fig 20: Schematic of conventional write driver circuit tanner

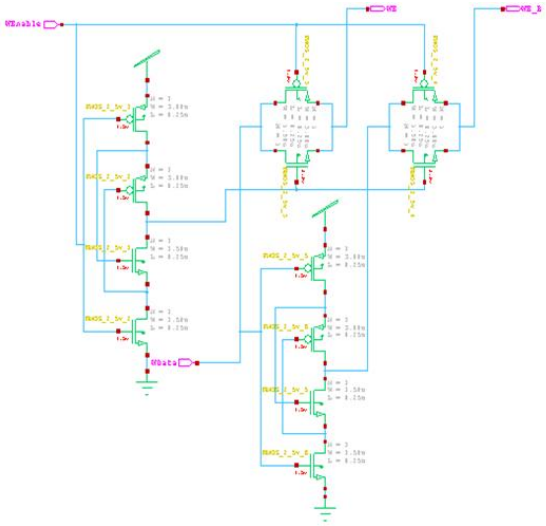

Fig 21: Schematic of write driver circuit using lector in tanner

Table 6: Comparison of power dissipation results write driver circuit in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	**Lector**	
250nm	4.517460e-005	4.156591e-005	7.9%
180nm	1.549203 e-006	7.964656e-007	48.5%
90nm	7.520833e-007	3.976489e-007	47%

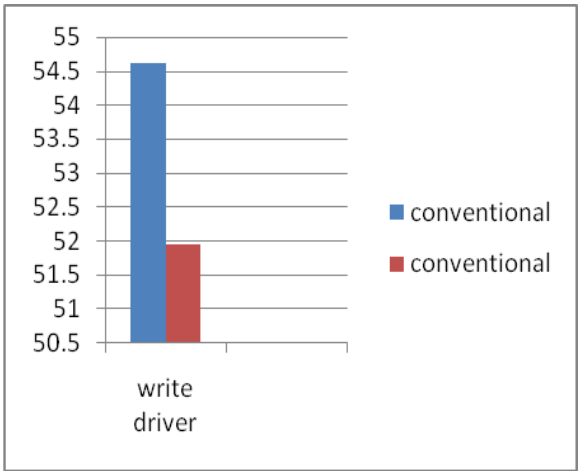

Fig 23: Bar Graph showing reduction in power dissipation in write driver circuit

4.6 Experimental Results of 64-Bit SRAM Array:

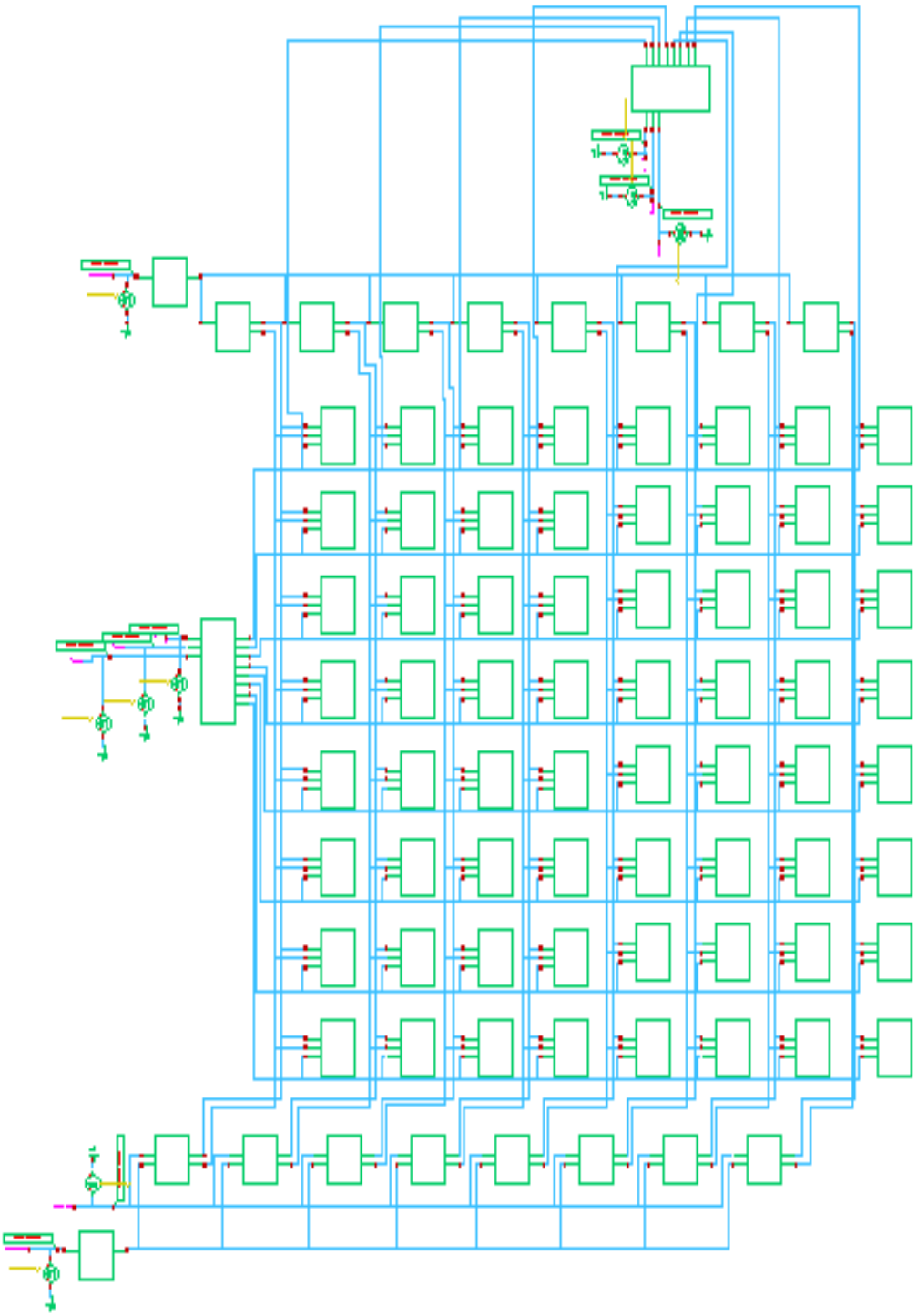

Fig 25: Schematic of 64-bit SRAM array in tanner

Table 7: Comparison of power dissipation results 64-bit SRAM in conventional and lector technique

Technology Process	Average Power Consumption (in micro watts)		% decrease in the power consumption
	Conventional	Lector	
250nm	1.285813e-001	1.154642e-001	10.2%
180nm	2.220370e-003	1.966213e-003	11.4%
90nm	5.789263e-004	3.267453e-004	43.5%

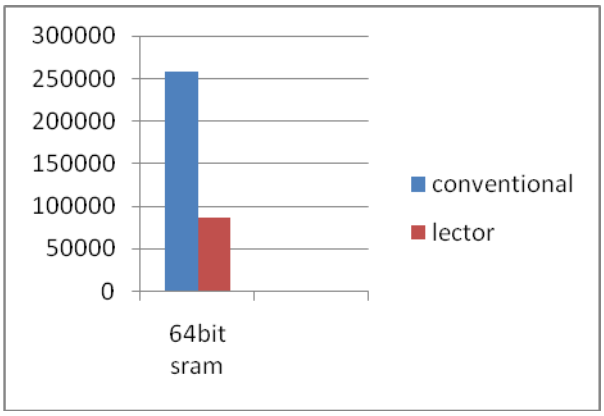

Fig 26: Bar Graph showing reduction in power dissipation in 64-bit SRAM

V. Conclusion

The scaling down of device dimensions, supply voltage, and threshold voltage has largely contributed to the increase in leakage power dissipation. With deep-submicron and nanoscale technologies, the leakage current becomes more critical in portable systems where battery life is of primary concern. LECTOR yields better leakage reduction as the threshold voltage decreases and hence aids in further reduction of supply voltage and minimization of transistor sizes.

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