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# Design and Comparison of 8x8 Wallace Tree Multiplier using CMOS and GDI Technology

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***Abstract:*** *Multiplier is an important building block in the design of digital circuits. Multiplier is widely used in Digital signal processing and in communication applications. Compact and small circuit with low power dissipation and very small delay are main desire of circuit designer in the field of VLSI design. A Wallace tree multiplier is an example of improved version of tree base multiplier. Many algorithms have been introduced in the search of the fastest multiplier. There are different types of multiplier based on the algorithm and Wallace tree multiplier is one of them. It uses carry save addition algorithm. The result shows that the GDI based Wallace tree multiplier is performing best as compare to CMOS based multiplier. Power dissipation and delay of GDI and CMOS based Wallace tree multiplier at 1.8 V power supply is 8.8mW and 9.6mW and 0.02nS & 0.17nS respectively.*

***Keyword:*** *Multiplier, VLSI Design, Wallace Tree Multiplier, GDI, CMOS.*

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## I. Introduction

Performance of the circuit depends on the performance of the small parts of the circuit. So it is a very difficult and challenging task the designer to design high performance circuit. There are many different parameters that are considered in the performance of the circuit like area, power dissipation, propagation delay etc. Compact area, low power dissipation and high speed are main concern of any circuit designer. A multiplier consist three stages first is generation of partial products then addition of these partial product and then final stage of addition. This paper aim at reduction of power consumption and latency of 8x8 Wallace tree multiplier. This is accomplished by the use of small circuits like half adder, Full adder, 4:2 compressor, 5:2 compressor. Basically two unsigned integers are multiplied by Wallace tree multiplier. A Wallace tree multiplier uses an AND array for computing partial products and carry save adder for adding these partial products and carry propagate adder in the final stage.

## II. Basic Multiplication Process

In the multiplication of two binary digits, first digit is called multiplicand and the second one is multiplier. The multiplication process consist partial product of multiplicand and multiplier in first step. In the partial product row if the multiplier bit is "0" then the multiplication result will be zero and if the multiplier bit is "1" then the multiplication result will be same as multiplicand. After generation of partial product next step of multiplication is addition [1]. Block diagram of M-Bit Multiplicand and N-Bit Multiplier is shown in figure 1.

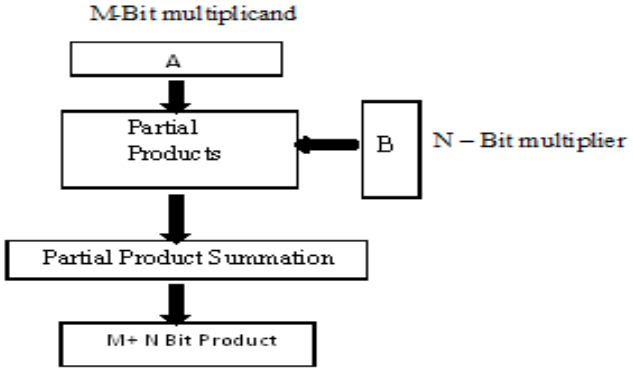


**Figure 1**: Multiplier Block Diagram

An example of 4-Bit multiplicand and 4-Bit multiplier product of two positive (unsigned) binary numbers radix 2 is given below:

```
        1010          (This binary number represents 10 in decimal)
    x   1001          (This binary number represents 9 in decimal)
------------------
      I 0 1 0         (1010 x 1)
    0 0 0 0 x         (1010 x 0, shifted one position to left)
  0 0 0 0 x x         (1010 x 0, shifted two position to left)
+1 0 1 0 x x x        (1010 x 1, shifted three position to left)
------------------
 1 0 1 1 0 1 0        (This binary number represents 90 in decimal)
```

## III. TYPES OF MULTIPLIER

Based on different algorithm there are different types of multipliers, in different algorithm there are different methods to produce partial product generation and partial product addition. The motives of all circuit designers to design the multiplier which provide high speed, regularity of layout, compact area, reduce latency. Many algorithms have been introduced in search of the fastest multiplier. Based on different algorithm there are different types of multipliers:

- Array multiplier
- Wallace tree multiplier
- Dadda Multiplier
- Modified Both Multiplier
- Hierarchical Array of Array Multiplier
- Vedic Multiplier

### 3.1 Wallace Tree Multiplier

The speed of multiplier is depends on the total time taken for summation of partial products. Wallace tree multiplier is faster than Array multiplier. Scientist Chris Wallace in 1964 introduced an easy and simple way of summing the partial product bits in the parallel using the tree of the Carry Save Adders which is known as "Wallace Tree" [2]. Wallace tree multiplier uses carry save addition algorithm. A typical Wallace tree architecture is shown in figure 2.

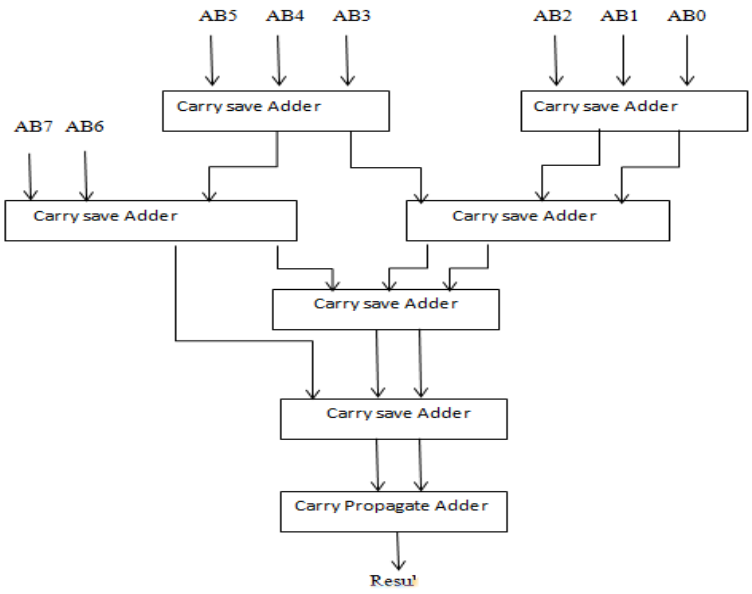


**Figure 2** : Wallace Tree Multiplier

Wallace multiplier includes some steps to multiply two numbers .The first step is formation of the bit products. Then carry save adder reduces bit product matrix into two row matrix. After that the remaining two rows are summed by using the fast carry propagate adder to produce the final result [3]. Some advantages and disadvantages of Wallace tree multiplier are given below:

Advantages

- Small Delay
- The number of logic levels required to perform the summation can be reduced.

Disadvantages

- Complex to layout and have irregular wires.

3.1.1 2-Bit Multiplier

In 2 -Bit Multiplier, the multiplicand has 2 bits and multiplier has also 2 bits. The result of multiplication is of 4 bits. A 2-Bit multiplier circuit consist AND array and half adder. Hardware realization of 2- Bit multiplier is shown in figure 3.

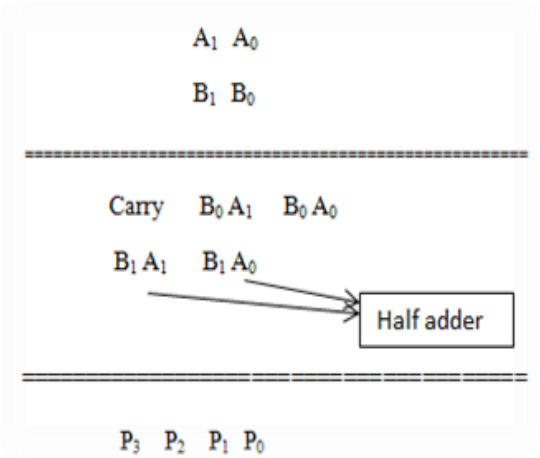


**Figure 3:** 2- Bit Multiplier

Schematic diagram of 2-bit multiplier is shown in figure using Wallace tree method shown above. P0, P1, P3 and P4 are the partial products.

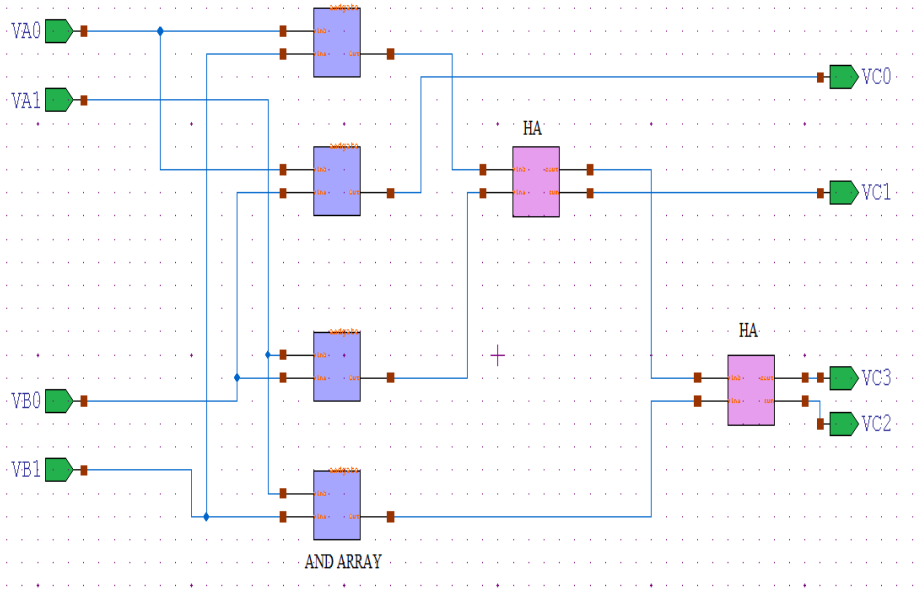


**Figure 4**: Schematic diagram of 2-bit multiplier

**3.1.2 4-Bit Multiplier**

After designing of 2- Bit multiplier, 4 bit multiplier also designed. In 4 -Bit Multiplier, the multiplicand has 4 bits and multiplier also has 4 bits. A 4-Bit multiplier circuit consist AND array and half adder and Full adder [4]. 4-bit multiplier is also designed using wallace tree method as shown in figure 5.

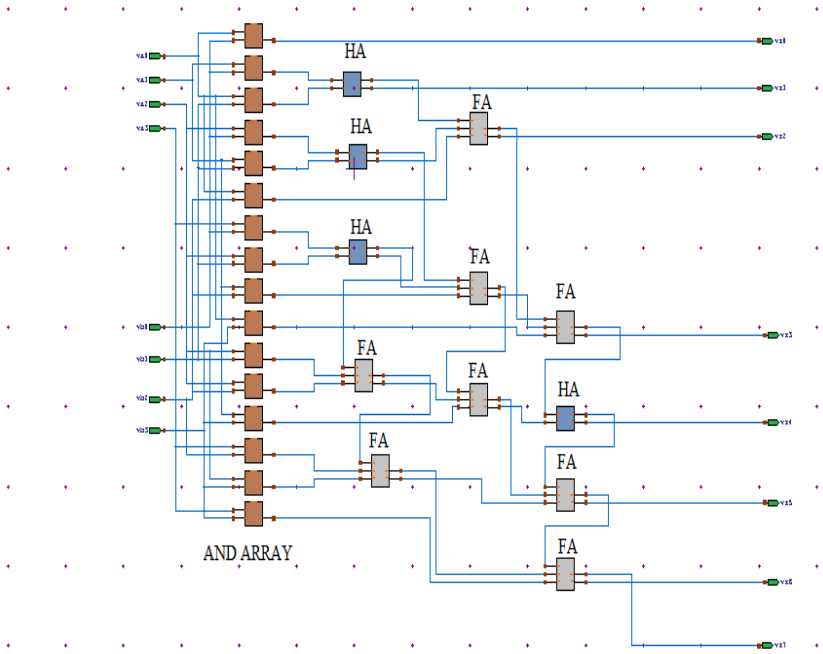


**Figure 5:** 4-Bit Multiplier

### 3.1.3 8-Bit Multiplier

8-Bit Multiplier based on Wallace Tree is more efficient in terms of power and regularity with low latency and area. Wallace method used three steps to multiply two numbers. These steps are given below:

- Formation of the bit products.
- Bit product matrix is "reduced" into two row matrix by using the carry-save adder (also called 3:2 counters).

The remaining two rows are summed by using the fast carry-propagate adder to produce the final product.

8x8 Bit multiplier using Wallace tree circuit consist AND array And also consist Half adder, Full Adder, 4:2 Compressor, 5:2 Compressor. AND gates are used for the generation of partial products in the parallel. Furthermore, the addition of the partial products is done using the Wallace tree, which is hierarchal, divided into levels [5]. There will be a reduction in power consumption, since the power is provided only to level that is involved in the computation. Schematic diagram of GDI based 8 x 8 multiplier is shown in figure 6.

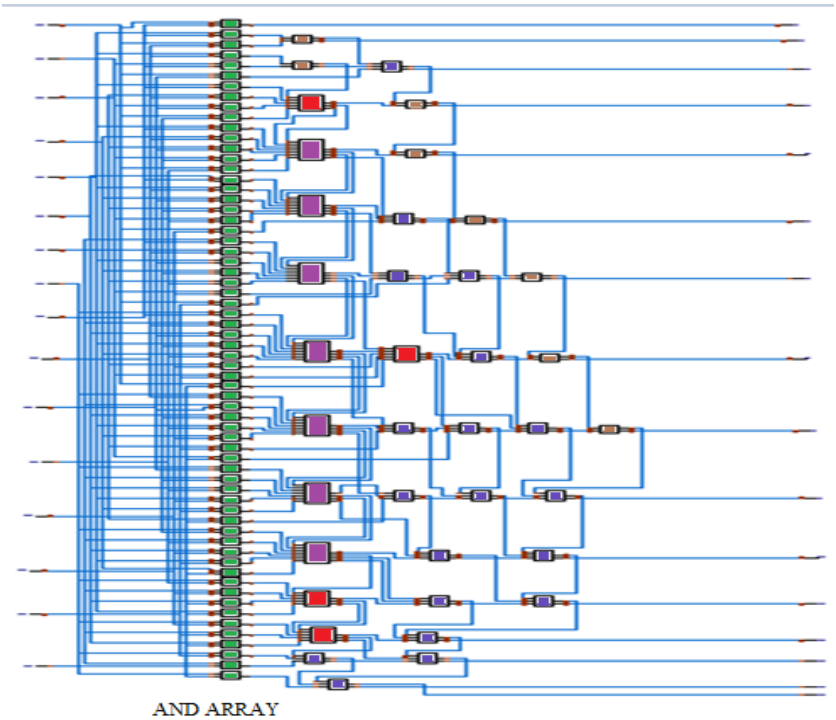


**Figure 6**: GDI based 8-Bit Multiplier Schematic

## IV. Simulation And Results

### 4.1 2-Bit Multiplier

Simulated waveform of 2-bit GDI based multiplier is shown in fig 7.

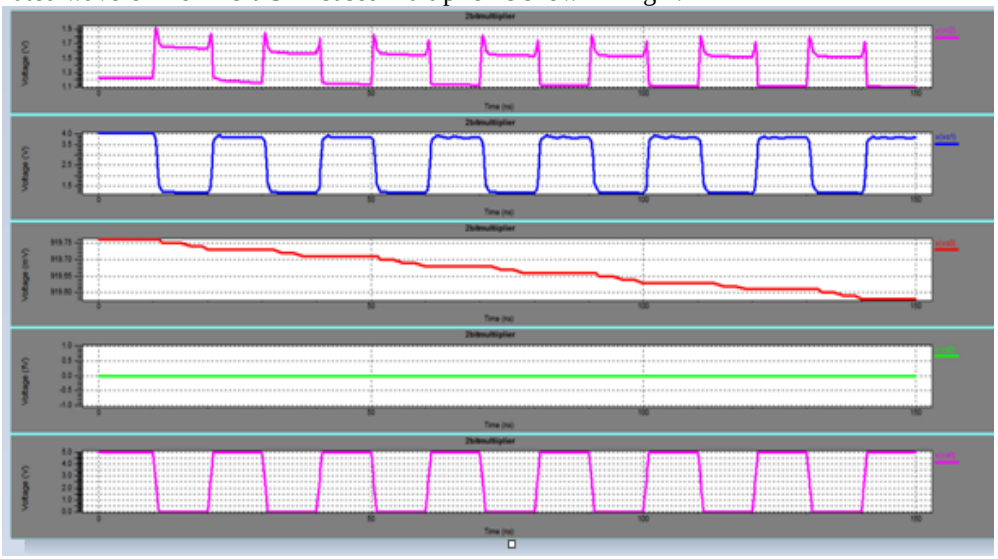

**Figure 7:** Waveform of 2-bit GDI based Multiplier

### 4.2 4-Bit multiplier

Simulated waveform of 4-bit GDI based multiplier is shown in fig 8. Multiplier and multiplicand inputs each are of 4 bits. After multiplication 8-bit partial products are generated. Here both CMOS and GDI based 4x4 multiplier are designed and analyzed. GDI based multiplier gives better results in terms of propagation delay, power dissipation and area by using transistor count.

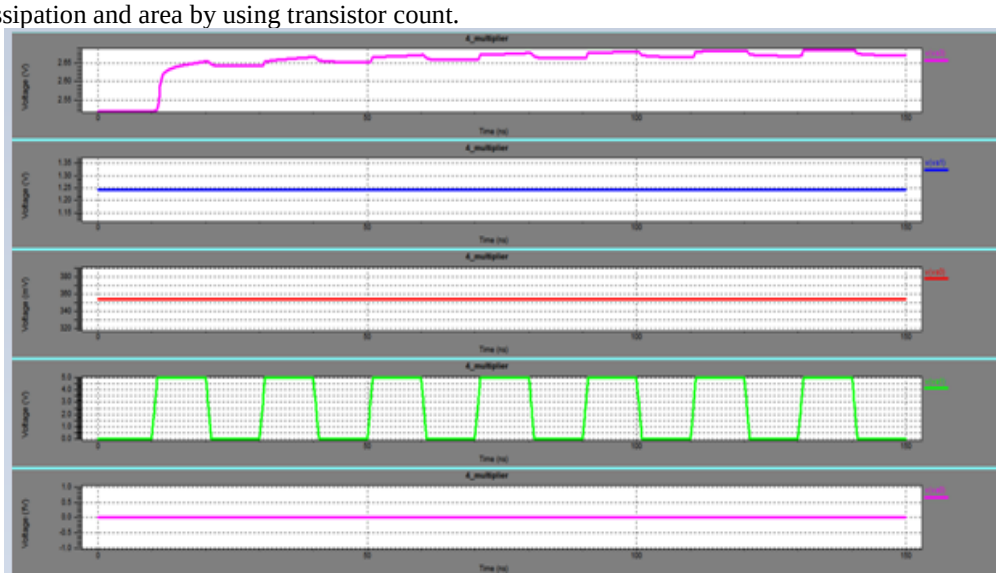

**Figure 8:** Waveform of 4- Bit GDI based Multiplier

**4.3 8-Bit Multiplier**

Simulated waveform of 8-bit GDI based multiplier is shown in fig 9. Multiplier and multiplicand inputs each are of 8 bits. After multiplication 16-bit partial products are generated.

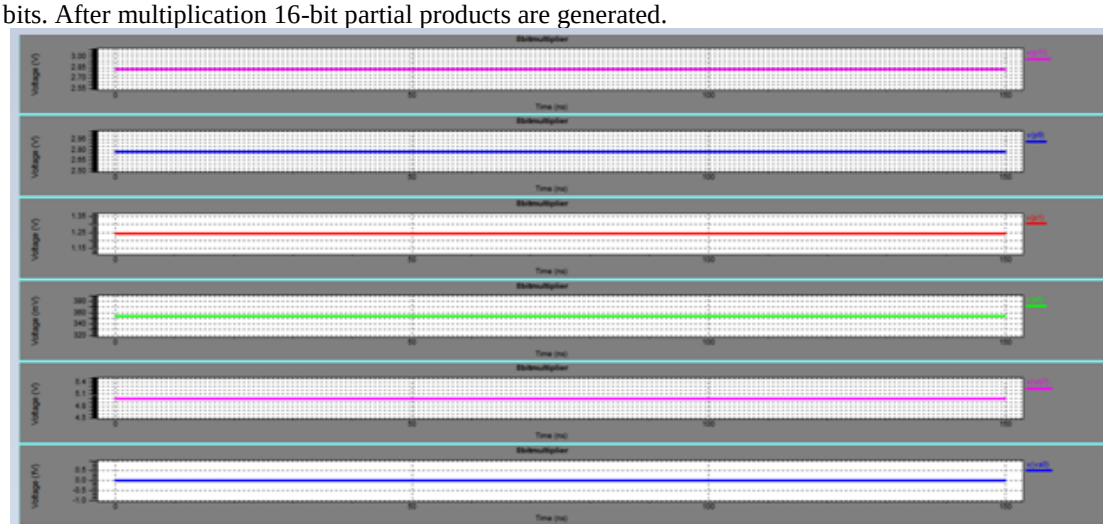

**Figure 9:** Waveform of 8- Bit GDI based Multiplier

Propagation delay and power dissipation of both 8-bit CMOS multiplier and 8-bit GDI multiplier is listed below in table 1 and table 2 respectively.

**Table1.** Parameter Of 8-Bit Gdi Multiplier

| Vdd (V) | Delay (ns) | Power Dissipation (mW) |
|---|---|---|
| 1.8 | 0.02 | 8.854 |
| 1.6 | 0.40 | 8.395 |
| 1.4 | 0.65 | 7.975 |
| 1.2 | 0.72 | 7.414 |
| 1.0 | 0.82 | 6.756 |

**Table2**. Parameter Of 8-Bit Cmos Multiplier

| Vdd (V) | Delay (ns) | Power Dissipation (mW) |
|---|---|---|
| 1.8 | 0.17 | 9.64 |
| 1.6 | 0.56 | 9.19 |
| 1.4 | 0.70 | 8.57 |
| 1.2 | 0.80 | 7.84 |
| 1.0 | 0.95 | 6.95 |

## V. Conclusion

The GDI based Wallace tree multiplier occupies smaller area compare to conventional Wallace Tree Multiplier. CMOS based multiplier use 1488 transistors in the designing of 8-Bit Wallace tree multiplier while GDI based multiplier use 912 transistors in the designing of 8-Bit Wallace tree multiplier. Power dissipation and delay of GDI and CMOS based Wallace tree multiplier at 1.8 V power supply is 8.8 mW & 9.6 mW and 0.02nS and 0.17 nS respectively. Thus the result shows that the GDI based Wallace tree multiplier is performing best as compare to CMOS based multiplier.

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