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Dual-threshold Single-ended Schmitt-Trigger Based Radiation Hardened memory Design with Fault modeling System

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Abstract: *Up to 70% of Systems on a Chip (SoC) area are occupied by embedded memories. Efficient SoC is developed by making memory efficient in terms of power consumption, de-sensitized to environmental changes, Speed and Fault free. Ultra low Power module can be developed by scaling Supply Voltage which leads to loss of stability because of reduced SNM and Switching Threshold levels and this problem can be rectified by introducing Single ended and Schmitt trigger topology to memory cell, which exhibits high read and hold SNM and consumes low power during the hold operation. Desensitized Memory architecture is developed by introducing two extra switches in Feedback path to isolate regenerative feedback of radiation hardened memory in hold mode. So when a radiation strike causes a value change on any node of the bit cell, the other four internal nodes are designed, so that the state change at this node cannot flip the cell and the disruption is suppressed within a deterministic recovery time. Weak cell fault model is proposed to identify week cells in the memory which are formed because of poorly formed contacts and vias during fabrication process. This results in the shift of the Meta-stability point of the cell, Data Retention Fault or Open-Resistive Fault and also causes read destructive fault and Leads to faulty swap of cell data. SRAM Cell Stability Model is proposed by negative feedback resistor model SRAM Cell which has adjustable SNM to compare weak Cells in the memory system. Build in Current Sensor (BICS) is designed to identify soft errors and single event upsets due to radiation effects. Memory is implemented in 45 nm CMOS technology at supply voltage of 400 mV near to sub-threshold Voltage levels.*

Index Terms: *BICS, Weak cell fault model, data retention fault.*

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I. Introduction

Memory Cell with write assist circuit and read sense amplifier pre-charge circuit and isolate circuit all these together like a memory architecture can be used for normal high speed embedded applications. But coming to high end applications like aerospace and military this memory architecture is not suitable. So Memory architecture should be modified according to environmental conditions and resources availability in those applications.

A. Write assist circuits with memory architecture:

6-T, 8-T SRAM memory models are proposed and sizing is also done according to circuit parameters like write margin, read margin, pull up ratio, cell ratio, Data retention voltage and SNM. In this 8-T Cell model two extra transistors to avoid read failure.

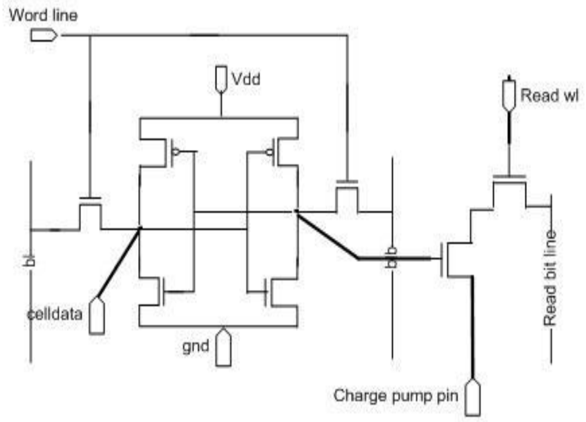

Fig.1 8-T SRAM Memory Cell

Write circuit is also designed to load differential data into memory when a particular control enable is activated. Write driver circuit with control and data input is represented in following diagram.

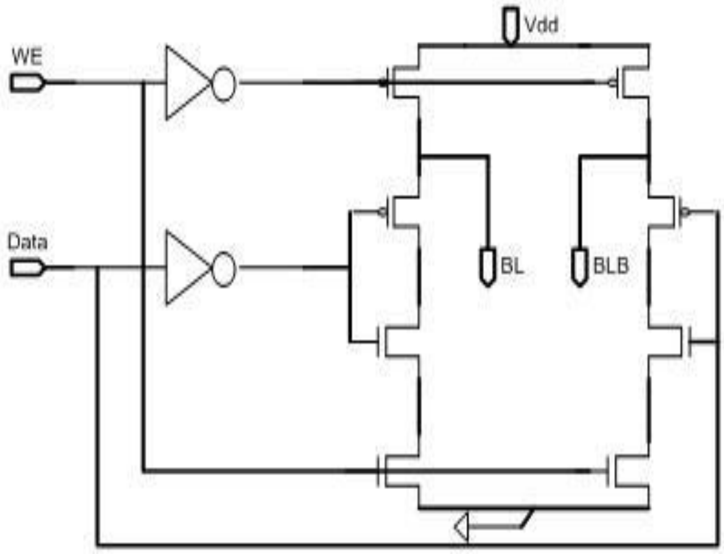

Fig.2 Write driver circuit

So as to have better performance in terms of accessing by improving Write Margin (WM) and this one is possible by using following Assist Schemes

a. Capacitive charge sharing scheme
b. Transient Negative bit line scheme
c. NBL at write circuit.
a. Capacitive Charge sharing Scheme:

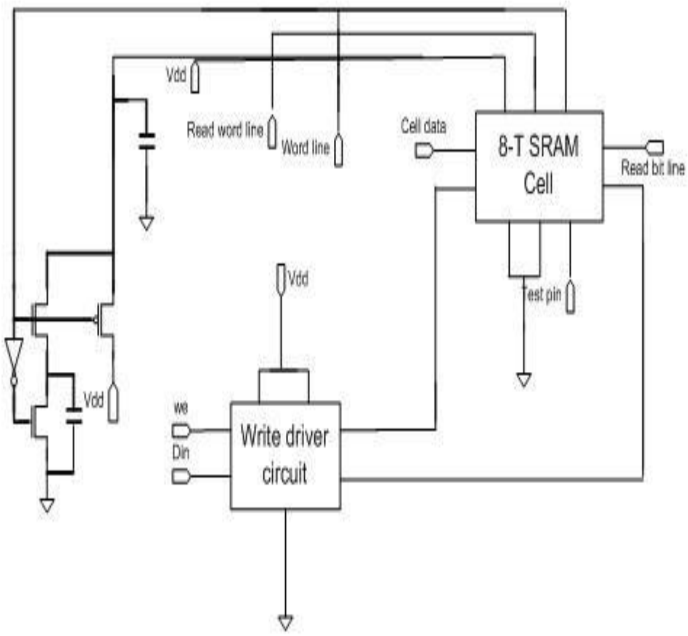

Fig.3 charge sharing circuit to 8T Memory cell

Supply voltage of cell can be adjusted based on mode of operation. This is the scheme also provides a solution to reduce power dissipation means ultra-low power memory applications can be developed.

b. Transient Negative bit line scheme:

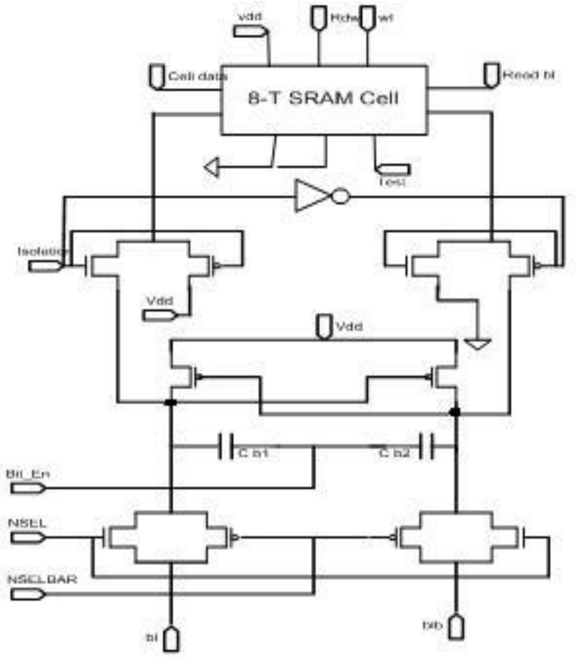

Fig 4: Transient Negative Bit Line circuit

By making bit lines negative accessing speed is improved. Here NBEL and BIT_En are control signal to switch on or off particular transistors by which isolation can be provided from write driver circuit.

c. NBL at write driver circuit

In this scheme instead of making bit line negative logic bit strength is reduced at write driver circuit. With compared to previous NBL scheme this assist scheme has more Write Margin.

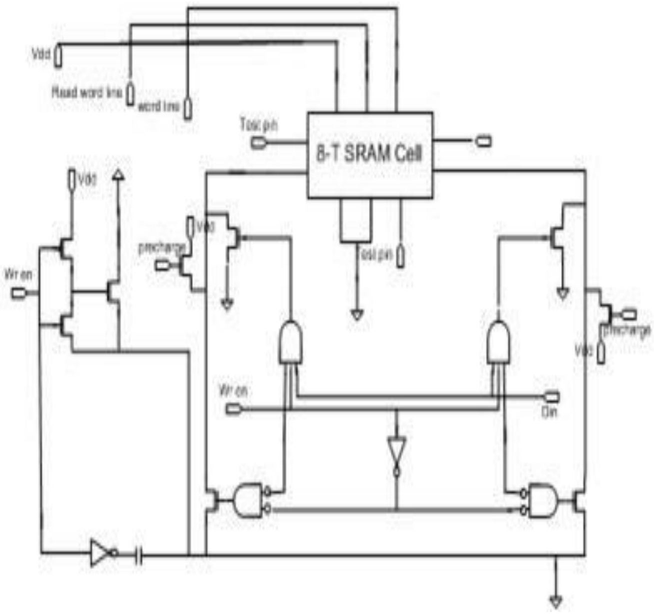

Fig.5 NBL at write driver circuit

In this same way read assist circuits and sense amplifiers are used to read data from memory.

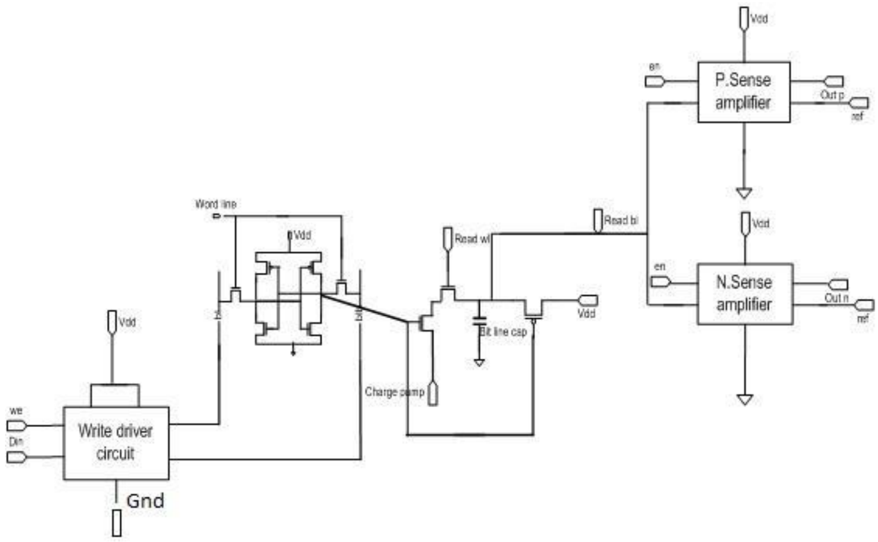

Fig.6 Read data from memory cell through sense amplifiers

II. Modified memory architecture

Memory architecture is modified according to environmental parameters like radiation effects and resources availability in aerospace applications. In high end applications memory architecture should be having following characteristics

A. Radiation Hardened memory architecture:

Dual driven multiple feedback mechanism is added in memory architecture as shown below. Here in each memory cell memory node is driven by four other nodes so because of radiation one node if it is effected even other nodes protects the memory.

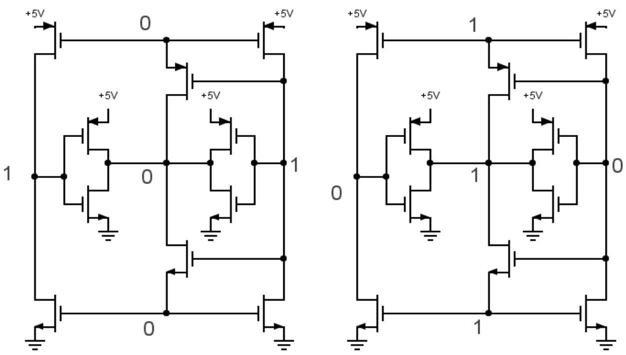

Fig 7: Dual driven multiple Feedback Memory Architecture

B. Ultra low power memory architecture

Power dissipation can be minimized by scale down supply voltage but problem is SNM is also scaled so stability of cell is reduced. So SNM is improved by introducing Schmitt trigger Topology to memory. Here Schmitt trigger based inverter and conventional inverter is compared using transfer characteristics and observed for ST based inverter is having more SNM.

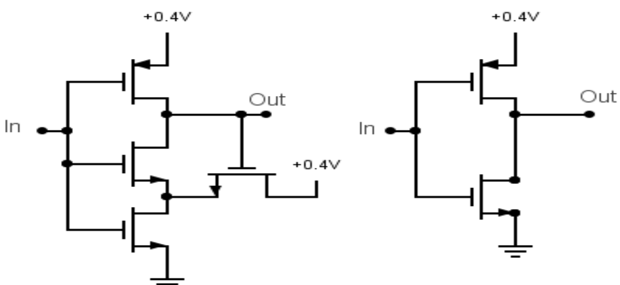

Fig 8: ST Based inverter and Conventional CMOS inverter

Using this Schmitt trigger switching threshold of inverter can be separated into two levels so as to improve SNM because these memory circuits are operated at near to sub-threshold region so switching at two levels definitely improves SNM.

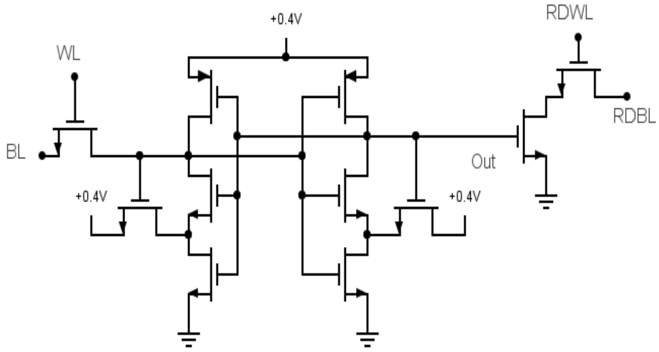

Fig 9: Schmitt Trigger Based 11-T SRAM Memory Cell

III. DFT Techniques for Soft Errors

A. Build in Current Sensor as a DFT Module

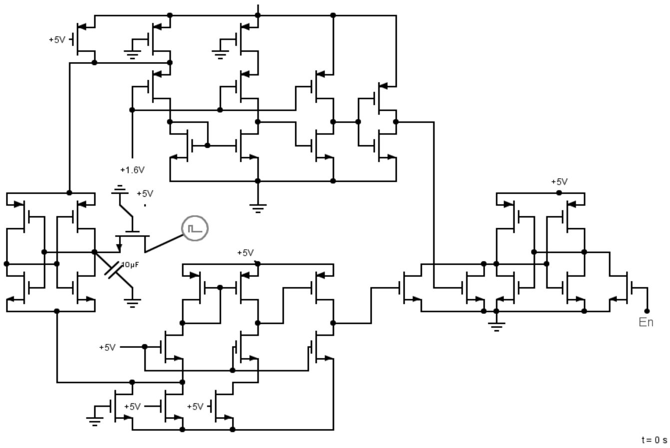

Fig 10: Build in Current Sensor for soft error identification

Embedded memories in aerospace applications should be desensitized to radiation effects. If there any single event upsets occurs those should be recognized by BICS kept along with the memory architecture.

B. Weak Cell Fault Model

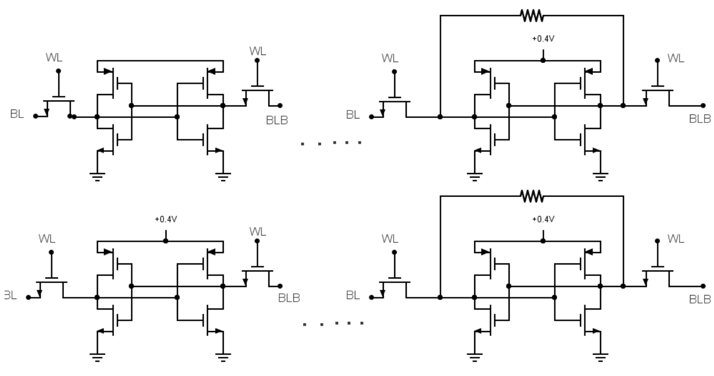

Fig 11: Weak Cell fault model with negative resistor model

Degree of weakness can be controlled by negative feedback resistor in memory cell. Here weak cell fault model is proposed to identify which another memory cell having same strength compared to proposed one.

IV. Results

Table I Calculation Of Power Required In Different Operations

Condition	power (f W)
Write Logic-1	132.2
Write Logic-0	102.3
Read Logic-1	32.3
Read Logic-0	22.9

Table II Calculation of Write Margin

Name of the write assist scheme	Write trip voltage	write trip current
Capacitive W-AC	0.59 V	5.8μ A
Transient-NBL	0.52V	9.1μ A

Analysis 8-T cell:

The Delay and leakage currents for 8-T SRAM cell are calculated below when the Cell is sized according to better write and read margins.

Delay calculations:
Writing into bit-line = 32.02 pS.
Writing into bit-line-bar = 25.4 pS.
Calculation of currents:
I read= 40.2 µA
I leakage= 47.4 pA.
Leakage power of the cell= I leakage x supply voltage =1.62 µW.

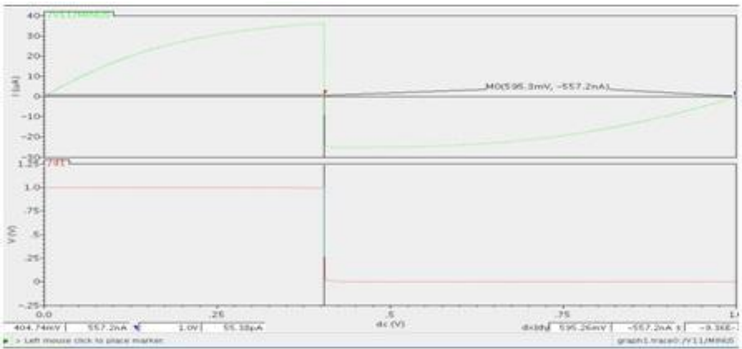

Fig 12: Capacitive W-AC writes circuitry DC-analysis to Calculate WM

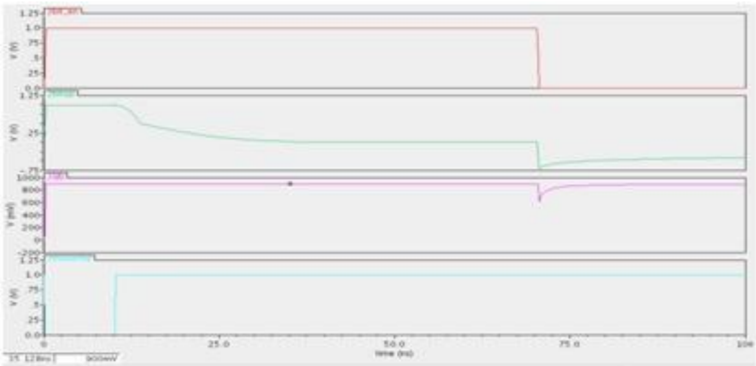

Fig 13: Output waveform for latching fail operation

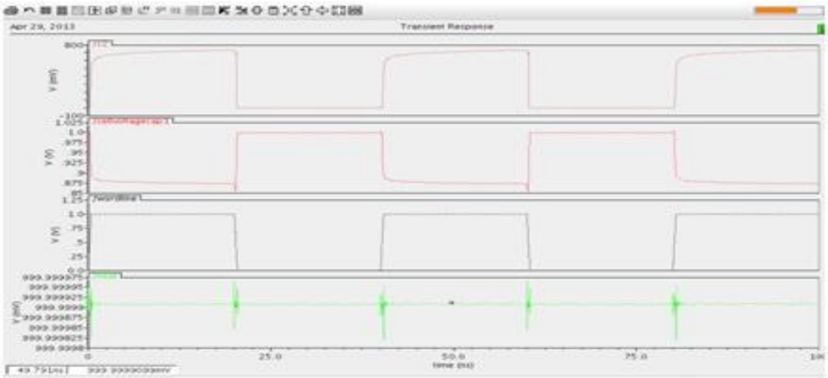

Fig 14: Waveform for correct latching operation

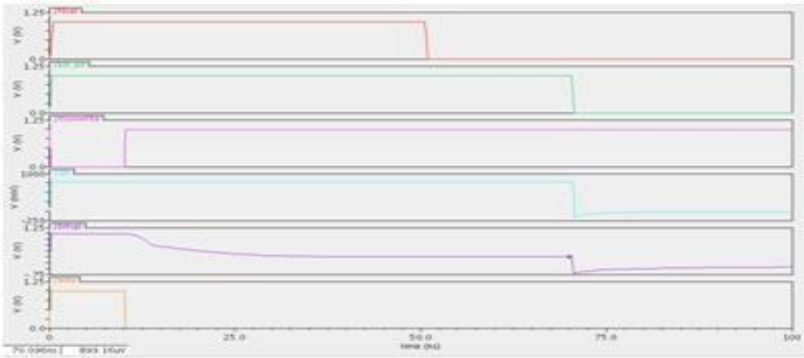

Fig 15: NBL write operation waveforms

V. Conclusion

Design synchronous memory means all read and write operations sync with clock so that few options are available to burst accessing memory (at a time more number of cells) and pipeline accessing (instead of one by one along with another) memory so as to increase system speed with compared to latency of the system.

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