IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 7, Issue 4, Ver. II (Jul. - Aug. 2017), PP 48-55
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

An Improvised Bottleneck Routing Algorithm for virtual Buffer based energy efficient NoC's

B.Nageshwar Rao[1] and N.S.Murti Sarma[2]
[1](*Research Scholar, department of ECE, Rayalaseema University, Kurnool, Andhra Pradesh, India)*
[2](*Professor Sreenidhi Institute of Science and Technology, Yamnampet, Ghatakesar, Hyderabad, India)*

Abstract: *Network on chip technology will be a major factor in future communication system which is based on intra core system, But when comes to power usage this practical NoC system consumes considerably huge power , then the Architecture of the crossbar routers will directly increases with respect to the no of intra core system . When comes to bulky systems, the average power consumption in crossbar switches relatively high. While detailing the components of the routers we found that buffers in the input terminals leads to major power consumption, when we try to remove buffers in NoC routers, the overall performance will reduce due to the bottleneck Increase. To make These Network on Chip crossbars efficiently without degradation in performance we propose a better systematic approach in the crossbar switches by incorporating virtual Memory system as a substitute of conventional register based memory, this will leads to energy efficiency with increase in overall performance. We are going to apply this architecture in NoC system which based on 5 Intra core system, our proposed system reduced nearly 30% of overall power usage.*

Keywords: *Low Power, Network on Chip, Bufferless, Bottleneck Algori*

I. Introduction

The Multiprocessors systems and the communication blocks in the integrated chips are constantly growing, so that the reliable communication protocol needed for the efficient communications between the integrated chips. In modern integrated chips design scenarios the design methodologies focusing on the communication centric approach rather than the computation centric. Traditional communication connections are replaced by the bus based communication topology due to its higher efficiency in bandwidth, scaling, and multi-processing communications. The Network on Chip architecture largely used by the multiprocessor system called as Multiprocessor System on Chip (MPSoc).

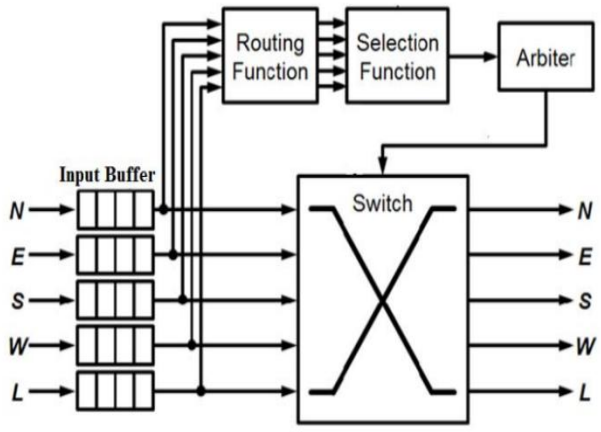


Figure (1) Base Architecture of Network on Chip system.

NoC systems majorly depends on the packet switching for enhancing its communication amount the intra chip cores. The designing process of NoC chip was more important due to its power and area profiles. NoC crossbar consumes nearly 30 % of total chip power for its interconnections between all intra chips. Memory circuits that's input buffers acts major role in NoC power Profile. Nearly 72% of leakage power caused by these type of buffers only, These characteristics of buffers leads to significant loss in energy efficiency of NoC System. The power consumption chart of these buffers directionally proportional with the data flow rate.

Network on Chip was a communication platform that was mostly uses by the modern communication processors. Network on Chip mostly depends on the application and the architecture oriented. The NoC consists

of the Arbiter and the Particular routing algorithm for switching the multiple data's between input and the output ports. The routing algorithm depends on the arrangement of the input and the output ports. Routing algorithm consists of the flow control used to control the packet flow between the input and output ports. Overall packet flow depends on the overall packet size and the availability of the slotted output.it details the how to switch the packet from the input to the output ports. And the router gives priority when the multiple packets from the multiple inputs arrive for the same output. In system on chip the single input connected with the thousand SoC output cores. However when the number of input cores increases the number of bus connection between the cores also increases which leads to the complex scenario system on chip. At same time the increase in the bus count will leads to the higher power consumption. To reduce the overall power consumption we have to reduce the bus count between the input and the output cores.

The overall power and the area of the practical multicore system directly increase with the overall interconnects we are using in architecture. While analyzing the chip level properties of the we found that major power consuming factor was buffers present in the input processors which consumes almost 67 % of total dynamic leakage power also the buffers presents in the conventional system consumes higher number of dynamic power and this power usage of buffers directionally proportional to the number of packets flows through the input and output ports. Practical research on buffers proves that these buffers using more leakage and dissipation power while transmitting packets when compare to the storing of the same packets. Also buffers are major area consuming factors in the NoC which is proved nearly 60% of overall NoC. In this paper we are focusing on the eliminating the buffers present in the conventional NoC systems.

The Multicore systems have the strong capacity of producing unmatched high range performance with the practically low cost by using the parallel processing technology. The overall processing speed of this multi core system practically used to measure the overall effectiveness and performance of the system. These multicore system having large number of small processors and using the N*N multistage bus interconnections. These interconnections are using the full duplex communication links for processing.

In this paper we are proposing the N*N multicore NoC system with efficient buffer less topology and novel bottleneck routing algorithm which deals with the low power technology. Here the crossbar switching topology having ability to limits the outgoing packet from the internal input ports to the outputs ports and output packets are arriving the output ports with less traffic and the higher throughput. But in the conventional systems when the throughput of the NoC achieves higher rate the latency of the system also goes high which leads to the performance loss. At the same time when more than two or more packets from the different routers are arriving for the same output at the time the bottleneck algorithm based crossbar router will store the packet in the FIFO so that only one packet will be forwarded to the output this will leads to the traffic elimination. By that way we can achieve the maximum throughput in proposed multicore NoC system with Bottleneck algorithm. Also the router will forward the remaining stored packet the output port when the particular output port was no longer used in processing packet. Our proposed FIFO having the infinitive storage cost which used to store all the packets which arrives crossbar router. The storage time depends on the availability of the particular output port when the particular output port was no longer processing at that time of instance the router will forward the packet from the FIFO memory. But for one cycle it will forward only one packet which was stored in the FIFO memory. But in conventional buffer based systems these buffers having finite limit storage cost and limited bandwidth for processing packets. Also in conventional systems when the buffer was full this leads to less throughput rate and its leads to the many issues in the multicore NoC systems.

In this paper we are making following contributions

- We are introducing in the novel bottleneck based routing algorithm for elimination traffic in the multicore NoC systems
- We present the buffer less scheme for storing and handling of incoming packets in the NoC core for minimizing the overall power usage. Simultaneously it will used reduce the overall area utilization of the NoC system.
- While detailing the architecture of the NoC system the router consists of large numbers of MUX and DEMUX based splitting architecture for making connection between the input and outputs. These circuits are using the multipliers as base operation this leads to higher power dissipation. Instead of this AND operation we are using XOR gate for making MUX and DEMUX and this will create a significant changes in overall power efficiency.
-

II. LITERATURE REVIEW

2.1.DME-enhanced Multi-core NoC Platform

DME based architecture for NoC system first suggested on 2010. From that suggestion the DME system used in the many kind of practical applications for the NOC system due to its

feasible memory architecture. In this technique they have separated the memory into private memory and the shared memory. The main architecture of the DME based NoC system showed in the below figure.

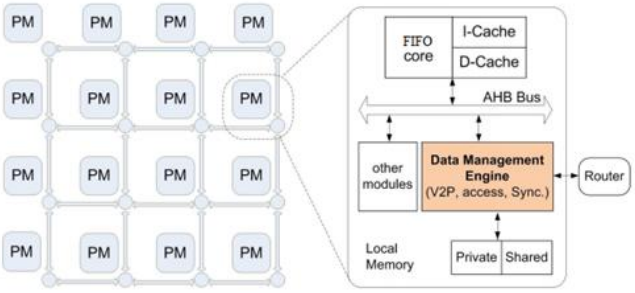


Figure (2) DME based NoC Architecture.

In DME based NoC system we are having separate memory as Private memory and shared memory and both the memory elements was connected with the router architecture via the interconnect bus system. Here they have used the FIFO system for creating cache based memory for faster processing. The shared memory used to store the common packets used by the all cores and private memory used to store the individual packets of the processor cores. By this way they had saved the unwanted storage cost of the system its leads to the lower power consumption as well as much lower delay.

2.2. Elastic Buffer Architecture for Network-on-Chip Routers

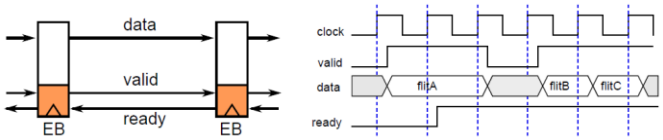


Figure (3) (a) Elastic Buffer Protocol (b) Handshake Protocol for the Elastic Buffer.

The above figure represents the elastic buffer protocol and here baseline of the elastic buffer was data bus and here they added additional two control lines for elastic representation, valid and ready those are the that two control lines. This elastic buffer used to replace the conventional buffer system. When the Elastic buffer receives an input it can generate the ready signal to upcoming packets also when the its stored by packet in buffer it will generate the valid signal to the output core by this way it can communicate with the input and output ports easily. When bot the control signals are positive at the time of instance the stored packet flows to the output port easily without any loss of data. Figure (3b) represents the handshake protocol of the elastic buffers.

2.3.Virtual Channel Regulator based NoC

In Virtual channel based NoC , they have suggested the virtual channel allocator called as ViChar which used allocate practical virtual channel for transferring packet from the input to the output ports and this allocator used to control overall packet flow of the system. This virtual channel allocator is separate mechanism which is used to determine available virtual channel by sensing the outgoing packet count and the overall traffic of the system. Also this virtual channel allocator used to control the availability of the buffers for the storing of the information's from to the memory core. This virtual channel allocator runs separate routing algorithm for routing packets from many multicore system.

2.4.Distributed Shared Memory NoC

In this technique they have suggested the distributed shared memory architecture based buffered NoC which having two separate buffers for storing incoming buffers and separate buffer for storing outgoing packet. Also they have added the pipelining process for efficient data handling with novel flow control algorithm for traffic elimination in the NoC. This method reduced nearly 60% of delay when compare to previous research methods. However this method not sufficient to create a power efficiency in multicore system.

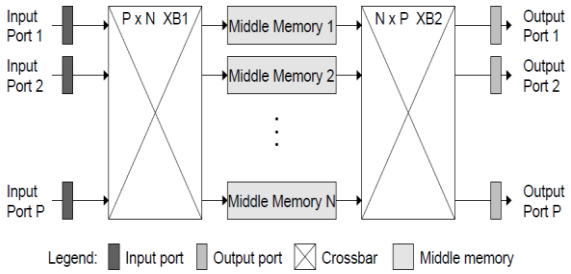


Figure (4) Shared Buffer based NoC system

2.5..Bless:

BLESS [5] is the first buffer less NoC. In this one hot-potato routing is used. The packet is injected by local processor only if one or more input links are free. The packets from input link are directed to any one of the output links. They are not saved in routers. The output link(s) which directs the packet towards its destination are called productive link(s). The output links which put the packet away from the required destination are called non-productive links. A packet may have either one or two productive links in a mesh network. A packet may have two or three non productive links in a mesh network. When competition arises for a particular output link, only one packet is assigned to productive link and other packets are assigned to non-productive links. All packets have a field to record the number of deflections. This field is initialized to zero when the packet is injected to the network. Whenever the packet is assigned to a nonprofit able port the count is incremented. The count remains same when profitable link is assigned to the packet. The packet with highest deflection count wins during competition for an output link. The winner is chosen randomly when two or more packets with same deflection count compete. It eliminates the live lock problem.

2.6.Chipper:

Bit field for deflection count is the main draw back in the BLESS [5] router. It increases the packet size. The deflection count is more than half of the diameter of the network. To increase the data ratio in packets CHIPPER [6] suggests a synchronous algorithmic approach. The deflection count field is removed in CHIPPER [6]. All routers are agreed to consider a packet as "gold packet" for a particular time period. This time period is called "golden epoch". In a golden epoch only one packet is considered as a gold packet. One golden epoch lasts for the circuit diameter number of clock pulses. The number of clock pulses for a golden epoch is known to all routers. It is equal to the worst case time of delivering a packet to the destination. Hence if a packet is considered as "gold packet" and it is always assigned to the profitable port during a golden epoch, then the delivery of gold packet is guaranteed within one golden epoch. This inspiration is exploited in CHIPPER [6]. All routers synchronously begin and end a golden epoch. In a golden epoch all routers synchronously and independently know the gold packet. For this they use a tuple (source number, packet number). These are initialized to first source number, first packet number in the first golden epoch. Invariably, this will be (0, 0). From the next golden epoch onwards the source number is incremented till all source number are covered. In the next golden epoch the packet number is incremented with the very first source number. Usually now the golden packet will be (0, 1). These iterations will go until the entire communication is over. Since the source number and packet number are available in the header field of all packets, it can be easily identified. Priority is given to this packet. In this strategy all packets becomes golden certainly. So, live lock is eliminated.

III. Problem Definition

The main problem of the NoC system was it having highest leakage power when compare to the other communication architecture, the main power leakage cause was buffers present in the NoC circuit, the buffers are having huge power dissipation factor. Here NoC cores having more than one number of input and output cores all the input and output cores are connected using the Crossbar router. If router busy with processing data means at the time of instance the incoming data will be losses due to the busy state of the router. To overcome these losses the traditional NoC system are using the Buffers for storing the input packets, after the storing of the data in Buffers system will add address parity to the data for classifying the respected output ports.

Buffers are the impedance based elements they are used to transfer the current form high impedance circuit from low impedance circuit. Using these properties they are used to store the data's for the particular period of time. But the main drawback of the buffers based system was it having the highest leakage power. This leads to more power consumption the NoC systems.

Removing power causing buffers from the NoC system also will leads to increase in traffic of the multicore chips. This traffic will cause the more number of data loss, due to the more number of data loss system should resend all the packets. Double the packets transmission cause the double the power usage. So that

elimination buffers from the NoC without traffic elimination algorithm was not a ideal solution for the NoC power minimization.

NoC crossbar switches using the Mux and Demux circuits for making connections between the input and output ports. The basic property of the Mux and Demux using the AND logic based multiplier circuits. More number of Multipliers present in the NoC also causes the high range of power usage. Finally we are concluding the Major power usage factors are Buffers presents in the Input Cores also the Traffic Problem will leads to packet drop, Power wastage and finally multipliers presents in the Mux and Demux circuits will leads to significant power loss.

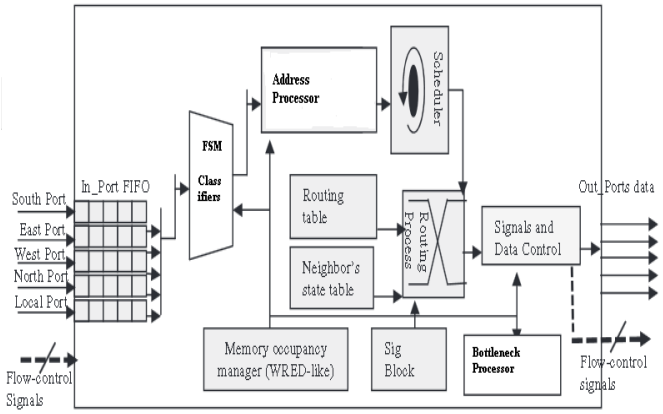
IV. Proposed System

We have proposed that energy efficient virtual memory based First In First Out scheme to enhance the power efficiency of these NoC crossbars. More importantly these virtual memory circuits producing some delay to read and input signal ie data, to overcome these effect we are incorporating bottleneck based routing technology. For eliminating the impedance based physical buffers presents in the traditional NoC system we are creating FIFO based Virtual NoC buffers which leads to the significant power reduction in the Multicore NoC system. This FIFO based Virtual buffers uses the FSM (Finite State Machine) Logic for maintaining all the input data without any losses. But the major consideration was elimination of buffers will leads to the traffic in the router crossbar. And it also will create a Data loss in the NoC system. For eliminating the Traffic we are suggesting the Bottleneck Based Routing algorithm in NoC system. The Novel Bottleneck based Routing Algorithm will detect the Overall packet processing Rate of the NoC system and depends upon the packet processing rate it will allows the packets to the Router with Varying Packet Size. If router packet processing was Busy means the NoC system will Allows packets with Minimum Size and if NoC Router Packet processing Rate was high means it will allows the Packets with Higher Size based on this algorithm this system will maintains the Minimum Traffic Rate and multicore NoC system.

For Eliminating the High power causing Multipliers presents in the Traditional NoC we are proposing the Xor based Mux and Demux circuits for reducing the overall power usage compare to the common multiplier based Mux and Demux our proposed Xor based Circuits having Lower power dissipation hence overall power usage of the NoC system will reduced.

V. Methodology

In our proposed system out each input channels are assigned as physical channel which is based on the addressing scheme to reach its desired output port. We are totally having 5 input port and 5 output ports. These port are interconnected using the crossbar switches. At the input stages the desired data input given to the virtual memory circuit, then that data will be given to the First In First Out circuit which is used to act as a Queue. The First in First out Circuit connected with the bunch of logic flip flop machine which called as FSM that is Finite State Machine, They act as a logic machine to separate addressing and the data from our input packets, The switching Circuit consists of following components Routing Compotator, crossbar Arbiter, switch and link traversal. We are using dedicated clocking circuit at the each stages of routing. This clocking circuit will make our data's as a pipeline processes data Which is easier to process, at stage of bottle neck routing with the virtual memory we are limiting the output packets with respect to the clocking period. This will leads to increase the processing speed of arbiter, which gives better performance in operation of the NoC. The holding time of the virtual buffer will controlled by the FSM structure. Mux and Demux circuits are used to interconnect the output ports and input ports , these circuits are using large of multiplier circuits this will leads to more power dissipation. To overcome this issue we are applying dynamic circuit design which consist of only Xor gates instead of AND gates. This will give better energy efficient results. In the proposed technique, the Dynamic CMOS technology is used to design the CMOS circuits, which requires less number of transistors. Various Dynamic CMOS technology is used to design the circuits such as Domino logic, Pseudo NMOS logic, Complementary logic, Transmission gate logic etc. From the above logic, any one Dynamic CMOS logic will be used to design the proposed circuits. Also capacitor is used in the Dynamic Logic with large number of NMOS transistor. Hence, Discharging or Pull Down is very easy when compared to the charging or Pull Up (i.e) Dynamic CMOS technology is best to reduce the leakage power also total circuit power. Also 65nm CMOS technology will be incorporated into the proposed system in order reduce the area and power utilization.



Fig(5) Overall Architecture of Proposed System with Buffer less Architecture

5.1. Buffer less Architecture

The First in First out (FIFO) circuit used to stores all the incoming asynchronous packets from the variable input cores. The overall capacity of the Network on Chip cores directly depends on the size of FIFO circuit. Basically the FIFO circuit independent of physical properties and its properties are maintained separately. Those FIFO based Architectures are used to overcome the power related problems produced by the traditional NoC systems.

5.2. Finite State Machine Classifiers

The FSM classifiers are used to identify the packet origin and responsible output port for the current packet and depends upon that it will add the address with current data. This address fields are used to transfer the packet to responsible output port without any losses. Later this address fields will be separate by the address Processors. Also it will maintain the virtual memory processor for maintaining the data without any losses. This virtual memory Architecture will helps to reduce the overall power usage of the Network on Chip Systems.

5.3.Address Processors

The address processors will process the incoming packets and forwards all the packets to their destinations without any losses in the packets. While processing the packets it will check the address presents in the packets and remove the address fields from the packets and forward those packets to the corresponding output ports with the help of routers. Overall memory used by the inputs ports are managed and controlled by the memory occupancy manager.

5.4..Router Scheduler.

The Router scheduler uses the Bottle neck algorithm for overcoming the traffic created by the buffer less architecture. Here we are applying the weight based algorithm for creating different weight for the router state and depends upon that we are applying the packets with the different sizes. This scheduling process also helps to reduce the overall complexity of the system,

5.5.Bottleneck Processer

The Bottleneck Processor used create a Novel Routing algorithm it used to create a seamless data flow between the input and output ports for that it will analyses the processing state of the Router crossbar switches. Depends upon the router crossbar switches state it will allows the packets with different size. If the crossbar switch was processing high number of packet means that time the bottleneck processor will splits the packets with different sizes and allows low size packets for the next cycle of the cross bar switches. Based on that we are overcoming the overall traffic created by the Buffer less NoC architectures.

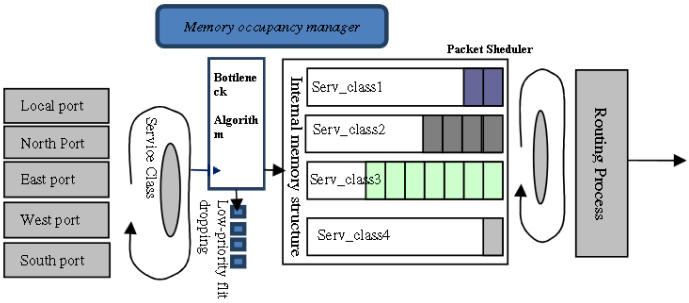


Fig (6) Architecture of Proposed Crossbar Switch

5.6.The Routing Crossbar

The router crossbar switches uses the many MUX and DEMUX circuits for making connections between the all the input and output ports. Usually the MUX and DEMUX circuits using the Multipliers based on the AND logic. This AND logics are having the high power dissipation properties. This AND based logic circuits causing the high leakage power and overall high power consumption. To overcome this problem we are eliminating the traditional AND based logic gates with the XOR based MUX and DEMUX circuits with the help of this modifications we are achieving the Low power usage with High Efficiency NoC processors.

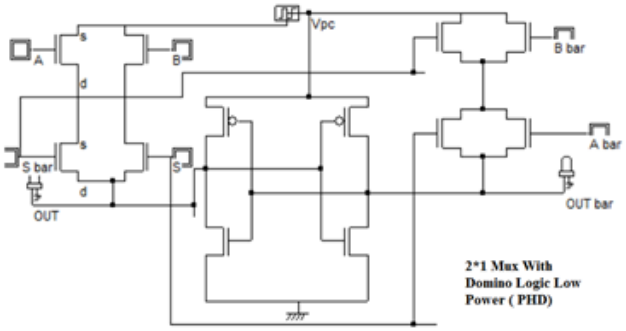


Fig (7) Proposed MUX Design susing XOR Gate Logic

VI. Results And Discussions

Performance Discussion

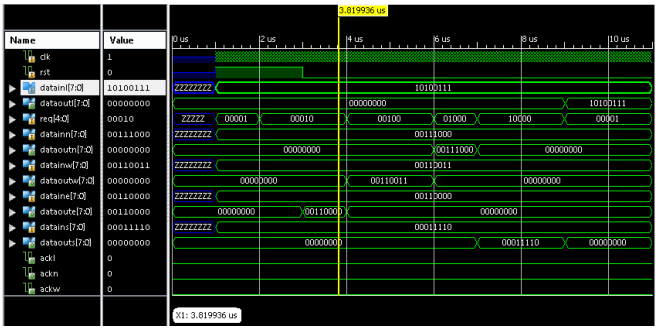


Fig (8) Simulation Results of Proposed Buffer less NoC Design

The proposed scheme was implemented and simulated using the Xilinx 14.2 tool and results achieved clearly showing that the overall power was reduced when compare to the conventional Network on Chip Architecture and also the proposed Buffer less NoC based Architecture having the best Power Efficiency ratio against the all possible at stages in communication processors.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1329	23872	5%
Number of Slice Flip Flops	1579	47744	3%
Number of 4 input LUTs	1065	47744	2%
Number of bonded IOBs	92	469	19%
Number of GCLKs	1	24	4%

The following figure (8) shows the overall Area utilized by the proposed Buffer less logic based NoC cores.. These results showing that the overall Area utilized by the proposed NoC was having very low area when compare to the existing systems.

Method	Frequency(MHz)	Dynamic Power (mW)
Proposed Scheme	1GHz	11
Conventional Scheme[1]	1GHz	30.96

And the below figure(9) shows that the overall power usage of the proposed Buffers less NoC with novel bottleneck algorithm based router. These results shows that power dissipation of the proposed scheme was 0.011W that is extremely reduced compare to previous conventional schemes.

VII. Conclusion

In this paper we have implemented buffer less architecture for Multi core NoC system for power efficient communication in Multi core systems. Also we proposed that Improvised bottleneck algorithm for congestion avoidance in Network on Chip core. This flow control schemes uses intelligent packet control scheme it allows different size of packets with respect to the different processing complexity of the router. Conventional crossbar switch was redesigned by XOR based MUX and DEMUX for better scaling in Power usage. This three proposed schemes are applied in the Multicore NoC system and results showing that overall power usage of the system was reduced nearly 30% when compare to the conventional routing schemes. Also the proposed scheme having best throughput with negligible delay with bottleneck algorithm scheme.

References

[1]. Ahmed Aldammas.: The efficiency of buffer and buffer-less data-flow control schemes for congestion avoidance in Networks on Chip. In: Journal of King Saud University – Computer and Information Sciences, pp. 96–112 (2016)

[2]. Carloni, L.P., Pande, P., Xie, Y.: Networks-on-chip in emerging interconnect paradigms: advantages and challenges. In: Proceedings of the 2009 3rd ACM/IEEE International Symposium on Networks-on-Chip, pp. 93–102 (2009)

[3]. Rahmani, A.-M., Latif, K., Vaddina, K.R., Liljeberg, P., Plosila, J., Tenhunen, H.: Congestion aware, fault tolerant and thermally efficient inter-layer communication scheme for hybrid NoC-bus 3D architectures. In: Proceedings of the 5th ACM/IEEE International Symposium on Networks-on-Chip, pp. 65–2 (2011).

[4]. Feero, B.S., Pande, P.P.: Networks-on-chip in a three-dimensional environment: a performance evaluation. IEEE Trans. Comput. **58**(1), 32–45 (2009

[5]. Pavlidis, V.F., Friedman, E.G.: 3-D topologies for networks-on-chip. IEEE Trans. Very Large Scale Integr. Syst. **15**(10), 1081–1090 (2007).

[6]. John Jose, Bhawna Nayak, Kranthi Kumar, Madhu Mutyam, "DeBAR: Deflection based adaptive router with minimal buffering", *in Design*

[7]. *Automation and Test in Europe Conference*, pp.1583-1588, March 2013.

[8]. Jing Lin, Xiaola Lin, Liang Tang, "Making-a-stop: A new bufferless routing algorithm for on-chip network", *Elsevier Publish Journal ofParallel and Distributed Computing*, pp.515-524, 2012.

[9]. Chris Fallin, Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu, "MinBD: Minimally-Buffered Deflection Routing for Energy-Efficient Interconnect", *in SixthIEEE/ACM International Symposium on Networks on Chip (NoC)*, pp.1- 10, May 2012.

[10]. Robert Mullins, Andrew West, Simon Moore, "Low-Latency Virtual- Channel Routers for On-Chip Networks", *ISCA*, 2004.

[11]. Cota E, Morais Antony, Soares Lubaszewski, "Reliability, Availability and Serviceability of Networks- on- Chip," *Springer*, 2010.

[12]. G. Michelogiannakis, D. Sanchez, W. J. Dally and C. Kozyrakis, "Evaluating Bufferless Flow Control for On-Chip Networks," *NOCS*, 2010.

[13]. T. Moscibroda and O. Mutlu. "A case for bufferless routing in on-chip networks," *ISCA-36*, June 2009.

[14]. M. Hayenga, N. Jerger, and M. Lipasti, "Scarab: A single cycle adaptive routing and bufferless network,"

[15]. Jerger, N.E., Peh, L.-S., Lipasti, M.: Virtual circuit tree multicasting: a case for onchip hardware multicast support. In: Proceedings of the 35th Annual International Symposium on Computer Architecture, pp. 229–240 (2008)

[16]. Hu, W., Lu, Z., Jantsch, A., Liu, H.: Power-efficient tree-based multicast support for networks-on-chip. In: Proceedings of 16th Asia and South Pacific Design Automation Conference, Piscataway, NJ, USA, pp. 363–368 (2011)

[17]. Wang, L., Kim, H., Kim, E.J.: Recursive partitioning multicast: a bandwidthefficient routing for networks-on-chip. In: International Symposium on Networkson- Chip (NOCS), San Diego, CA, May 2009

[18]. Chaochao, F., Zhonghai, L.U., Jantsch, A., et al.: Support efficient and faulttolerant multicast in bufferless network-on-chip. IEICE Trans. Inf. Syst. **95**(4), 1052–1061 (2012)

[19]. Feero, B., Pande, P.P.: Performance evaluation for three-dimensional networks-onchip. In: Proceedings of IEEE Computer Society Annual Symposium On VLSI (ISVLSI), pp. 305–310, 9th-11th May 2007

[20]. Millberg, M., Nilsson, E., Thid, R., Kumar, S., Jantsch, A.: The nostrum backbone communication protocols stack for networks on chip. In: Proceedings of IEEE Computer Society, International Conference on VLSI Design, pp. 693–696 (2004)

B.Nageshwar Rao. "An Improvised Bottleneck Routing Algorithm for virtual Buffer based energy efficient NoC's." IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 7, no. 4, 2017, pp. 48–55.