# IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)

### **Managing Editor Board**

- ❖ Dr. B. D. Venkatraamana Reddy Dept. of ECE, MITS, A.P, India
- Dr. Mohsin khan Rural Education and Development Foundation, Pakistan
- Dr. S.Sasikumar ANNA university, India
- Dr. P. Karthigaikumar Karunya University, India
- Dr. Rania Ahmed jazan university, Egypt
- Dr. Roukhe Hassane Ismac, Malaysia
- Dr. Aleksandr Cariow West Pomeranian University of Technology, Szczecin, Poland
- Dr. Swapnadip De Jadavpur University, India

#### **Contact Us**

Website URL: www.iosrjournals.org Email: Support@iosrmail.org









# **Qatar Office:**

**IOSR Journals** Salwa Road Near to KFC and Aziz Petrol Station, DOHA, Qatar

# **India Office:**

EHTP, National Highway 8, Block A, Sector 34, Gurugram, Haryana 122001

#### **Australia Office:**

43, Ring Road, Richmond Vic 3121 Australia

#### **New York Office:**

8th floor, Straight hub, NS Road, New York, NY 10003-9595



# IOSR Tournal of VLSI and Signal Processing **IOSR** Journals

**International Organization** of Scientific Research

p-ISSN: 2319 - 4197 e-ISSN: 2319 - 4200 Volume: 7 Issue: 4 Version-2

# **Contents:**

FPGA Implementation of Edge Detection using Modified Canny Edge and 01-06 **Adaptive Threshold** 

A High Performance Reconfigurable Data Path Architecture For Flexible 07-18 Accelerator

Technologies beyond Moore's Law: Simulation results of Heuristic Model 19-30

Low-Power, High-Throughput and Low-Area Adaptive Fir Filter Based 31-37 On Distributed Arithmetic Using FPGA

Identification of High-Risk Hardware Path-Delay Fault Locations and 38-47 **Evaluation of Their Impact** 

An Improvised Bottleneck Routing Algorithm for virtual Buffer based 48-55 energy efficient NoC's

Design and Estimation of Power, Delay and Area for Parallel Adder in 56-65 VLSI Circuits using 45nm Technology