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An Average power Estimation Technique for Integrated Circuits.

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Abstract: *As world is moving along with electronics, designing VLSI circuits, accurately estimate the silicon area and the expected performance are become most important analysis before the circuit goes into fabrication. The requirements for low power, makes the designers to analyze and optimize the MOS structures and their designs with respect to power dissipation. The accurate estimate of power dissipation at different levels is the design abstraction. In this paper the estimation of average power in MOS circuits. The circuit reliability gives an average power of battery life while maximum or peak power is related to performance of the circuit and the proper design of power and ground lines.*

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I. Introduction

The utilization of low power devices, increases use of portable and battery operated devices has raised With higher speed and density of CMOS circuits. The power dissipation has become an major issue for the researchers. Also, newer technologies are changing the balance of power between various dissipation mechanisms. Therefore the detailed power estimation is required to facilitate low power design and power optimization of CMOS circuits. Information on how the different components of power vary with different technologies is an important factor for any CMOS designer. It is also important to identify new techniques to estimate dynamic power in the presence of process variability caused power variation in gate delays. Currently, a common approach is to use Monte Carlo simulation of sample circuits taking into account the variation in delays. However, this is a time consuming approach. Thus, the need for a faster approach is required.

II. Power Dissipations In Cmos Circuits .

There are two kinds of power dissipations.

1. Static Dissipation
2. Dynamic Dissipation

The static dissipation is depended on the short circuit current, leakage activity and power consumption due to stand by mode of the CMOS device [1]. This power consumption can be estimated through a proper analyzing the CMOS working conditions on which the device power consumption. Paper describes the techniques in which power consumption of capacitive switching in particular and short-circuit current, Power estimation approaches can be estimated .

1.1 Simulation Techniques:

The direct simulation or statistical sampling techniques has been used to analyze. The hazard generated and propagation delay, fan out conditions , correlations, are taken into consideration. If performed after layout and parasitic extraction, accurate estimation of capacitances and their effects is possible. A circuit simulator such as P-Spice is used for estimation of power. A gate-level HDL simulation using tools, can also be utilized to report power dissipation using power models of gates from the library.

1.2 Probability Switching Techniques:

The probability [1] of switching activity that is Probabilistic approaches are being carried out because the strong pattern dependence and simulation based approach is will be having more running time for the designed circuits. Further to this at each gate node and the node's power consumption can be estimated and increase the performance estimation, this will help designer to estimate the power utilization of circuit and provide better options circuit power consumption calculation.

The transition probability of each gate is carried out by using P-spice and Cadence Design Systems.

These approaches uses an infinite driver and short-circuit power , follows a simple Spice simulation based approach to generate the look-up tables for wires with interconnect for different lengths, using these can compute for power consumption for different integrated circuits.

Take a switch factor based approach to model capacitive coupling[2] , incorrectly assumes the worst-case switch factor to be one, and also assumes all lines to be transitioning simultaneously essentially modifies activity factors of lines to take into account neighbor switching. The slew rate

Timing and switching options are neglected. The above-mentioned techniques compute average power consumption in a design.

Complexity of circuits made to decrease in device size and to increase the speed the operating frequency becomes more relevant because of these arrangements switching activity increases and intern power consumption becomes more critical. performance and reduces chip life-time. To control their temperature levels, high power chips require specialized and costly packaging and heat-sink arrangements.

This, combined with the recently growing demand for low-power portable communications and computing systems, has created a need to limit the power consumption in many chip design. The low-power design techniques as a technological need of the Semiconductor design and development.

To design make any analysis tools are very important in such Computer Aided Design (CAD) tools will be playing vital role. Using these tools make designers to understand the design of integrated circuits in a more efficiently so that designer can estimate the performance of the device such as estimation of power consumption, speed parameter calculation and so on .

The simple solution of estimating power by using a simulator is complex because of pattern-dependence problem. Input signals are generally un- known during the design phase because they depend on the system in which the chip will eventually be used.

It is practically impossible to estimate the power by simulating the circuit for all possible inputs. several techniques have been proposed to overcome this problem by using probabilities to describe the set of all possible logic signals, and estimating the power resulting from the collective influence of all the signals. Thus the formulation gives a certain amount of pattern-independence that allows effectively estimating and manipulating the power dissipation.

III. Average Power Estimation Technique

In many electronic applications, it is important to consider the instantaneous power or the stable power in a circuit. Such estimation is important for the design of voltage drop on lines, power and ground lines,. It is important in mobile applications where battery life is important for average power dissipation with the scaling of device sizes, when more transistors are used, the instantaneous current can be large due to the simultaneous switching of a large number of logic gates. Since the power ground lines are associated with some inductance *L*, the voltage drop due to such a change in current is equal to *L di(t)/dt* .

Therefore, there is a need to accurately estimate the instantaneous power and current. Estimation of maximum dynamic power requires to determine the average dynamic dissipation in nmos and pmos devices of the circuit to induce maximum switching of capacitance. These kind of estimations are complex by the fact that logic gates have finite delays.

There fore need to determine the input voltage such that the total switched capacitance due to both functional and transitions are formed. The problem of the maximum power estimation is difficult because the problem is incomplete.

This paper is to determine lower bounds of power so that the bounds can be effectively used during the design of VLSI circuits and systems.

3.1 Transition Based Approach

In a CMOS circuits, the power dissipation during switching activity , the circuit is dominated by the dynamic current, and hence the instantaneous power dissipation due to two consecutive inputs P0,P1 correspond to probability of having logic 0 and logic 1 respectively .

This switching activity leads to measuring a speed of the device . the switching speed of CMOS is time taken by a capacitor to charge and discharge of the signals .

There fore gate delay can be formulated as

$$G_{TD} = R_{On} * C_g$$

For this activity the power dissipated at gate will be a static and dynamic component dissipation and this can be written as

For static dissipation[2]

$$Ps = (Vdd)^2 / R_{On}$$

For dynamic dissipation

$$Pd = Eg * f_0$$

When $Eg = C_g / 2 * (Vdd)^2$

$$f_0 = w/l * u C_0 Vdd / C_g$$

The above analytical components represents during switching action, when CMOS logic gate makes a logic transition In CMOS circuits, the capacitive load of a logic gate can be approximated by the fan out of the gate. Therefore the dynamic power dissipation due to two consecutive input vectors can be represented as[1]

$$P_{avg} = C_{load} (Vdd)^2 \; f clk * nT$$

nT represents node transition factor which is the effective number of power consumption can be analyzed and expressed .

This average switching power dissipation of CMOS logic gates suggests that several different means for reducing the power consumption . Which includes reduction of supply voltage , voltage swing , switching probability and reduction in load capacitance .

IV. Conclusion

The reduction of power supply, and measuring the switching activity are widely used to estimate power consumption in the nitrated circuit. In this paper discussed the techniques separating and estimating the different power dissipation components and power consumption the average power estimation of dynamic power requires to determine the primary input vectors of a circuit to induce maximum switching of capacitance .This average power estimation technique addresses important issues like power dissipation in the integrated circuit. with this a low power and effective system performance can be achieved .

References

[1]. V. D. Agrawal, "Low-Power Design by Hazard Filtering," in Proc. Tenth International Conf. on VLSI Design, Jan. 1997, pp. 193–197.

[2]. V. D. Agrawal, M. L. Bushnell, G. Parthasarathy and R. Ramadoss, " Digital Circuit De- sign for Minimum Transient Energy and a Linear Programming Method," in Proc. Twelfth International Conference on VLSI Design, Jan. 1999, pp. 434–439.

[3]. V. Bartkute and L. Sakalauskas, "Three Parameter Estimation of the eibull Distribution by Order Statistics," in C. H. Skiadas, editor, Recent Advances in Stochastic Modeling and Data Analysis, pp. 91–100, World Scientific, 2007.

[4]. J. W. Bierbauer, J. A. Eiseman, F. A. Fazal, and J. J. Kulikowski, "System Simulation with MIDAS," AT&T Tech. J., vol. 70, no. 1, pp. 36–51, Jan. 1991.

[5]. L. Bisdounis, S. Nikolaidis, and O. Loufopavlou, "Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter," IEEE Trans. Circuits and Systems I: Funda- mental Theory and Applications, vol. 45, no. 3, pp. 259–270, Mar. 1998.

[6]. S. Bobba and I. N. Hajj, "Maximum Leakage Power Estimation for CMOS Circuits," in Proc. 15th International Conf. on VLSI Design and 7th Asia and South Pacific Design Automation Conf., Jan. 1999, pp. 116–124.

[7]. A. Bogiolo, L. Benini, and B. Riccò, "Power Estimation of Cell-Based CMOS Circuits," in Proc. Designtomation Conf., 1996,

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