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Multiple Constant Multiplication Architecture Using Graph Based Algorithm

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Abstract: *Efficient algorithms and architectures exist for the design of low-complexity bit-parallel multiple constant multiplications (MCM). This operation dominates the complexity of many digital signals processing system. Alternative to this, digit-serial MCM design is available with less complexity. But it is not as much popular as the former one. Here the gate –level area and power of digit-serial MCM design is tried to optimize. So initially from the basic parallel designs, like shift –adds implementation, the common sub-expression elimination and graph-based method are used. From this the efficient one is selected, that is the GB technique and is applied to digit-serial design. Then the newly designed MCM block will be placed to the multiplier block of an FIR filter. Thus comparing to bit-parallel FIR filter design, digit-serial design has power reduction and area reduction and are independent of data word-length. These algorithms are implemented using Xilinx ISE 10.1 simulator. The power, area and delay of the algorithms are computed using cadence.*
Keywords: *Cadence,Multipliers,MCM,Xilinx.*

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I. Introduction

Finite impulse response filters are of great importance in digital signal processing (DSP) systems since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high-performance filters. The direct and transposed-form FIR filter implementations are the two types. Although both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency. The multiplier block of the digital FIR filter in its transposed form, where the multiplication of filter coefficients with the filter input is realized, has significant impact on the complexity and performance of the design because a large number of constant multiplications are required. This is generally known as the multiple constant multiplications (MCM) operation and is also a central operation and performance bottleneck in many other DSP systems such as fast Fourier transforms, discrete cosine transforms (DCTs), and error-correcting codes. Although area-, delay-, and power-efficient multiplier architectures, such as Wallace and modified Booth multipliers, have been proposed, the full flexibility of a multiplier is not necessary for the constant multiplications, since filter coefficients are fixed and determined beforehand by the DSP algorithms. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift adds architecture, where each constant multiplication is realized using addition/subtraction and shift operations in an MCM operation. For this implementation of constant multiplications, a straightforward method, generally known as graph based method is used.

II. CSE Algorithm

The CSE algorithms are directly obtained from the digit-based recoding methods. In this, first we find common sub patterns in the representations of the constants after the constants are represented in conventional number representation such as binary and CSD formats. The main drawback in these algorithms is the performance of these algorithms depends on the number representation. This problem can be considered as NP-complete and its optimal solutions does in general not provide the optimal MCM solution. Recently, Dempster and Macleod proposes alternative number representations to find feasable solution for the MCM problem.

The main idea of common sub-expression elimination algorithm is to find the digit terms which are common between different constants and if they have common expressions then decrease the number of

repeated expressions by sharing. It has many algorithms which deal with CSE and in most all algorithms have main three steps. They are:

1. Identify the multiple expressions present in the input matrix of coefficients.
2. Then select one expression for elimination
3. Finally eliminate the same expression in all coefficients and share it.

This process is repeated until there are no more multiple expressions present in the multiple constants. There are two important metrics in this algorithm which are run time and quality of the solution. The following example explains CSE algorithm. Usually multipliers have large area and power and also multiplication is expensive in hardware. In MCM, since the constants are fixed and known before hand. Hence, multiplications are implemented by using shift and add/subtract methods. Suppose if you want to compute 29*x and 43*x. The constant 21and 43 are represented in binary format as 11101 and 101011. So, by using shift and add method we can compute them as below:

29x=(11101) = x<<4+x<<3+x<<2+x

43x=(101011) = x<<5+x<<3+x<<1+x

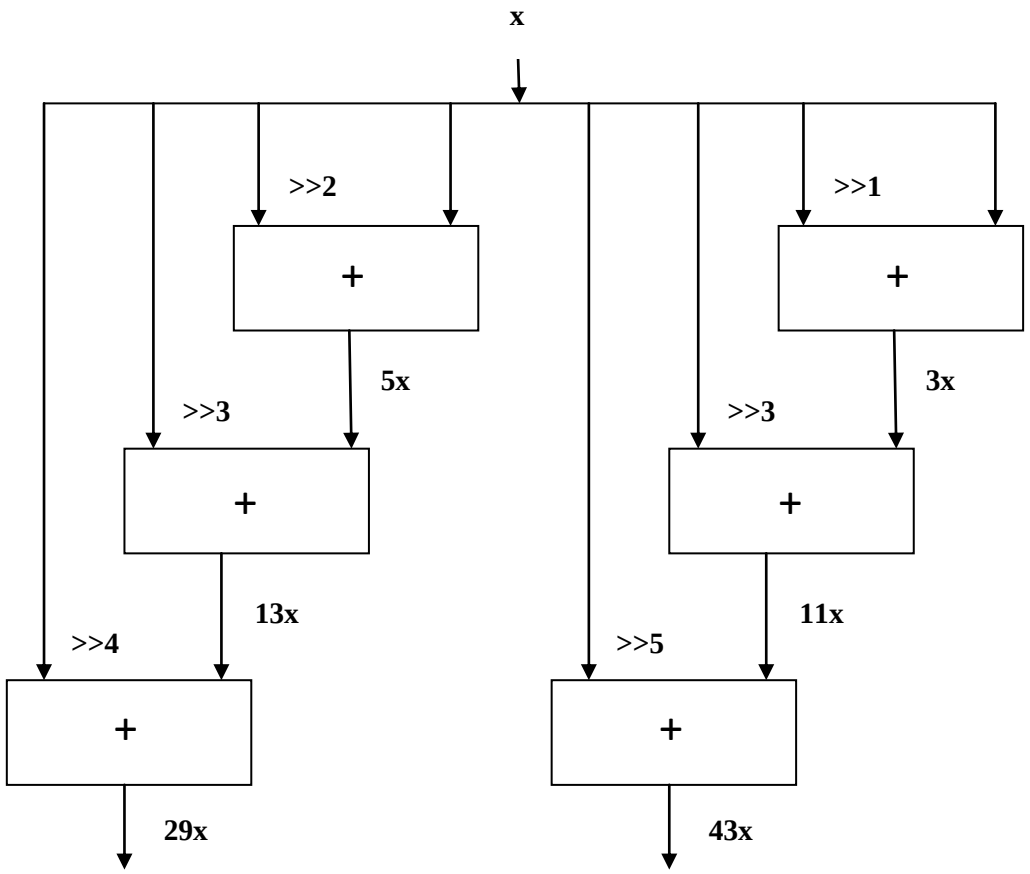

Fig.1 Flow Diagram of CSE Algorithm Without Product Sharing

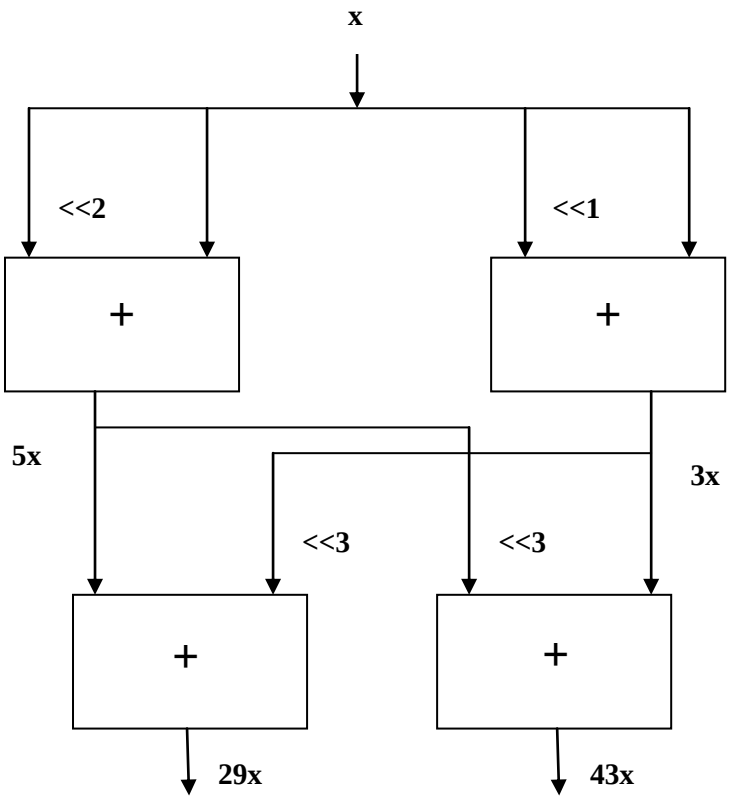

Fig.2 Flow Diagram of Exact CSE Algorithm

1.1 CSE Simulation Results

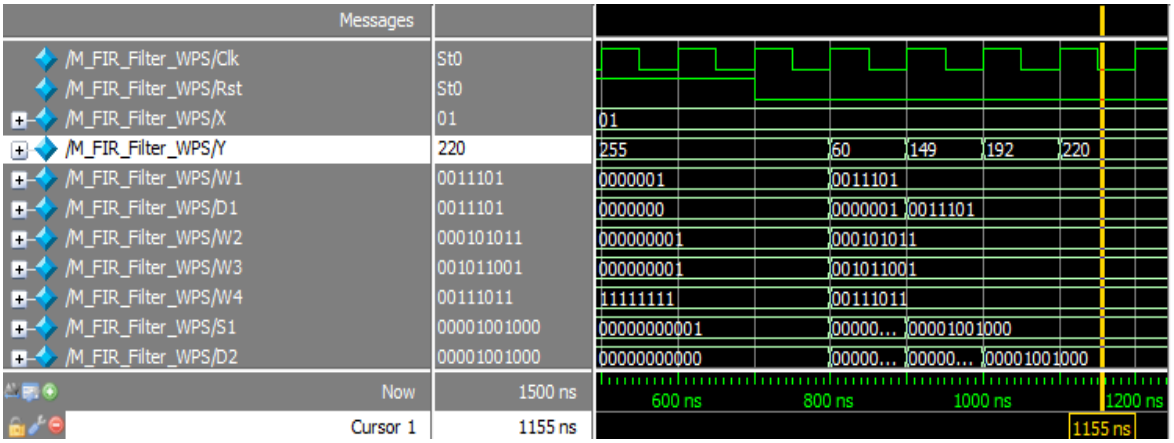

Fig.3 Simulation Result

III. GRAPH BASED ALGORITHM

To design MCM architecture without Common Sub-expression Elimination (CSE) algorithm is used in this method. In this Graph Based (GB) algorithm four constants are taken as taken as coefficient pair. According to MCM principle constant multiplication is performed by number of shifting and addition operation. For this purpose compare with other algorithms, GB algorithm is used to find number of shifting and addition operation. Consider the first coefficient pair as 29x and 43x. For this pair, without partial product sharing algorithm requires six addition and six shifting operations and CSE algorithm requires four additions and four shifting operations. But GB algorithm requires only one subtractor, two adders and three shifting operation. Steps of GB algorithm can be applied for any coefficient pair combinations. Hence GB algorithm is used and number of operation is reduced drastically than other algorithms.

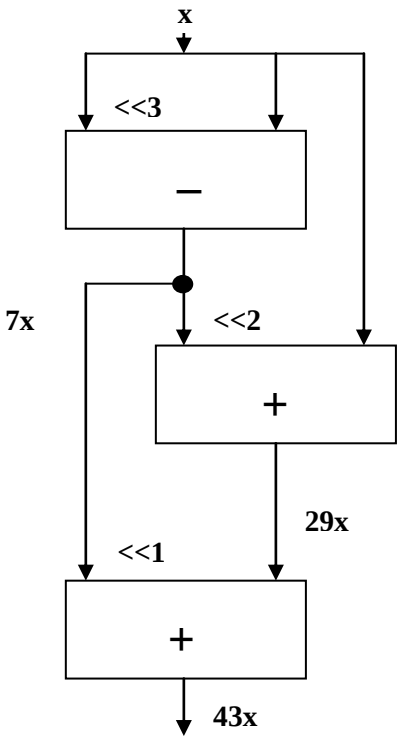

Fig.4 Flow Diagram of GB Algorithm

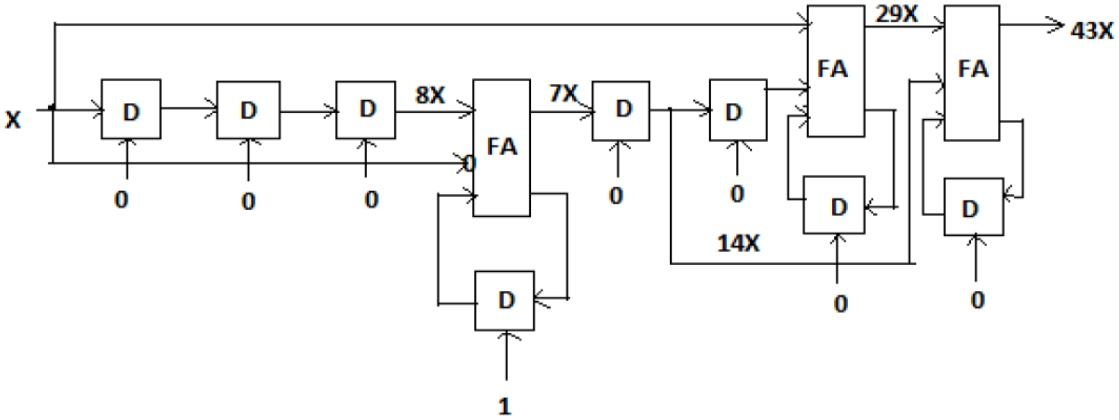

Fig.5 Block Diagram of GB Algorithm

1.2 Graph Based Simulation Results

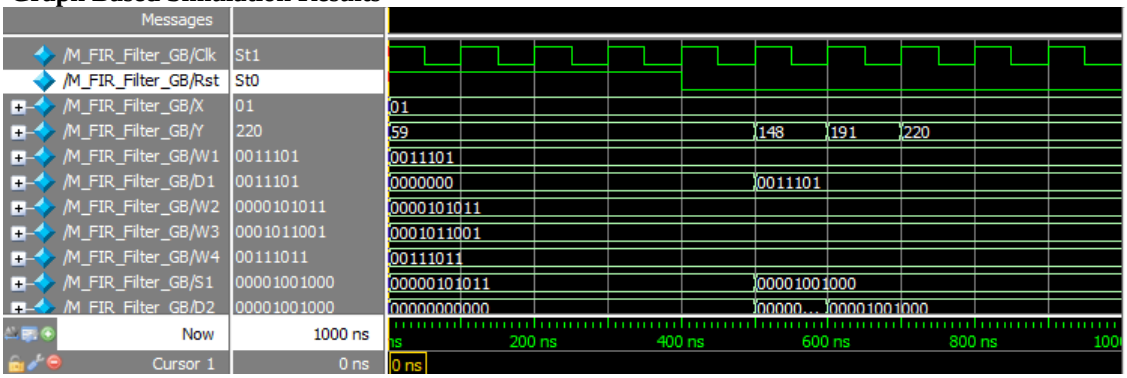

Fig.6 Simulation Result

IV. Performances Result of These Algorithm

MCM algorithms are implemented using Xilinx software and power ,delay and area are computed using cadence tool

Table.1 cadence Results

Algorithms	Delay (ns)	Power (mW)	Area
CSE	11.764	222	29
GB	6.216	215	14

V. Conclusion

Thus the implementation of digit serial FIR filter was implemented with low complexity MCM architectures using GB algorithm. Hence this MCM approach drastically reduces the system complexity, area and delay and FPGA hardware real time implementation has performed with spartan3 version. Device utilization and delay values are compared for hardware implementation. Future enhancement of this paper is to design MCM architecture with more coefficient pairs for FIR filter implementation.

Refernces

[1]. L. Aksoy, E. Costa, P. Flores, and J. Monteiro, "Exact and approximate algorithms for the optimization of area and delay in multiple constant multiplications," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 6, pp. 1013–1026, Jun. 2008.

[2]. Y.-H. Ho, C.-U. Lei, H.-K. Kwan, and N. Wong, "Global optimization of common subexpressions for multiplierless synthesis of multiple constant multiplications," IEEE Explore,pp.119-124, 2008.

[3]. Dempster and M. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 42, no. 9, pp. 569–577, Sep. 1995.

[4]. H. Nguyen and A. Chatterjee, "Number-splitting with shift-and-adddecomposition for power and hardware optimization in linear DSPsynthesis," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8,no. 4, pp. 419–424, Aug. 2000.

[5]. Y. Voronenko and M. Püschel, "Multiplierless multiple constant multiplication," ACM Trans. Algor., vol. 3, no. 2, pp. 1–39, May 2007.

[6]. C. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron.Comput, vol. 13, no. 1, pp. 14–17, Feb. 1964.

[7]. O. Gustafsson and L. Wanhammar, "ILP modelling of the common subexpression sharing problem," in Proc. ICECS, 2002, pp. 1171–1174.

[8]. M. Potkonjak, M. Srivastava, and A. Chandrakasan, "Multiple constant multiplications: Efficient and versatile framework and algorithms for exploring common subexpression elimination," IEEE Trans. Comput-Aided Design Integr. Circuits Syst., vol. 15, no. 2, pp. 151–165, Feb.1996.

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