

Computation and Analysis of Excitatory Synapse and Integrate & Fire Neuron: 180nm MOSFET and CNFET Technology

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Abstract :Neuromorphic circuits and systems are mixed analog and digital hardware implementations of biological networks. The Neurons and Synapses form the basic building blocks of these networks analogous to their biological counterparts. The analog VLSI implementation of neuron and synapse circuits with devices working in subthreshold regime ensure compactness and low power consumption in these circuits. The use of advanced technologies of MOSFETs has further improved the area and power efficiencies of the neuromorphic circuits. In this work, we have implemented a Static Excitatory Synapse circuit and an Integrate and Fire Neuron circuit in 180nm technology. The circuits are simulated using Cadence software and verified for the functionality with varying circuit parameters. Further, the Static Excitatory Synapse circuit is cascaded to an Integrate and Fire Neuron circuit and simulated with adjusted component and parameter values in 180nm MOSFET technology in Cadence software and the Carbon Nanotube Field Effect Technology in HSPICE software as well. The effect of the parameter values on the functionality of the cascaded circuit and the passage of signals is studied, analyzed and compared in the two technologies in terms of power and area efficiencies of the circuits.

Keywords–Carbon Nanotube, Neuromorphic, Neuron, Synapse.

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I. INTRODUCTION

Neuromorphic Engineering is a branch of Electronics Engineering that deals with the design and architecture of electronic circuits and systems inspired from the biological networks. Carver Mead initiated the investigation in the field of building up of circuits and systems based upon the operational and organizational principles of biological systems at Caltec in late 1980s [1]. The term “neuromorphic” coined by Carver Mead refers to analog VLSI Artificial neural systems based on biological nervous systems. The Neuromorphic Circuits provide much higher efficiency in computation of large data in parallel as compared to the digitally simulated Neuronal networks and the traditional digital computation systems based on Von Neumann architecture. These systems are suitable for real time large scale neural emulations which is not possible in the other computing systems. Further, the neuromorphic circuits in a VLSI are much compact and consume less power as compared to their digital counterparts [2]. The large scale dense, compact, and low power neuromorphic circuits find their applications in implants and prosthetics.

A group of researchers in the field of Neuromorphic Engineering are working on the implementation of compact low power circuits operating in real time which can be integrated with the biological system. The pioneering work in this field has been done by Giacomo Indiveri, Institute of Neuroinformatics at Zurich. The basic components building up these systems are the neurons and synapses analogous to the biological systems. The use of subthreshold regime of the devices in these circuits results into very low power consumption in the circuits. The innovative field of Neuromorphic Engineering thus utilizes the combination of power and area efficiencies of analog circuits with programmability of digital architectures to build up robust and implantable systems. The implementation of such large-scale hardware neuromorphic systems need dense packaging of neurons and synapses to achieve volumes comparable to biological networks in human brain. The challenge therefore is in developing compact and low power neuron and synapse circuits which can mimic the functionality of their biological counterparts.

The neurons are the basic signaling units of the nervous system and has four main regions to its structure: Cell body or Soma, dendrites, axons, and presynaptic terminals. The cell body of the neuron integrates

synaptic input signals received from various other neurons through its dendrites to generate an output signal known as the action potential in case this stimulus crosses a certain threshold value. The action potential propagates through the axon of the neuron to its presynaptic terminal. The signal from the presynaptic neuron is transferred to the post synaptic neuron at the sites called synapse. The synapse is the area of contact between the two neurons. The neurons do not actually physically touch and are separated by the synaptic cleft. The synapses form communication links between neurons and are responsible for computation and transfer of electrical signals through chemical interactions from pre-synaptic neuron to the post-synaptic neuron [3]. There is a period called the refractory period after an action potential has been fired in which it may be virtually impossible to initiate another spike. The communication between neurons via synapse in biological nervous system is shown in Fig. 1.

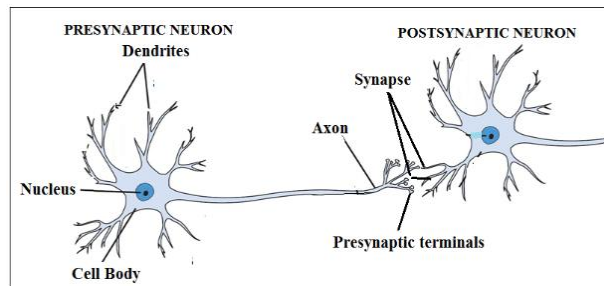


Figure 1. Structure of biological neuron and synapse

The efficiency of the neuromorphic network is largely dependent upon the modelling, biological plausibility and implementation of the neuron and the synapse hardware circuits which form the basic building blocks of these networks. There have been many neuron models proposed in literature which include varying features of biological neurons and have been formulated as electronic circuits that can be realized in Analog VLSI circuits. Lopicque developed a phenomenological neuron model in 1907 to model the action potential of a neuron in simple manner [4]. Hodgkin and Huxley in 1952 proposed the first detailed neuronal model which was a multicompartiment model that included the dynamics of the voltage dependent membrane conductance responsible for the generation of action potential [5]. The first ever analog VLSI implementation of this model was proposed by Mahowald and Douglas in 1991 [6]. The models proposed by Morris Lecar [7] and FitzHugh-Nagumo [8] are simplifications of the conductance based Hodgkin and Huxley model. Though the conductance based aVLSI implementation of neurons offer high degree of biological realism but occupy large amount of silicon area. The Integrate and fire model of neurons is a phenomenological model with significant explanatory power in understanding the behaviour of neuronal networks both in theory and simulation. The Integrate and Fire neurons integrate presynaptic input currents and generate a voltage pulse analogous to an action potential when the integrated voltage reaches a threshold. The first simple VLSI version was probably the Axon Hillock circuit built by Mead in late 1980s [1]. Starting from this circuit an entire generation of Integrate and Fire neurons have been designed with each one introducing some new features or optimizing certain aspects found in real neurons [9, 10]. The analog circuits based on Integrate and fire neuron models are well suited and most widely used neuron circuits for large scale Neuromorphic hardware network implementations owing to their edge over other models in terms of area and power efficiencies.

Synapses are the specialized junctions which mediate interactions between the biological neurons and form connections between silicon neurons too. They are fundamental elements for computation and information transfer in both real and artificial neural systems. These synapses can be excitatory which source current into the postsynaptic membrane capacitor leading to its depolarization or inhibitory which sink current from the postsynaptic membrane capacitor leading to its hyperpolarization. The chemical synapses are responsible for the interaction mediated via neurotransmitters between the presynaptic and postsynaptic neurons. The arrival of the presynaptic spike at the presynaptic terminal of the neuron initiates the release of neurotransmitters. The neurotransmitters act on the receptor molecules in postsynaptic membrane leading to alteration in the ionic fluxes. The change in the ionic fluxes result into the change in postsynaptic membrane potential which leads to firing of action potential when it exceeds the cell membrane threshold voltage [11]. The excitatory synapses in the neural networks can be static with constant gain or dynamic with modification in the synaptic strength during computation. The static synapses are specified by a fixed weight during operation whereas the effective conductance of the membrane channels change in dynamic synapses. Many models are reported in literature to capture the nonlinear properties and the dynamics of real synapses. The aVLSI circuits based upon these models efficiently reproduce the synaptic dynamics in real time [10, 12, 13]. These circuits convert input spikes into analog charge which then produces post-synaptic currents that get integrated at the membrane capacitance of the post-synaptic neuron. The pulse current source synapse is one of the simplest synaptic circuits in which the

circuits consist of a voltage controlled subthreshold current source transistor in series with a switching transistor activated by the input spike [11].

The human brain contains about 85 billion neurons and each neuron may be connected to other neurons via as many as quadrillion (10^5) synaptic connections and requires only 20 watts of power and performs complex computations and tasks in this small power budget [14]. The implementation of such dense low power hardware networks emphasizes on the need of compact and scalable devices with very small footprints and very low power consumption. The MOSFETs are the most prominent devices used for the implementation of these circuits which have been constantly benefitted in terms of area and power consumption with the advanced technology nodes of semiconductor fabrication technology. However, the CMOS technology is now approaching its final scaling limits towards the end of Moore's law. Thus, there is a quest for an alternative novel device which may replace MOSFETs in the circuits and continue with the Moore's law.

Carbon Nanotube field effect transistor (CNFET) is a promising novel device which has superior device characteristics as compared to traditional MOSFET. CNFETs are one of the potential devices which may be utilized in neuromorphic systems for emulation of biological networks in terms of density, scale, and power consumption. Carbon nanotube based systems may be useful in implants and prosthetic as CNTs have been used to interact with living tissues [15]. The Stanford CNFET model proposed by Jie Deng is based upon MOSFET like CNFET containing single walled CNTs bridging the distance between source and drain. The CNTs present in the channel region provide ballistic or near ballistic transport of carriers under low voltage bias as it has ultra-long ($\sim 1\mu\text{m}$) mean free path for elastic scattering. The circuit compatible complete CNFET model is implemented hierarchically in three levels including all the practical device non-idealities [16,17]. The HSPICE software is based upon the Stanford CNFET model.

In this work, we have ported a static excitatory synapse circuit and an integrate and fire neuron circuit shown in Fig. 2 and Fig. 3, already reported in literature [10], to 180nm technology using Cadence software. Both the circuits are simulated and analyzed for varying parameter values to confirm their functionality. The static excitatory synapse circuit is then connected to an integrate and fire neuron circuit and simulated in 180nm technology using Cadence software. The simulations are carried out with adjusted and matched parameter values in the connected excitatory synapse and neuron circuits such that spike pulse input given at the input of the synapse circuit forces the neuron circuit to fire a similar spike pulse at its output. To check the feasibility of CNFET technology in implementation of neuromorphic circuits the static excitatory synapse circuit implemented in CNFET technology [18] is connected to the Integrate and fire neuron circuit in CNFET technology [19] with adjusted component and parameter values and is simulated using Stanford CNFET model of HSPICE software.

The synapse and neuron circuit interconnections are checked and analyzed for their functionality in 180nm MOSFET technology as well as in CNFET technology. A comparison of power consumption in 180nm MOSFET and CNFET technologies is also carried out. The study and analysis of the hardware aVLSI static excitatory synapse circuit connection to integrate and fire neuron circuit in CNFET technology is done to ensure the possibility and feasibility of implementation of low power dense neuronal networks in Neuromorphic systems. The CNFET technology may be benefitting in terms of area and power consumption in neuromorphic network implementations in future.

II. CIRCUIT DESIGN

The static excitatory synapse circuit and the Integrate and fire neuron circuits are the basic component modules which are connected for the study and analysis of communication between neurons and signal transfer from a synapse to the post-synaptic neuron in this work.

2.1. The Static Excitatory Synapse

The Fig.2 shows the circuit diagram of a static excitatory synapse circuit originally proposed by Giacomo Indiveri [10]. It passes the spike pulse voltage input V_s from a presynaptic neuron to a postsynaptic neuron in the form of a steady state current. The pre-synaptic input pulse V_s is fed to the transistor M1 which acts as a switch and switches on when there is a pulse but remains off in between the pulses. The synaptic weight V_w drives the discharge transistor M2 which acts as a voltage controlled subthreshold current source and controls the rate of discharge of the capacitor C1 when a pulse appears at the input of M1. The capacitor C1 is charged towards V_e via the diode connected transistor M3 in between the pulses. The voltage across the capacitor drives the transistor M4 and hence controls the post synaptic current I_d .

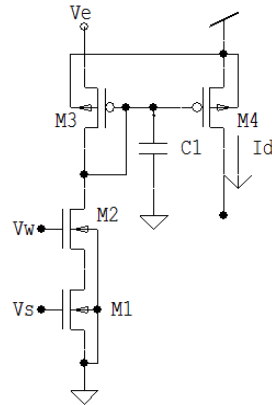


Figure 2. Excitatory Synapse Circuit [10]

The capacitor C1 is charged towards V_e via the diode connected transistor M3 initially in absence of input pulses. On occurrence of a pulse, the capacitor starts discharging via transistors M1 and M2 and the voltage across the capacitor decreases. As the capacitor voltage is driving PMOS transistor M4 the current I_d through transistor M4 increases exponentially with decreasing voltage across the capacitor C1. In between the spikes the capacitor charges towards V_e and the current I_d decrease exponentially. This process continues with until I_d reaches a mean steady state value in presence of a pulse spike train V_s driving M1. The increased synaptic weight in the circuit increases the gain and hence the mean steady state value of output current I_d of the circuit. Further, the increase in the frequency of the input pulse V_s leads to increased integration rate which again results into a higher steady state value of the output current I_d for constant synaptic weight in the circuit.

2.2. The Integrate and Fire Neuron

The Fig. 3 shows the circuit diagram of an Integrate and Fire neuron originally proposed by Giacomo Indiveri [10]. The post synaptic current output from the synapse circuit serves as the input current I_{inj} to the Integrate and fire neuron shown in Fig. 3. The current I_{inj} is integrated by the membrane capacitance C_{mem} which leads to an increase in the membrane potential V_{mem} . As the potential V_{mem} goes above the threshold voltage V_{thr} of the transconductance amplifier, formed by transistor M1 to transistor M5, the output of the transconductance amplifier goes high. This results into the generation of an action potential at the output V_{out} via two inverters. The high output voltage activates the positive feedback in the circuit leading to an increase in the membrane voltage V_{mem} above V_{thr} by a fraction $\frac{C_{fb}}{C_{mem} + C_{fb}}$ thus ensuring that the output is not hampered by any noise at the input.

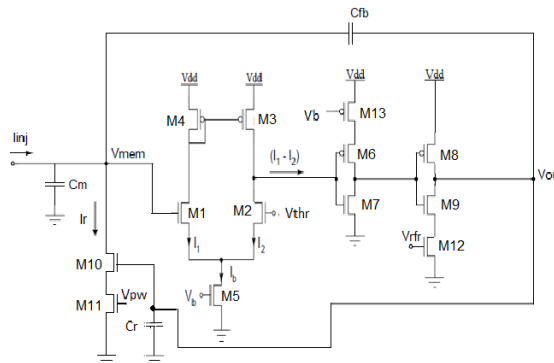


Figure 3. Integrate and Fire Neuron Circuit [10]

The output voltage V_{out} drives the transistor M10 in the discharge circuit formed by transistor M10 and transistor M11. As the output V_{out} goes high transistor M10 switches on and membrane voltage V_{mem} starts discharging at a rate set by the pulse width control voltage V_{pw} . It implies that the discharge current I_r is controlled by the voltage V_{pw} . As V_{mem} goes below V_{thr} , the output of the transconductance amplifier becomes low resulting in a low voltage at the output.

The refractory period of the neuron is controlled by the refractory control voltage V_{rfr} which drives the transistor M12. As the output voltage V_{out} goes low, transistor M9 switches on and the capacitor C_r discharges via transistors M9 and M12 at a rate set by the refractory control voltage V_{rfr} . In this period no pulse can be generated at the output and hence this period corresponds to the refractory period of the neuron. The pulse width duration t_{high} as per the mathematical model of the circuit [1] is expressed as,

$$t_{high} = \frac{C_{fb}}{-(I_{inj} - I_r)} V_{dd} \quad (1)$$

And the inter pulse duration t_{low} is given as,

$$t_{low} = \frac{C_{fb}}{I_{inj}} V_{dd} \quad (2)$$

III. CIRCUIT SIMULATION AND RESULT ANALYSIS

3.3. Simulations at 180nm MOSFET technology using Cadence Software toolset

3.3.1. Static Excitatory Synapse

The static excitatory synapse circuit shown in Fig. 2 has been implemented at 180nm technology and simulated in Cadence software at schematic as well as layout level. The parameter values in the circuit are kept below the threshold value of the MOSFETs ensuring subthreshold operation. The circuit simulation has been done for varying parameter values and their effect of on the output current I_d , which is same as the current through the resistor R0 i.e. $I(R0)$ in Fig. 4, has been studied and analysed. The schematic implementation and corresponding mask layout of the static excitatory synapse circuit implemented in 180nm technology in Cadence software is shown in Fig. 4(a) and Fig. 4(b) respectively. The Assura LVS for the static excitatory synapse circuit in Cadence software showed no errors. The circuit simulation outputs for varying values of synaptic weight $V_w (= 0.35V$ and $0.38V)$ keeping all other circuit parameters at constant values is shown in Fig. 5(a) and Fig. 5(b) at schematic and layout level respectively. The simulation outputs in Fig. 5 shows that the steady state values of the output current $I(R0)$ increase with the increased values of the synaptic weight V_w due to the increased gain of the circuit.

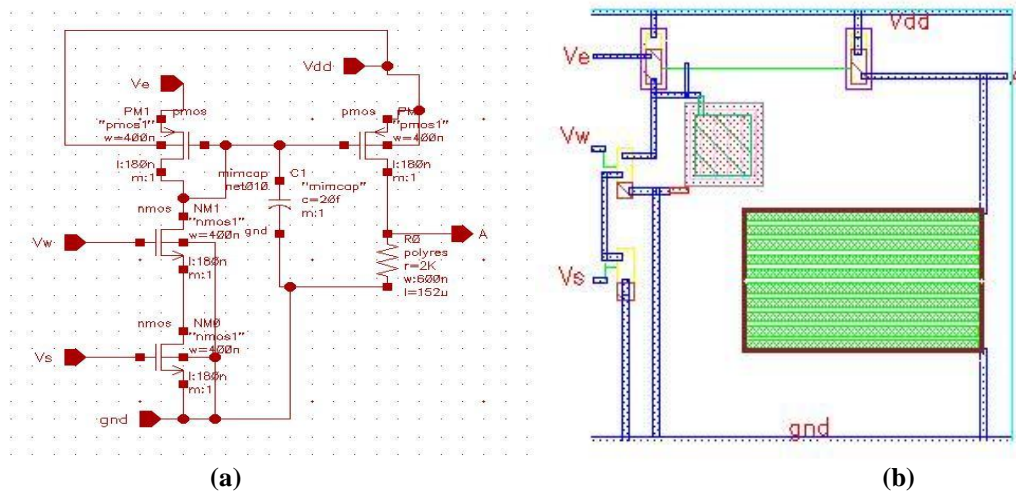


Figure 4. Static Excitatory Synapse Circuit Implementation

- a) Schematic
- b) Layout

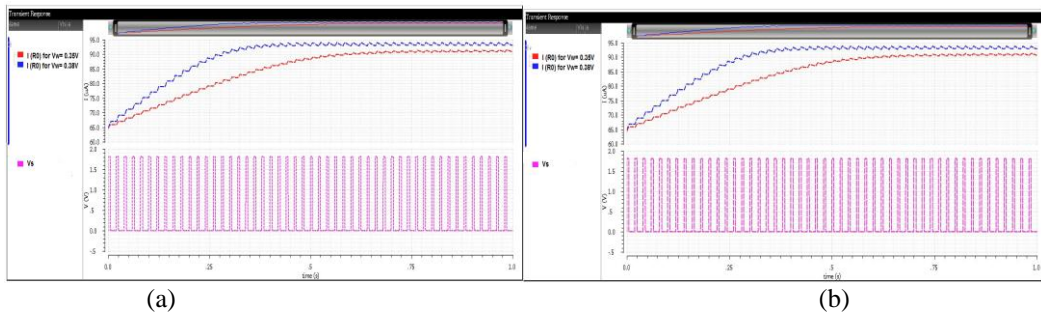


Figure 5. Static Excitatory Synapse Circuit Simulation Outputs - Effect of varying V_w on $I(R0)$ ($V_s = 50Hz$, $V_e = 700mV$)

- a) Schematic
- b) Layout

The circuit is simulated for varying frequencies of the presynaptic input voltage pulses V_s to study the effect of varying frequencies on the output current $I(R)$. Fig. 6(a) and Fig. 6(b) show the circuit response for change in the frequency of V_s ($=100\text{Hz}$ and 25Hz), with other circuit parameters at constant values, at schematic and layout levels respectively. The increased frequency of the input voltage spike pulse V_s leads to a higher steady state value of the output current $I(R)$ due to increased integration rate at higher frequencies which is clearly visible in the simulation outputs of Fig. 6(a) and Fig. 6(b).

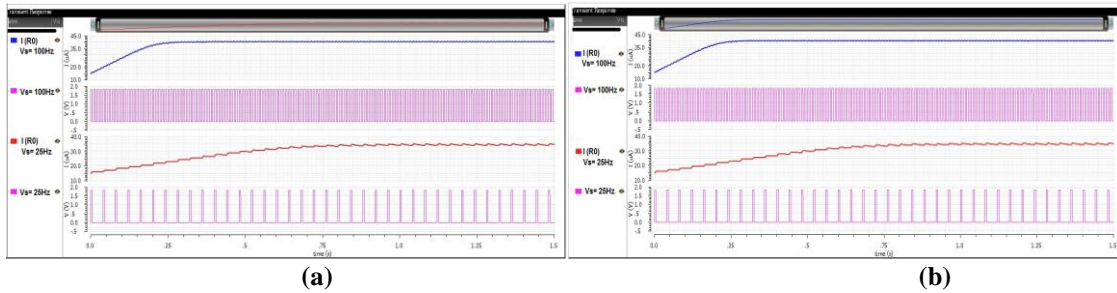


Figure 6. Static Excitatory Synapse Circuit Simulation Outputs - Effect of varying frequencies of V_s on $I(R)$ ($V_e=1200\text{mV}$, $V_w= 350\text{mV}$)

- a) Schematic
- b) Layout

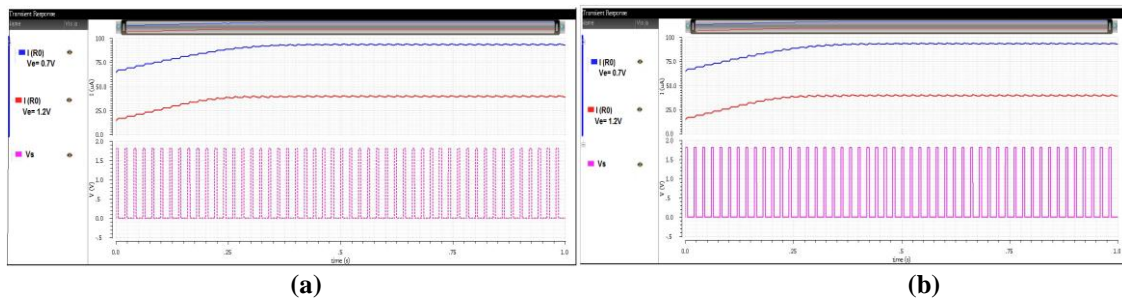


Figure 7. Static Excitatory Synapse Circuit Simulation Outputs - Effect of varying V_e on $I(R)$ ($V_s= 50\text{Hz}$, $V_w= 380\text{mV}$)

- a) Schematic
- b) Layout

Finally, the effect of changing bias voltage V_e is studied by simulating the circuit for varying values of V_e ($=0.7\text{V}$ and 1.2V) keeping all other circuit parameter values constant. Fig. 7(a) and Fig. 7(b) show the output response at schematic and layout level respectively. The simulation results demonstrate the increase in the gain of the circuit with decreased values of the bias voltage V_e .

3.3.2. Integrate and Fire Neuron

The Integrate and Fire Neuron circuit of Fig. 3 has been implemented at 180nm technology and simulated in Cadence software at schematic level as well as layout level. The aspect ratio of all the MOSFETs have been kept at a value of 2.22 and the selected capacitor values maintain a capacitive feedback $\frac{C_{fb}}{C_{mem} + C_{fb}}$ of 0.1 in the circuit. A supply voltage of 1.8V is used and all the parameter values are kept below the threshold voltage of the MOSFETs to ensure subthreshold operation of the circuit. The schematic circuit level diagram and corresponding mask layout diagram of the Integrate and Fire neuron circuit implemented in 180nm technology in Cadence software is shown in Fig. 8(a) and Fig. 8(b) respectively. The Assura LVS for the Integrate and fire neuron circuit in Cadence software showed no errors.

The circuit is simulated for different values of input injection current I_{inj} ($=4\text{nA}$ and 8nA) keeping all other circuit parameters at constant values. The corresponding membrane voltage V_{mem} and the output voltage V_{out} are shown in Fig. 9(a) and Fig. 9(b) at schematic and at layout level simulations respectively. The comparison of the output waveforms in Fig. 9(a) and Fig. 9(b) depict an increase in the frequency of the output voltage spike pulse, V_{out} , with the increased value of the dc input injection current I_{inj} as summarized in Table 1.

The increased input current I_{inj} leads to an increase in the rate of charging and discharging of the membrane capacitor C_{mem} thus decreasing the pulse width duration t_{high} and the inter pulse duration t_{low} of the output voltage spike pulse V_{out} . This results into an increase in the frequency of the output voltage spike V_{out} .

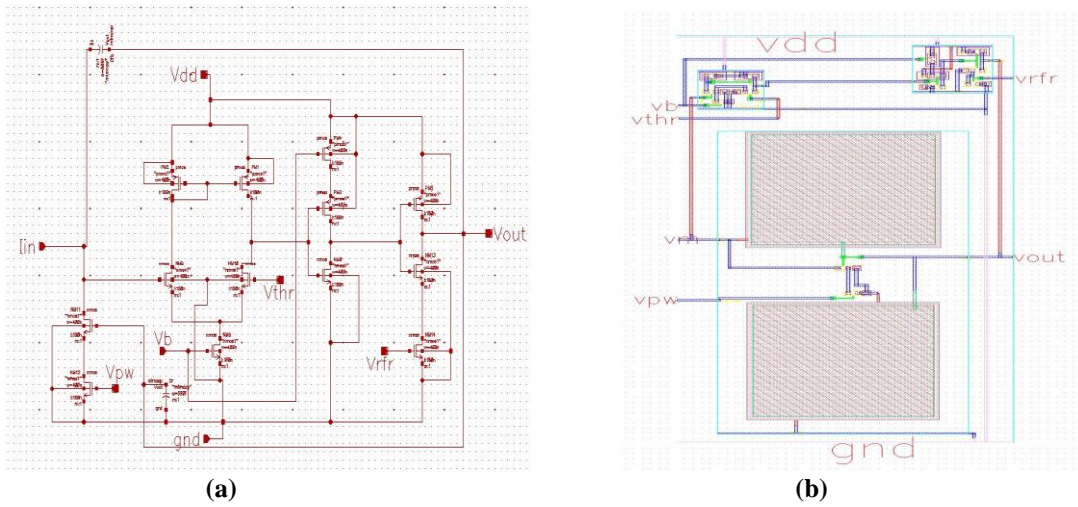


Figure 8. Integrate and Fire Neuron Circuit implementation

- a) Schematic
- b) Layout

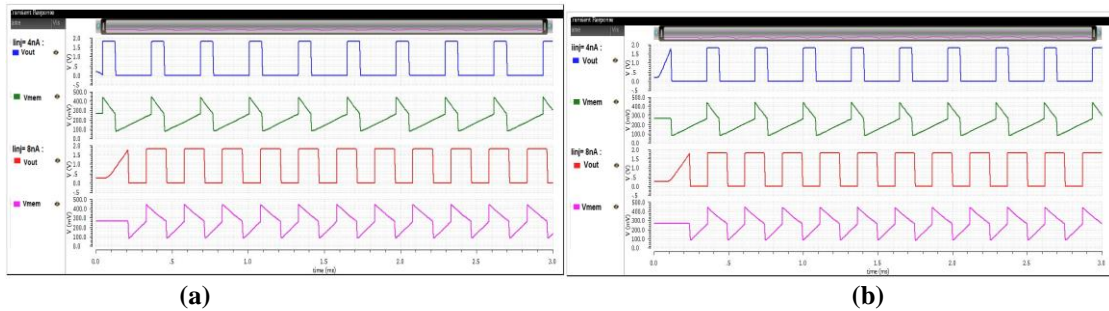


Figure 9. Integrate and Fire Neuron Circuit Simulation Outputs - Effect of varying I_{inj} on V_{out} ($V_b=290mV$, $V_{pw}=300mV$, $V_{thr}=300mV$, $V_{vfr}= 350mV$)

- a) Schematic
- b) Layout

Table 1. Effect of Varying I_{inj} on the Frequency of V_{out} ($V_b= 290mV$, $V_{pw}= 300mV$, $V_{thr}= 300mV$, $V_{vfr}= 350mV$)

S. No	Input Current I_{inj} (nA)	Simulation- level of abstraction	Pulse Width Duration t_H (μS)	Inter Pulse Duration t_{low} (μS)	Output Pulse Train Frequency (KHz)
1	4	Schematic	83	238	3.115
		Layout	83	240	3.095
2	8	Schematic	131	119	4.000
		Layout	131	120	3.984

The pulse width control voltage V_{pw} controls the width of the output voltage spike pulse V_{out} . This is demonstrated in the outputs shown in Fig.10(a) and Fig.10(b) for circuit simulation at schematic and layout levels respectively for varying values of V_{pw} ($=230mV$ and $250mV$) keeping rest of the parameter values constant. Its observed in that increase in the value of V_{pw} results into a decrease in the pulse width duration t_{high} as summarized in Table 2. The rate of discharge of the membrane capacitor C_{mem} and hence the discharge current I_r increase with the increase in the value of V_{pw} thus decreasing the high time t_{high} or the pulse width duration at the output. The inter pulse duration is dependent only upon the constant circuit parameters and the input current, which are constant in this case, hence t_{low} is constant.

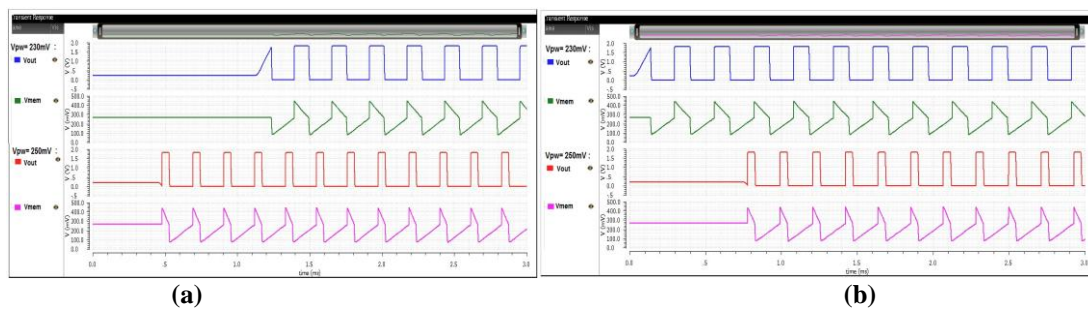


Figure 10. Integrate and Fire Neuron Circuit Simulation Outputs - Effect of varying V_{pw} on t_{high} of V_{out} ($I_{inj}= 6nA$, $V_b= 290mV$, $V_{thr}= 300mV$, $V_{rfr}= 350mV$)
 a) Schematic
 b) Layout

Table 2. Effect of Varying V_{pw} On V_{out} ($I_{inj}= 6nA$, $V_b= 290mV$, $V_{thr}= 300mV$, $V_{rfr}= 350mV$)

S. No.	Pulse Width Control Voltage V_{pw} (mV)	Pulse width duration of V_{out} t_{high} (μS)		Inter Pulse Duration t_{low} (μS)	
		Schematic level	Layout level	Schematic level	Layout level
1.	230	102.00	102.00	158.00	160.00
2.	250	41.81	48.00	165.45	167.00

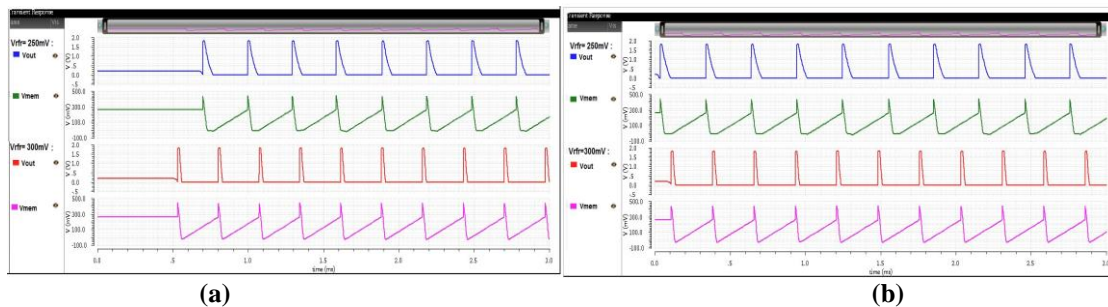


Figure 11. Integrate and Fire Neuron Circuit Simulation Outputs - Effect of varying V_{rfr} on V_{out} ($I_{inj}= 6nA$, $V_{pw}= 300mV$, $V_b= 290mV$, $V_{thr}= 300mV$)
 a) Schematic
 b) Layout

The refractory control voltage V_{rfr} is responsible to control the discharge of the output voltage spike pulse V_{out} when an action potential is generated and in this period the neuron circuit cannot generate another action potential at the output. Fig. 11(a) and Fig. 11(b) show the effect of varying values of V_{rfr} ($=250mV$ and $300mV$) on the output voltage spike pulse V_{out} with constant values of other parameters for simulations at circuit schematic and at layout level respectively. A comparison of the output pulses for varying values of V_{rfr} in Fig. 11(a) and Fig. 11(b) show that the increasing values of V_{rfr} increase the rate of discharge of the output voltage V_{out} resulting into a decrease in the refractory period of the neuron circuit.

3.3.3. Static Excitatory Synapse and Integrate & Fire Neuron Interconnection

The communication between the Static Excitatory Synapse Circuit and the Integrate and Fire Neuron circuit has been analysed by connecting the respective designed modules with adjusted parameter values. It is attempted to pass spike input voltage pulses of different frequencies from a presynaptic neuron, i.e. V_s , to a postsynaptic neuron via Static Excitatory Synapse. Fig. 12(a) and Fig. 12(b) respectively show the schematic and layout level connections of the static excitatory synapse module to the integrate and fire neuron module implemented in Cadence software at 180nm technology. The Assura LVS for the static excitatory synapse circuit integrated with Integrate and Fire neuron circuit in Cadence software showed no errors.

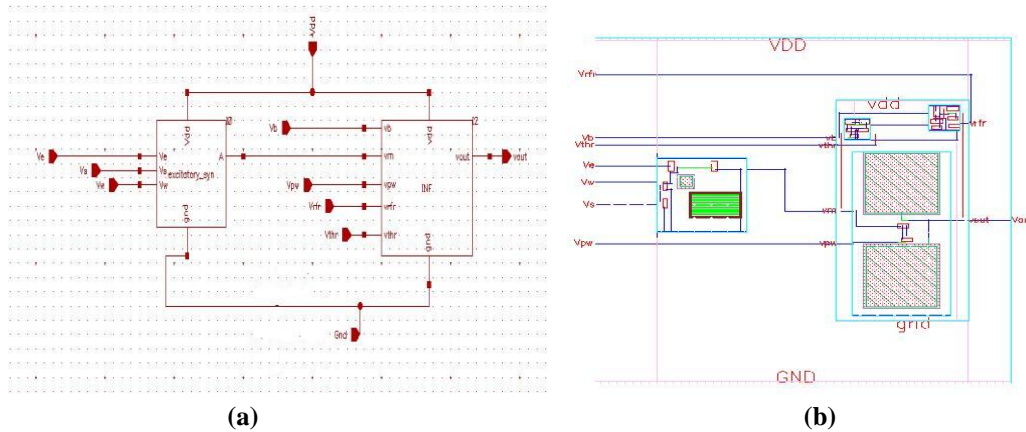


Figure 12. Connection of a Static Excitatory Synapse to an Integrate and Fire Neuron Circuit
 a) Schematic
 b) Layout

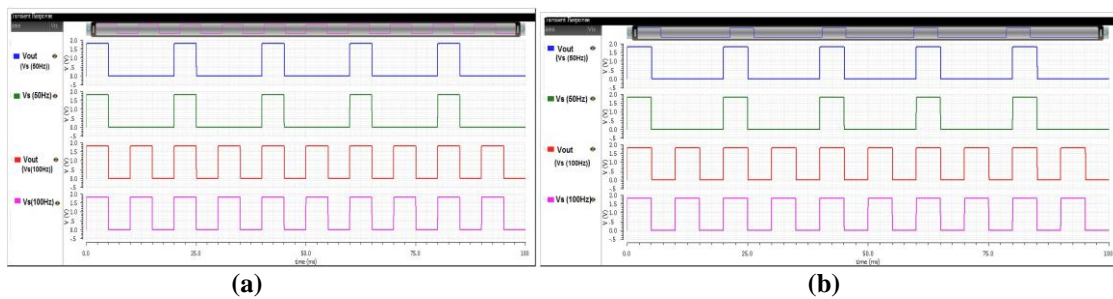
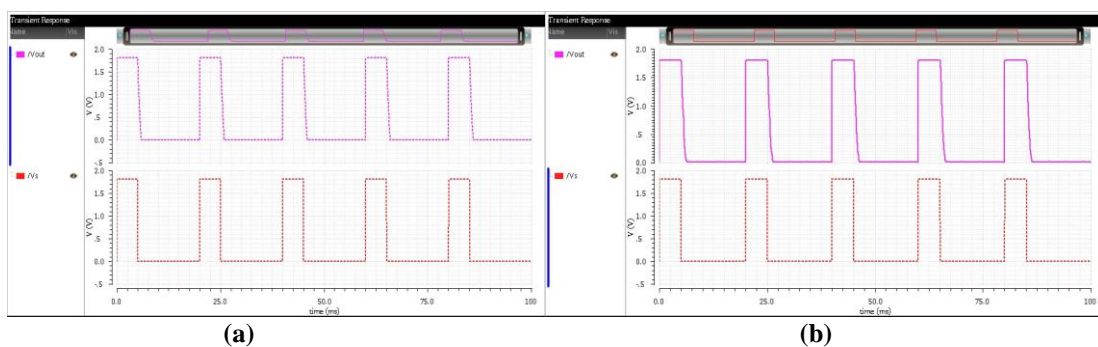


Figure 13. Connection of a Static Excitatory Synapse to an Integrate and Fire Neuron; Simulation outputs: V_s and V_{out} for frequencies of 50Hz and 100Hz ($V_e = 0.6V$, $V_w = -0.35V$, $V_{pw} = 0.38V$, $V_b = -0.29V$, $V_{thr} = 0.2V$, $V_{rfr} = 0.3V$)

- a) Schematic
- b) Layout

The schematic and the layout level simulation results of the static excitatory synapse circuit connected to the integrate and fire neuron circuit implemented in Cadence software at 180nm technology for adjusted component and parameter values is shown in Fig. 13(a) and Fig.13(b) respectively. The excitatory synapse circuit is provided with an input voltage spike pulse train V_s , synonymous to presynaptic input, to be passed to the postsynaptic neuron. As demonstrated in the circuit schematic and the layout simulations results, of Fig. 13(a) and Fig.13(b) respectively, the circuit successfully passes input voltage spike pulses of frequencies 50Hz and 100Hz.

Further to verify the functionality of the circuit, it is simulated both at the schematic and layout level for a decreased value of V_{rfr} ($= 0.15V$) in the Integrate and Fire Neuron Circuit. The simulation outputs of Fig.14(a) and Fig.14(b) respectively show the increase in the refractory period as expected both at Schematic and layout level simulation results.



(a) (b)

Figure 14. Connection of a Static Excitatory Synapse to an Integrate and Fire Neuron: Simulation Outputs for $V_{\text{ref}}=150\text{mV}$

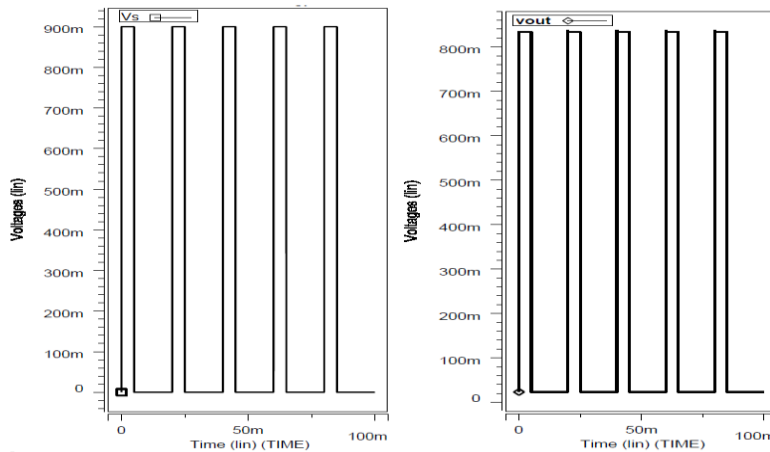
- a) Schematic
- b) Layout

3.4. Simulation in CNFET technology using HSPICE software tool

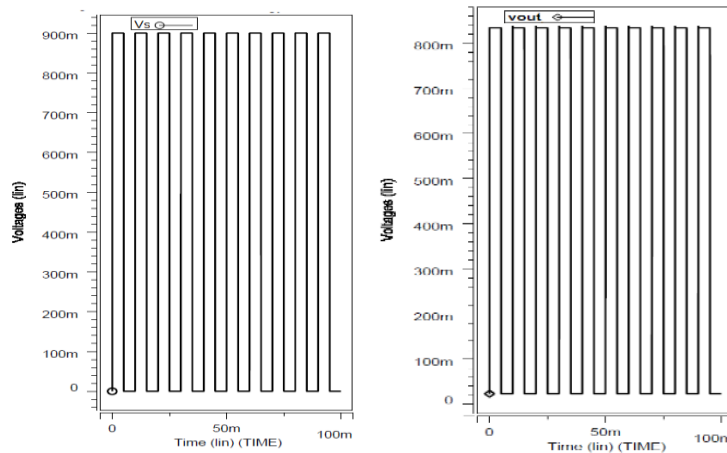
3.4.1. Static Excitatory Synapse and Integrate & Fire Neuron Interconnection:

The static excitatory synapse connection with an integrate and fire neuron circuit is implemented in CNFET technology. It utilizes the already reported circuit design of static excitatory synapse [18] and the integrate and fire neuron circuit [19] in CNFET technology. The circuit simulations are done in HSPICE software which is based upon the circuit compatible CNFET model proposed by Jie Deng [16, 17]. The CNFETs in the circuit are assumed to be containing a single walled semiconducting CNT with chirality (19, 0). The diameter of the CNT with chirality (19, 0) is 1.488nm and the threshold voltage of the CNFET is equal to 0.29V [20]. The component and parameter values in the circuit are adjusted as per the requirements of current and voltage levels needed to facilitate proper signal transmission. The parameter values are kept below the threshold voltage of the CNFETs (i.e. 0.29V) to ensure subthreshold operation and the circuit operates at a supply voltage of 0.9V. This results into a very low power consumption in the circuit.

The synapse circuit is provided with an input voltage spike pulse train, V_s , of frequency 50Hz. It generates the post synaptic current output which is fed to the Integrate and fire neuron circuit as the input injection current I_{inj} . The capacitor values in the neuron circuit are adjusted to provide the capacitive feedback fraction $\frac{C_{\text{fb}}}{C_{\text{mem}} + C_{\text{fb}}}$ of 0.1 in the neuron circuit. The parameter values are adjusted in the neuron and the excitatory synapse circuits when integrated together to facilitate generation of an output pulse V_{out} like the per-synaptic input spike pulse V_s applied at the input of synapse circuit. Fig.15(a) and Fig. 15(b) show the simulation output of the circuit for the input spike pulses of frequencies of 50Hz and 100Hz applied to the input of the synapse circuit respectively.



(a)



(b)

Figure 15 Connection of a Static Excitatory Synapse to an Integrate and Fire Neuron: Schematic Simulation Outputs in HSPICE software

- (a) V_s and V_{out} for frequencies of 50Hz ($V_e = 0.45V$, $V_w = -0.28V$, $V_{pw} = -0.11V$, $V_b = 0.046V$, $V_{thr} = V_{rfr} = 0.1V$)
- (b) V_s and V_{out} for frequencies of 100Hz ($V_e = 0.45V$, $V_w = -0.28V$, $V_{pw} = -0.11V$, $V_b = 0.046V$, $V_{thr} = V_{rfr} = 0.1V$)

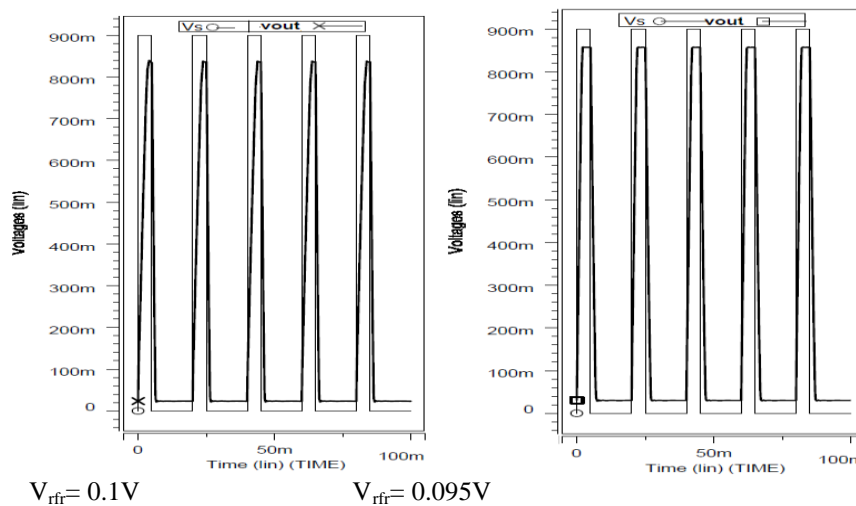


Figure 16 Connection of a Static Excitatory Synapse to an Integrate and Fire Neuron: Schematic Simulation Outputs in HSPICE software- V_s and V_{out} for frequencies of 50Hz for varying V_{rfr} (With higher capacitor values in neuron circuit and $V_e = 0.45V$, $V_w = -0.28V$, $V_{pw} = -0.11V$, $V_b = 0.046V$, $V_{thr} = 0.1V$)

The circuit is then simulated with the same parameter values and an input voltage spike pulse of frequency 50Hz as in the previous case but with capacitor values in the neuron circuit 10^3 times higher than the previous case. A capacitive feedback fraction of 0.1 is ensured in the Integrate and Fire Neuron circuit. The simulation results are shown in Fig. 16. A comparison of the output voltages V_{out} in Fig. 15(a), Fig. 15(b) and Fig. 16 show decreased rate of charging and discharging at the output which is because of the increased capacitor values in the neuron circuit. The results thus show the effect of changed component values on the output of the circuit. Further, the effect of changing values of V_{rfr} ($= 0.1V$ and $0.095V$) on the output voltage V_{out} is studied as shown in input and output waveforms of Fig. 16. It shows that the rate of discharge of the discharge capacitor C_r and hence the output voltage V_{out} decreases for smaller value of the voltage V_{rfr} leading to an increase in the refractory period.

The simulation results therefore show successful passage of presynaptic input pulse V_s through the excitatory static synapse circuit to the postsynaptic neuron as the output V_{out} of the neuron circuit in 180nm MOSFET as well as CNFET technology. Table 3 shows a comparison of the average power consumption in the excitatory synapse circuit, integrate and fire neuron circuit and the circuit interconnecting an excitatory synapse circuit to an integrate and fire neuron circuit in 180nm MOSFET and CNFET technology. The power consumed in all the circuit simulations is in the order of μW but the average power consumption in CNFET based circuit simulations is two orders of magnitude smaller than that in 180nm MOSFET circuits as shown in Table 3. The results therefore reflect the feasibility of implementing neuromorphic networks in CNFET technology and achieving a comparable performance with added advantages of CNFET technology in terms of power consumption and area occupancy.

Table 3. Average Power Consumption

Circuit Implementations	Average Power Consumption (μW)	
	180nm MOSFET Technology	CNFET Technology
Excitatory Synapse Circuit ($V_s = 50Hz$)	26.74	1.76 [18]
Integrate and Fire Neuron Circuit ($I_{inj} = 4nA$)	30.50	0.069 [19]
Excitatory Synapse and Integrate and Fire Neuron interconnection ($V_s = 50Hz$)	177.30	2.75

IV. CONCLUSION

The innovative field of Neuromorphic Engineering, pioneered by Carver Mead in late 1980s, deals with the design and implementation of dense hardware networks based on the operational and organizational principles of biological networks in mammalian brain. The Neuromorphic networks attempt to achieve area and power budget of biological networks by integrating area efficient analog VLSI neuron and synapse circuits. The devices in these circuits work in subthreshold regime, where the current levels are very low, ensuring very low power consumption in these circuits. It is possible to achieve real time as well as accelerated time operation of these networks. The compact and dense low power neuromorphic systems working in real time find their applications in implants and prosthetics.

The area and power efficiencies of these circuits have been constantly improved with the implementation of the circuits at advanced CMOS technology node. In this work, the integrate and fire neuron circuit and the static excitatory synapse circuit, already reported in literature, are ported to 180nm technology, and simulated using Cadence software tool set. The simulation output response for varying parameter values in the circuits verify the functionality of the circuits. The static excitatory synapse is then connected to an integrate and fire neuron circuit to demonstrate the passage of signal from a presynaptic neuron to a postsynaptic neuron through a static synapse. The simulation results show that a voltage spike pulse train provided as the presynaptic pulse at the input of the static excitatory synapse circuit is successfully passed to the output of the integrate and fire neuron circuit. The outputs also show that any circuit parameter variation is reflected at the output of the integrate and fire neuron circuit.

As the CMOS technology is approaching its final scaling limits and there is a quest for finding a replacement of MOSFETs in the VLSI circuits. CNFET is one of the potential devices which offers structural as well as operational advantages over the limitations in MOSFETs. In this work the CNFET based Static excitatory synapse circuit and the Integrate and fire Neuron circuit, already reported in literature, are connected with adjusted component and parameter values. The circuits are implemented and simulated in CNFET technology using HSPICE software. The simulation outputs demonstrate successful transmission of signal via a static excitatory synapse to the postsynaptic neuron. The power consumption in the circuit implemented in CNFET technology is two orders of magnitude smaller as compare to that required in 180nm MOSFET technology. Further the area occupancy of the circuits in CNFET technology would be less as compared to MOSFET technology owing to smaller footprints of CNFETs. The advantage of area and power efficacy of circuits in CNFET technology can be tapped in implementation of large scale dense real time neuromorphic networks of volumes comparable to biological networks in future.

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