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A Novel Energy Efficient Multiplier Using OTFC

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Abstract : *An Energy Efficient Multiplier Is Proposed And Implemented With Less Area, Minimum Delay, And Less Amount Of Power Dissipation. The Left To Right Truncated Multiplier Was Proposed Earlier. In That Design, N-Bit Multiplier Produces 2N Bit Partial Products, But These 2N Bit Partial Products Will Be Divided Into 2N-(N/2) Bits And N/2 Bits. Thus Finally 2N Bits Are Produced By Addition Of Above Bits Using Ripple Carry Adder. The Proposed Multiplier Was Implemented Without Any Truncation And Addition Method, And Designed As A General Array Multiplier Structure. A Smaller On-The-Fly Conversion (OTFC) Circuit Is Added At The End Of The Circuit. The Proposed Converter Produces The Most Significant Part Of Final Partial Product. The OTFC Logic Is Used To Speed Up The Carry-Propagate At The Last Stage Of Multiplication. The Delay Is Independent Of The No. Of Input Bits. Several Left To Right And Right To Left Multipliers Designed Earlier For 8bit, 16bit, And 32 Bits Were Compared With The Proposed Multiplier With Respect To Power, Delay, Area And Energy In 45nm Technology. It Results In Low Power, Minimum Delay, Smaller Area And Less Energy.*

Keywords *- Addition, On-The-Fly Conversion, Left-To-Right Multiplier, Right-To-Left Multiplier, Truncation*

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I. Introduction

Multipliers Play An Important Role In High Performance Systems Such As Microprocessors, DSP And Other Applications. Addition And Multiplication Of Two Binary Numbers Are Fundamental And Most Often Used Arithmetic Operations. Statistics Shows That More Than 70% Instructions In Microprocessors And Most Of DSP Algorithms Perform Addition And Multiplication. So These Operations Dominate The Execution Time. Due To This, There Is Need Of A High Speed Multiplier. The Demand Of High Speed Processing Has Been Increasing As A Result Of Expanding Computer And Signal Processing Applications.

Low Power Consumption Is Also An Important Issue In Multiplier Design. To Reduce Significant Power Consumption It Is Good To Reduce The Number Of Operations, Thereby Reducing Dynamic Power Which Is A Major Part Of Total Power Consumption. To Meet These Issues, Need Of High Speed And Low Power Multiplier Is A Necessity. The Efficiency And Accuracy Of Any System Depends On The Robustness Of The Critical Component, Which Is A Multiplier In Most Of These Kinds Of Applications.

Full Or Direct Multiplier Implementations Of N*N Bit Multiplication Yields A 2N Bit Product. In Order To Keep The Full Accuracy Of The System, DSP Architecture Would Need An Ever Growing Bit Width That Would Be Impossible Or Impractical To Implement. Usually Truncated Multiplier Was Implemented To Keep Results Within The Limits Of The Architecture Bit Width [2]. Some Columns And Rows In The Multiplier Array Can Be Turned Off Whenever Their Outputs Are Known. In Most Of The Applications 'N' Most Significant Bits Are Used For The Product. The Truncated Multiplier Implements 'N+K' Most Significant Columns Instead Of 2n. Truncated Multiplier Uses Error Correction Which Can Be Analyzed And Reduced By Various Correction Methods. In Many DSP Applications, A Truncation Error Less Than Ulp/2 Is Acceptable, Where $Ulp=2^{-N}$ Is The Weight Of The Least Significant Bit [2]. The Truncation Block Was Added To The Main Block Of The Multiplier Using Ripple Carry Adder To Overcome The Truncation Error While Performing The Addition Operation. The Main Block And Truncation Block Together Produces The Final Adder Results. The Drawbacks Of The Energy-Efficient Multiplier With Fully Overlapped Partial Products Reduction And Final Addition Is Used In Some Limited Applications. These Designs With Acceptable Error Can Be Used In MAC Unit, ALU And Image Processing Applications. In All These Applications, The Truncated Part Should Be Added To The Fully Overlapped Partial Products With A Ripple Carry Adder [3]. But Here Delay Plays A Lead Role In The Processing Of Final Addition. To Overcome This Problem, Fully Precision Multiplier With OTFC Has Been Implemented And This Approach Is Advantageously Used For Multiplication.

In This Paper, Full Precision Multipliers (8, 16, And 32 Bits) Have Been Implemented And Comparison Of Their Characteristics Is Done. The Designs Are Initially Compared By Using Analytical Models Based On Gate Delay And Size. Then The Designs Are Synthesized, Evaluated Based On The Parameters, Like Latency, Area, And Power. The RTL Compiler Is Used To Perform Logic Synthesis By Using The CMOS 45nm Technology. Encounter Tool Is Used For Physical Design Of Proposed Multiplier.

The Main Contributions Of This Work Are:

1) The Proposed Multiplier Has Lower Delay Area, Power And Energy (Power-Delay Product) As Compared With Other Multipliers.
2) The On-The-Fly Conversion Logic Is Used To Speed Up The Carry Propagate Addition At The Last Stage Of Multiplication And Provides Constant Delay Independent Of No. Of Input Bits [4].
3) An Analytical Delay And Size Of Our Multiplier Design Compared To Existing Designs Are Presented [5].

In Section II, The Energy Efficient Multiplier With Fully Overlapped Partial Products Reduction And Final Addition (Truncated Multiplication) Is Explained. An Understanding Of The Existing Multipliers Is Given In Section III. The Implementation Of The Proposed Multiplier Is Presented In Section IV, And Finally The Synthesized Results Analysis Is Presented In Section V And Conclusion In Section VI.

II. Truncated Multiplication

Consider The Multiplier Of Two Unsigned N-Bit Numbers, Where A= $A_{n-1},A_{n-2,\ldots}A_0$ Is The Multiplicand And B= $B_{n-1},B_{n-2,}\ldots..B_0$ Is The Multiplier. The Product P= $P_{2n-1},P_{2n-2\ldots.}P_0$ Can Be Written As Follows. [6]

$P=\sum_{(I=0,\ N-1)} \sum_{(J=O,N-1)} (A_i,B_j)\ 2^{i+J}$

An Example Of An Unsigned 8*8 Multiplication Is Shown In The Fig.2.1 Below.

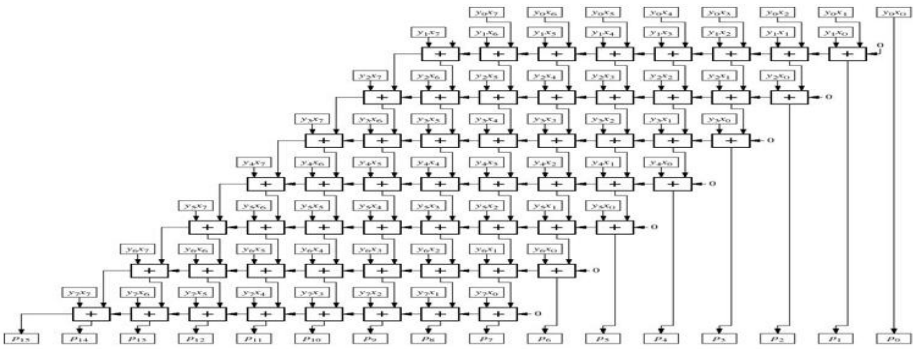

Fig.2.1: Basic Structure Of An Array Multiplier

To Achieve The High Speed Data Processing, Parallel Computing Process Is Proposed. This Parallel Processing Technique Is Implemented As A Systolic Multiplier For High Speed Data Processing.

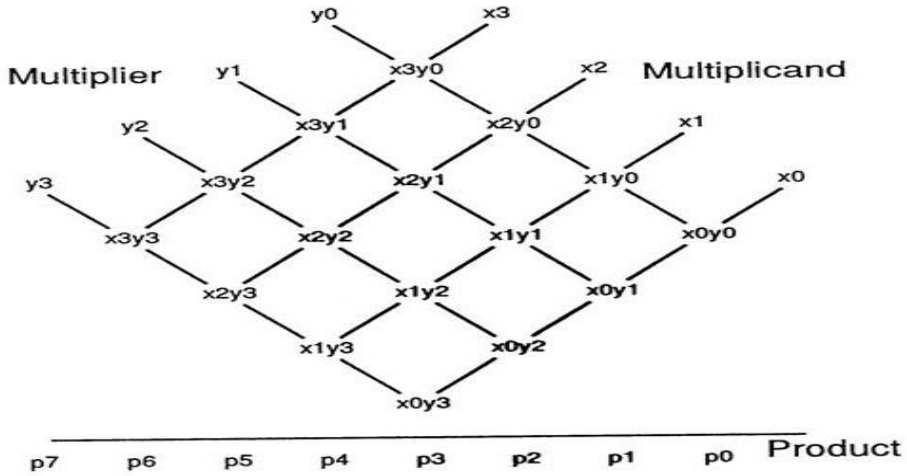

Fig.2.2: Systolic Structure Of An Array Multiplier

FIR Filter Designers Are Presented Using The Concept Of Faithfully Rounded Truncated Multiplier. This Multiplier Design Is Usually Considered, Where The Maximum Absolute Error Is No More Than 1 **Ulp**

(**Unit Of Least Position**), And Also Time Truncated Multipliers Offer Significant Improvement In Area, Delay, Power.

Multiplication Of Two No's Generates A Product With Twice The Original Bit Width. It Is Usually Desirable To Truncate The Product Bits To The Required Precision To Reduce Area And Cost Leading To The Design Of Truncated Multipliers, Which Compute Only 'N' **M**ost **S**ignificant **B**its (MSB) Of The 2n-Bit Product For N*N Multiplication And Use Extra Correction Circuits To Reduce Truncation Errors [2]. There Are In General Two Truncated Multiplier Design Methods Namely Constant And Variable Correction Depending On How To Compensate The Error Introduced Due To Simulation Of The Least Significant Partial Product Bits.

In Some Applications Like The Design Of FIR Filter In DSP, There Is A Need Of Truncated Multipliers With Accuracy Of Faithful Rounding Which Means That The Maximum Absolute Error After Truncation Is Less Than 1 **Ulp.**

III. Existing Multiplier

The Structure Of The Majority Truncated Multiplication Schemes Of Two N Bit Numbers Produces A 2n Bit Output Y. The Truncation Of The Multiplier Is Performed By Removing The Value Contained In The LSP (Least Significant Position) Minor Columns. [8] A Hardware Efficient Function Of The Two Inputs (A & B) Is Then Introduced As Compensation Into Column 'K' (LSP Minor) [7]. Once The Resultant Carry Is Summed, A Further N/2 (Or) LSP Minor Columns Are Truncated, The Result Is Then The Approximation To The Multiplication [7]. The Structure Of The General Multiplier Truncation Scheme Is Shown In Fig.3.1.

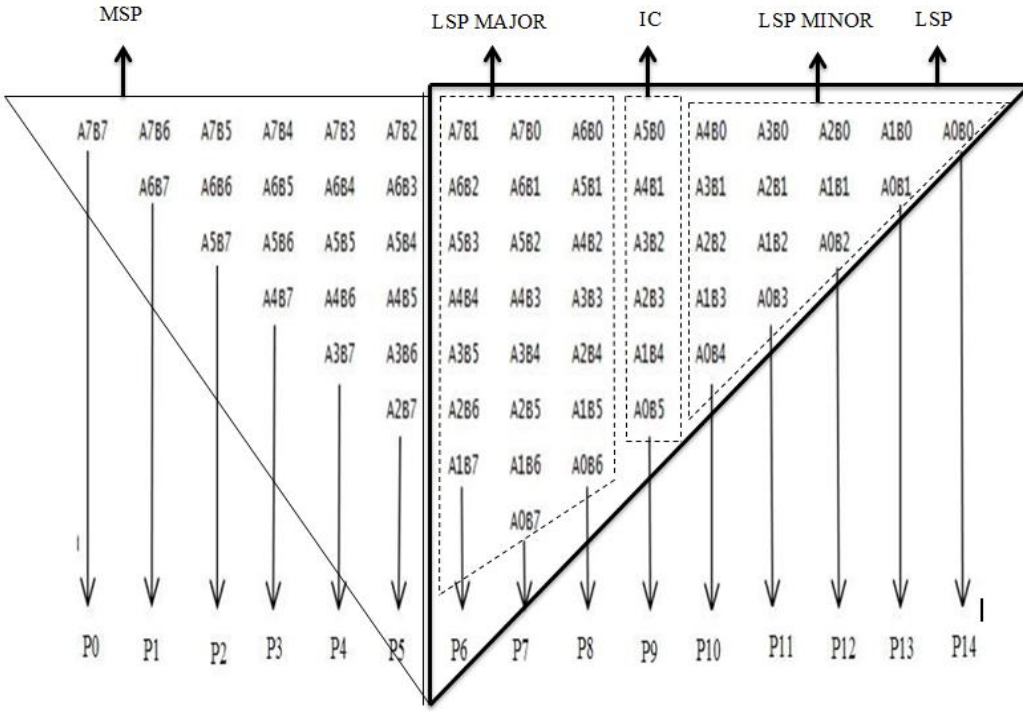

Fig.3.1: Truncated Multiplier

It Is Used To Reduce The First N+K Columns Of The Partial Product Array, The Value Of K, Which Is Less Than N Is Determined By The Allowed Truncation/Rounding Error In The Final Product. In Left To Right Multiplier AND Gates And Full Adders Are Used For Multiplication. In Normal Right To Left Multiplier AND Gates And FULL ADDERS Are Used For Multiplication. But At End Of The Multiplication Stage We Will Use The N-Bit Final Adder With The Help Of Full Adders To Produce The Most Significant Partial Products In 2n Bits. In Left To Right Multiplier, It Avoids The Final Adder By Using On-The–Fly Conversion (OTFC) Circuit [9]. The OTFC Circuit Can Be Performed In Parallel With Array Reduction.

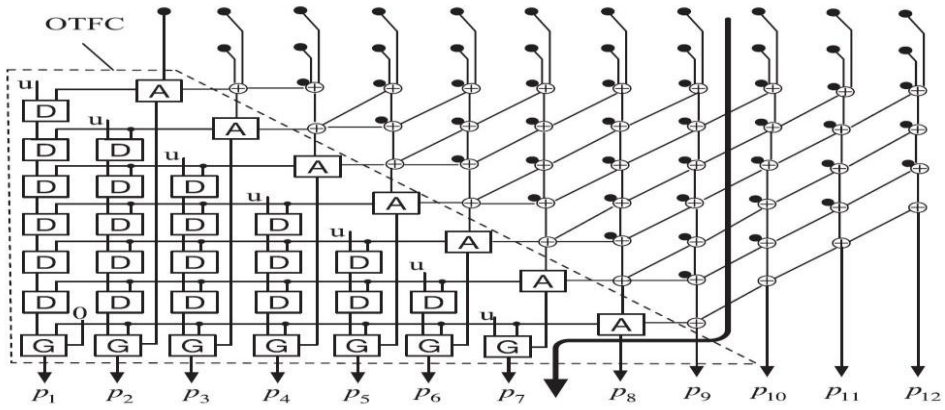

Fig.3.2: Single Precision Existing Multiplier

Figure 3.2 Shows Left To Right Truncated Multiplier[1]. In Each And Every Stage Of AND Gates, Which Produces The Products And Then The Full Adder Produces The Sum And Carry During The Partial Products Reduction Process. The Left Module In The Last Stage Of Multiplication In The Dashed Line Box Is The On-The-Fly Conversion Circuit. A-Cell Is Used For Addition Of The Inputs A,B And Producing Sum Digit $Z_{i,0}$ And Carry Digit $Z_{i,1}$ [10].

A-Cell Produces

$$Z_{i,0}=A \oplus B.$$

$$Z_{i,1}=A.B \quad \text{——————} \quad (1)$$

D-Cell Determines Whether To Propagate The Carries From The Lower Bit Position. Set Dp_i To Be The Propagate Signal And Dg_i To Be The Generate Signal. Here 'I' Is The Stage Index Of Array Reduction. The Carry-In Is Propagated When D_p= 1 And Is Stopped When $D_{pi}=D_{gi}=0$.

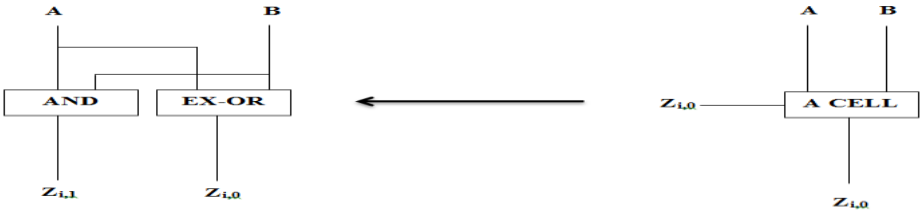

Fig.3.3: A Cell

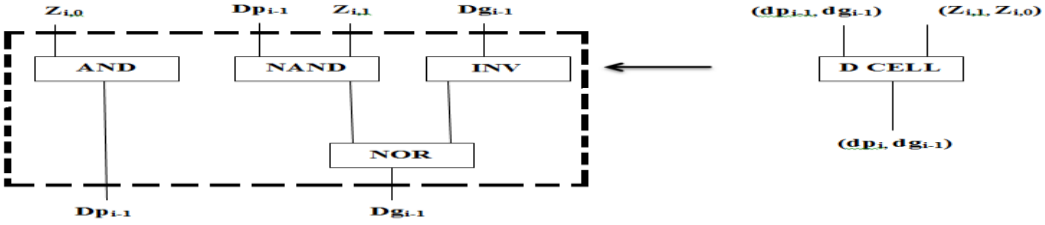

Fig.3.4: D Cell

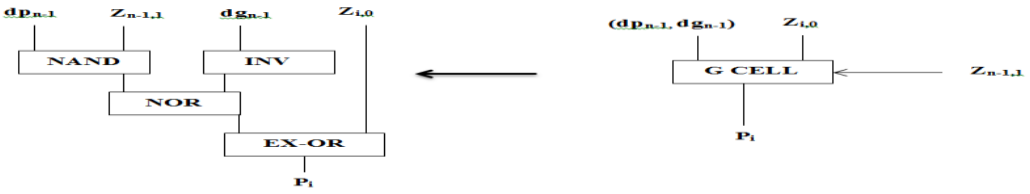

Fig.3.5: G Cell

The D-Cell Generates The Carry-Out When D_{gi}=1. There Are Two Input Pairs, One Is The Output From A-Cell ($Z_{i,0}$, $Z_{i,1}$) And The Other Is Output From The Previous D-Cell (D_{pi-1} ,D_{gi-1}). The Initial Value Of

(D_{p0}, D_{g0}) Is (1,0) Which Means The Carry Produced From The Array Is Propagated To The OTFC Converter And The Value Is Undecided (Represented 'U' In Fig) The Expansion Of D-Cell Are

$$D_{pi}=D_{pi}.Z_{i,0}$$
$$D_{gi}=\overline{D_{pi-1}.Z_{i,1}} + D_{gi-1} \quad \text{——————} \quad (2)$$

The Expression For The Outputs Of D-Cell Are Realized By Using The Propagate And Generate Signals. After $(N-1)^{Th}$ Stage, D_{pn-1} And D_{gn-1} Are Generated From The Last Rows Of D-Cells. The Most Significant Part Of The Final Product P_i (I=1, 2, 3,N-1) Is Obtained Using G-Cells.

$$P_i= Z_{i,0} \quad (D_{pn-1}.Z_{n-1} + D_{gn-1}) \quad \text{——————} \quad (3)$$

A-Cell Implements Eq.1, D-Cell Implements Eq.2 And G-Cell Implements Eq.3 To Produce The Final Product Bits. The N-Bit Multiplier Consists Of (N-1) A-Cells, $(N^2-3n+2)/2$ D-Cells And (N-1) G-Cells [11]. The Proposed Array Multiplier Is Explained In Section IV Which Focuses On Reducing The Size Of The On-The-Fly-Conversion.

IV. Proposed MULTIPLIER

In The Proposed Array Multiplier, All The Partial Products Along With The Final Products Are Considered, Since Many Applications Need A Full Result Of Multiplication, Instead Of A Truncated Result. The Challenge Is To Create The Most Effective Tradeoff Between Speed, Area And Power. As Discussed Earlier, The OTFC Is Used To Speed Up The Carry Propagate Addition And Provides Constant Delay Independent Of No.Of Input Bits. The Modified On-The-Fly-Converter Was Applied In Our Proposed Array Multiplier.

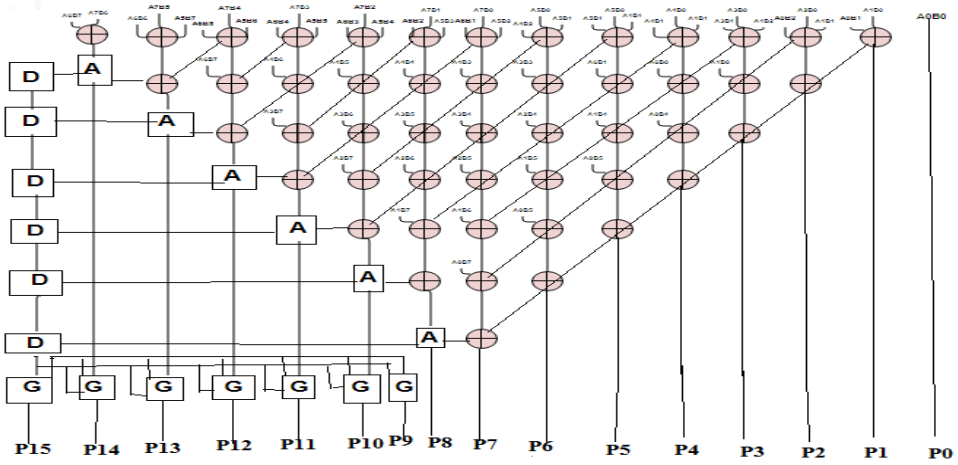

Fig.4.1: Proposed Multiplier

Fig.4.1 Illustrates The Block Diagram Of The N-Bit Multiplier. The AND Gates (Products) At Every Stage, Are Routed Through Circles, With A + Mark Representing The Full Adder Producing The Sum And Carry Of Each Stage. The Carry Of Adders Is Forwarded To The Next Stage Until The End Of The Multiplication Process. Towards The End Of The Multiplication Process, OTFC Is Connected. The Final Partial Products Of Most Significant Bits Are Produced By The OTFC. In The OTFC Circuit, A-Cell Is Used For Addition Of The Inputs A,B Which Produces Sum ($Z_{i,0}$) And Carry ($Z_{i,1}$).

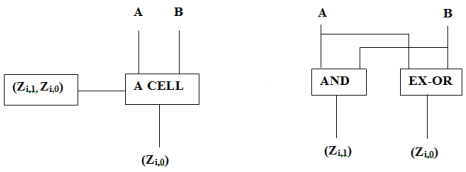

Fig.4.2: Proposed A-Cell

Where $Z_{i,0}= A \oplus B$

$Z_{i,1}=A.B$

D-Cell Represents The Carry Propagation; The Carry From The Lower Bit Position Sets The D_{pi} To Propagate The Signal And D_{gi} To Generate The Signal. The Carry Is Propagated When $D_p=1$ And Is Stopped When $D_{pi}=D_{gi}=0$. The D-Cell Generates The Carry-Out When $Dg_i=1$

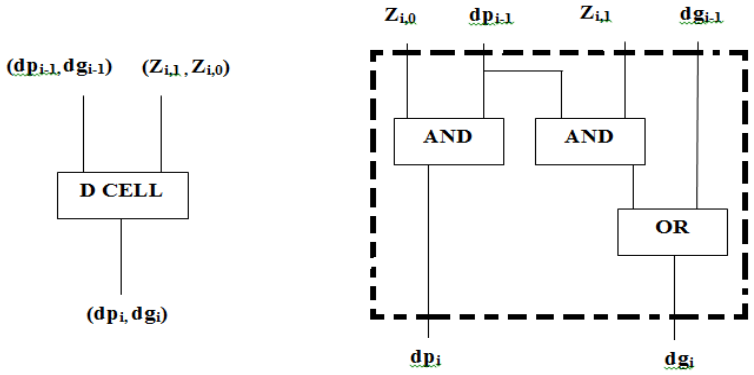

Fig.4.3: Proposed D-Cell

Where $D_{pi} = D_{pi-1}.Z_{i,0}$

$D_{gi} = D_{gi-1}+D_{pi-1}.Z_{i,1}$

Every Stage D-Cells Produces The Outputs Which Are Given To The Next Stage D-Cell Inputs. The Final $(N-1)^{Th}$ Stage D-Cell Output Is Given To The G-Cell Inputs.

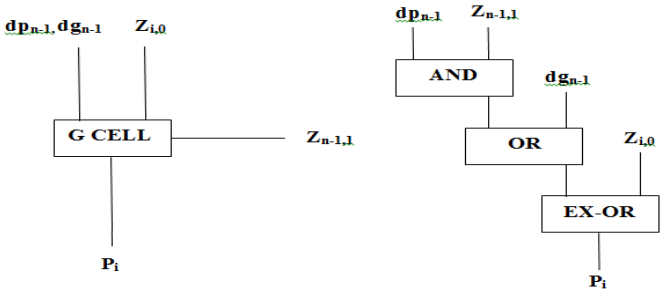

Fig.4.4: Proposed G-Cell

The G-Cell Produces The Final Partial Product Of OTFC.

$P_i = Z_{i,0} \quad (D_{pn-1}.Z_{n-1,1}+D_{gn-1})$.

V. Synthesis Results

We Implemented The Energy Efficient Multiplier Using Cadence 45nm Technology. All Considered Multipliers Are Implemented In The Same Platform For Comparison. The Synthesized Results Of Delay, Area And Power For 8-Bit, 16-Bit And 32-Bit Are Shown In Table No. 1, 2 And 3. The Energy Is Obtained By The Product Of Power And Delay.

Table I Comparison Of Different Multiplier Parameters For 8-Bit

PARAMETER	GATE COUNT	AREA (um^2)	POWER (mW)	DELAY (ns)	ENERGY (pJ)
PROPOSED	255	1222	1.825	21.842	39.861
LRCF	287	1479	1.930	25.938	50.060
VEDIC	317	1603	1.859	22.221	41.3088
WALLACE	337	1402	1.996	24.770	49.440
ARRAY	361	1827	2.091	25.497	53.3142

Table II Comparison Of Different Multiplier Parameters For 16-Bit

PARAMETER	GATE COUNT	AREA (Um^2)	POWER (Mw)	DELAY (Ns)	ENERGY (Pj)
PROPOSED	1226	5831	5.184	22.491	116.593
LRCF	1505	7391	5.863	25.626	150.245
VEDIC	1462	7332	5.300	22.512	119.313
WALLACE	1576	6505	6.119	25.522	156.169

ARRAY	1608	8081	6.326	26.151	173.433

Table III Comparison Of Different Multiplier Parameters For 32-Bit

PARAMETER	GATE COUNT	AREA (um^2)	POWER (mW)	DELAY (ns)	ENERGY (pJ)
PROPOSED	5503	25881	11.193	22.640	253.409
VEDIC	6348	31311	12.010	22.702	272.651
WALLACE	6933	28728	14.309	25.320	369.458
ARRAY	7109	34449	15.741	26.322	414.334
LRCF	6414	31141	19.898	25.787	513.109

Our Proposed Multiplier Was Implemented With Low Power, Less Delay, Small Area And Lower Energy. The Physical Design Is Also Done For The Multiplier By Using Encounter Tool.

PD Is A Chip Design Process Which Is Followed By Standard Cells Placement, Floor Plan, Power Plan, Timing And Optimization Of Routing Clock Synthesis Steps. In Rtl Verification When We Achieve All Our Specifications Then We Will Get Desired Converted Net List. That Net List Is Given To PD Encounter Tool As A Input. Adjust The PR Boundary And Perform The Floor Plan With Core Utilization. Create The H-Rails For Power Supply By Using Power Planning. Place The Standard Cells After Adding The Rings And Strips. Placing Of The Standard Cells Is Done By Placement Method.

Verify The Connectivity For Routing. Perform The Clock Tree Synthesis For Timing Analysis. If The Specifications Are Met, Move On To The Next Step Or Else Again Perform The Optimization To Achieve The Timing.

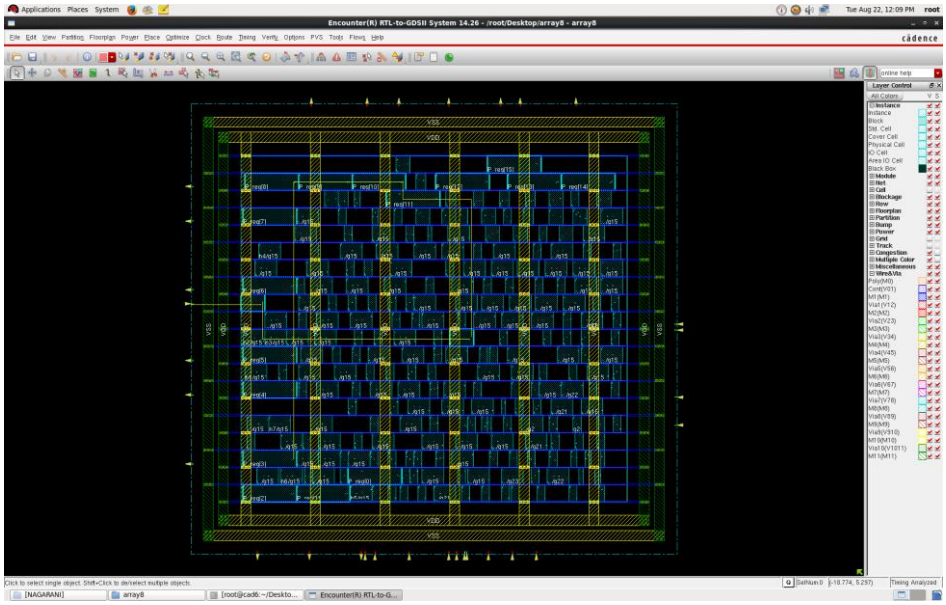

Fig.5.1: Physical Design With Clocking Of Proposed Multiplier

After Completion Of Timing Analyses, Perform The Routing And Verify The Connectivity For Routing Connections. Place The Physical Cells By Adding Fillers To Fill The Free Space In IC Chip. After Checking Has Been Performed Place All The Cells Into The IC By Using Placement Technique. Then Save The Design Net List LEF File And DEF File. The Total **PHYSICAL DESIGN** Process Is As Shown In The Figure Below.

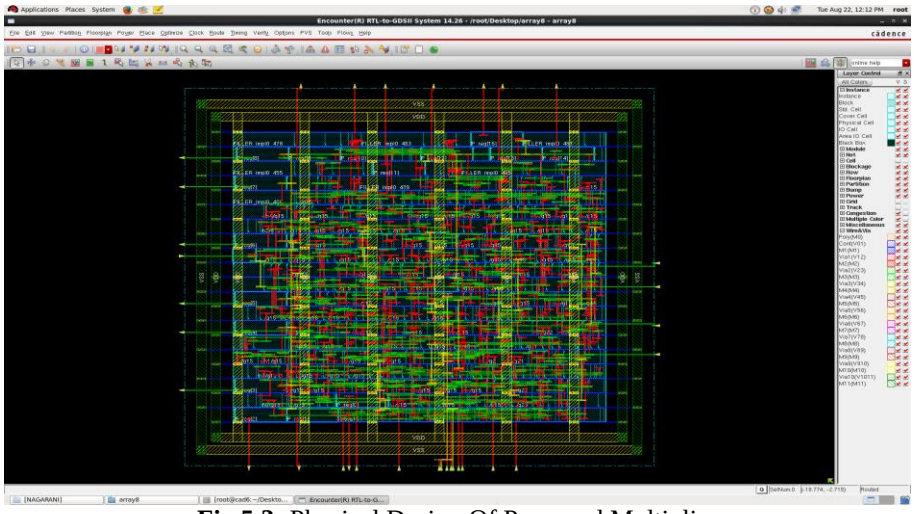

Fig.5.3: Physical Design Of Proposed Multiplier

VI. Conclusion

The Proposed Multiplier Has Lower Delay, Area, Power And Energy (Power-Delay Product) As Compared With Other Existing Multipliers. The On-The-Fly Conversion Logic Is Used To Speed Up The Carry Propagate Addition At The Last Stage Of Multiplication And Provides Constant Delay Independent Of No.Of Input Bits. This Project Can Also Be Done In Advanced Technologies Like 32nm, 28nm Etc. The 8 Bit Multiplier Technique Was Used To Develop For 16 Bit, 32 Bit, And 64 Bit Multipliers Etc. This Project Can Also Be Developed Using Fin-FET, CNT-FET Technologies Which Are Still In Research.

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