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Design of a Low Power and High Speed 512-Bit Shift Register Using Static Differential Sense Amplifier Shared Pulsed Latch Circuit

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Abstract:*Flip-flops and latches are the most considerable storage elements used in many VLSI circuits. They are gaining more importance in designing shift register, which has many applications now a days. In this paper, shift register is implemented using PULSED LATCH circuit. The pulsed latch circuit is driven by the pulsed clock signal, generated by the pulse generation circuit. By using the pulsed clock signal, clock power is very much reduced, thereby reducing the overall power consumption. Among different pulsed latch circuits like Modified Hybrid Latch Flip-Flop (MHLFF) and Transmission Gate Pulsed Latch (TGPL), the Static Differential Sense Amplifier Shared Pulsed Latch(SSASPL) which has low power and less delay is chosen to design 512-bit shift register in TANNER EDA tool using 180nm technology.*

Index Terms*-Pulsed latch, flip-flop, shift register.*

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I. Introduction

Low power VLSI has gaining much importance now-a-days.Flip-flops and latches are the important sequential elements used in many VLSI circuits and mainly used in shift registers, microprocessors, microcontrollers and also has its applications in image processing.Flip-flops and latches are the 1-bit storage elements used in many processors. The main difference between flip-flop and latch is that, the flip-flop is edge-triggered and latch is level-triggered.

The master-slave flip-flop is designed using two latches driven by the opposite clock edges. The reason for using two latches is to stop the race-around condition occurring in the JK-flip-flop. The race-around condition occurs when J=K=1 and when long clock pulse occurs, the output at this state is toggling. To avoid this, one solution is to drive another latch by giving opposite clock pulse which is named as master-slave flip-flop. By doing this, the race around condition is eliminated completely, but the drawback is that the area is very much increased by using two latches thereby increasing the overall powerconsumption.

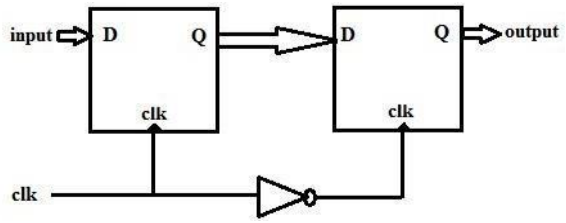

Fig.1 Master-slaveflip-flop.

Another solution for eliminating the toggling effect is by using pulsed latch circuit. The pulsed latch circuit consists of only one latch driven by pulsed clock signal, generated by the pulse generation circuit. By using the pulsed latch circuit which uses only one latch,the area which is the drawback in the case of the master slave flip-flop which uses two latches with opposite clock signal is eliminated. And also by using the pulsed clock signal the clock overhead is very much reduced thereby reducing the overall power consumption.

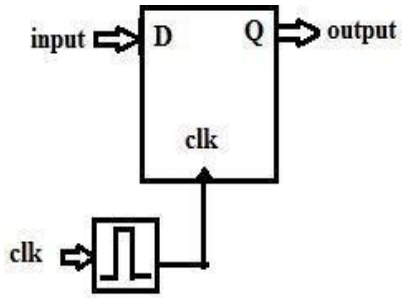

Fig.2 Pulsed latch circuit

In this article we are presenting comparative analysis of different types of pulsed latches like Modified Hybrid Latch Flip-Fop (HLFF), Transmission Gate Pulsed Latch (TGPL) and Static Differential Sense Amplifier Shared Pulsed Latch(SSASPL) with respective to power, delay and power-delay product and among them the SSASPL which has low power and less delay is used in designing 512-bit shift register. The paper is organized as follows, section II discusses about different design approaches for pulsed latch circuit and their simulation results. Section III discusses the comparative analysis of different pulsed latch circuits. Section IV discusses the design of 512-bit shift register using Static Differential Sense Amplifier Shared Pulsed Latch. Section V gives theconclusion.

II. Different Pulsed LatchedCircuits

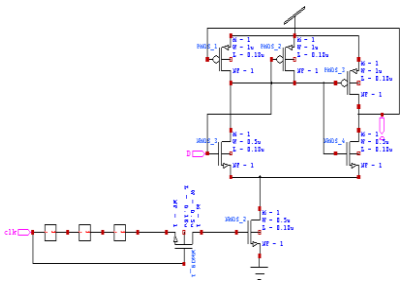

Fig.3MHLFF

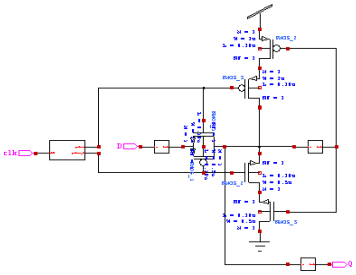

Fig.4TGPL

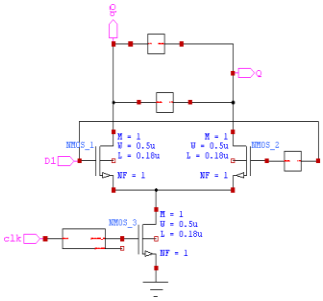

Fig.5SSASPL

SudhaKousalya and G.V.R.Sagar has proposed Modified Hybrid Latch Flip-Flop(HLFF) [4]. This is one of the pulsed latch circuitand the pulse generation circuit used in this MHLFF consists of inverters and the pass-transistor as shown in above Fig.3. The Modified Hybrid Latch Flip-Flop has very simple circuitry with less no. of transistor count and with simple pulse generation circuit. The MHLFF has small discharge path by only through two transistors (N2-N3).The power consumption of the MHLFF is obtained as 175.23uw and the delay is obtained as52ns.

Wael M. Elsharkasy has proposed Transmission Gate Pulsed Latch (TGPL) [1] shown in Fig.4. The pass transistor logic used in the MHLFF, does not provide full swing due to its circuit behavior, so it is replaced by the transmission gate in the TGPL.The power consumption of the TGPL is obatined as 4uw and delay as 57ns. The delay is little high in the case of TGPL, when compared with the MHLFF is due to its high clock load. In TGPL circuit, four transistors are driven by the pulsed clock signal generated by the pulse generation circuit, so the clock load is little higher than the MHLFF, thereby increasing the delay of thecircuit.

Byung-Do Yang has proposed Static Differential Sense Amplifier Shared Pulsed Latch (SSASPL) [2] shown in Fig.5. The drawback of both MHLFF and TGPL circuits is that, they have high delay due to its large discharge path and high clock load. These drawback can be overcome using Static Differential Sense Amplifier Shared Pulsed Latch with very low power consumption. The SSASPL circuit is designed with less transistor count and also with simple pulse generation circuit. The operation of the SSASPL circuit is also very simple when compared with other pulsed latch circuits. When clk=1, D1=0, the n-mos transistor is on, N1 transistor is off and N2 transistor is on, the Q discharges the output to ground and obtained as Q=0, when D1=1, N1 transistor is on and N2 transistor is off then Q_b discharges to ground so Q_b=0 and Q=1.The power consumption for SSASPL is obtained as 1.98uw and delay as 51ns. The power consumption, area and delayare

very much reduced when compared with the other pulsed latch circuits like MHLFF and TGPL. The SSASPL uses pulse generation circuit to generate pulsed clock signal as shown in below Fig.6. The pulse generation circuit consists of delay unit, NOT gate, AND gate and a buffer.

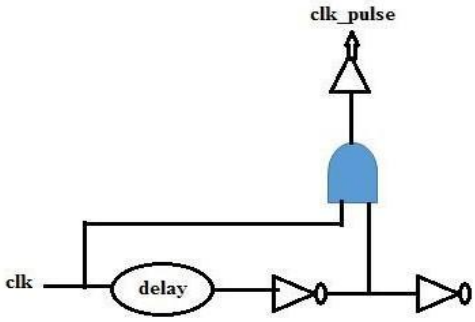

Fig.6 Pulse Generation Circuit

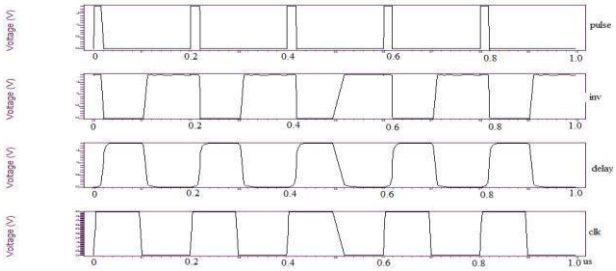

Fig.7 Simulation result of Pulse Generation circuit

Fig.8 Simulation result of MHLFF

The latch operation is like whenever the clock is low, the output remains in the previous state and when clock is high whatever the data input is given is obtained at the output,which is shown in above figure. For this MHLFF, as shown in Fig.8, clock time period is taken as 100ns and pulse width is taken as 50ns. In this we considered ten clock pulses in 1us time period. The data pattern is taken as D=10101010 with a time period as 200ns and pulse width of 95ns and the output sequence is obtained as Q=10101010. The rise and fall time are taken as 5ns. The supply voltage is taken as Vdd=1.8v.

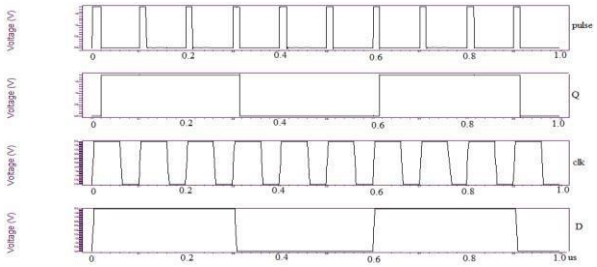

Fig.9 Simulation result of TGPL

Whenever the pulsed_clock is low, the output remains in the previous state and when pulsed_clock is high whatever the data input is given is obtained at the output For the TGPL, as shown in Fig.9, clock time period is taken as 100ns and pulse width is taken as 50ns. Similarly in this TGPL, ten clock pulses are taken in 1us time period. The data pattern is taken as D=111000111 with a time period as 600ns and pulse width of 300ns and output sequence is obtained as Q=111000111. The rise and fall time are taken as 5ns. The supply voltage is taken asVdd=1.8v.

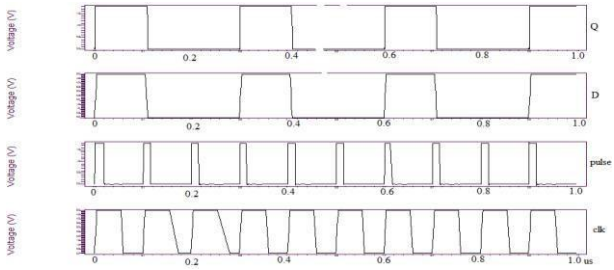

Fig.10 Simulation result of SSASPL

For the SSASPL,asshown in above Fig.10, clock time period is taken as 100ns and pulse width is taken as 50ns. In this also we considered ten clock pulses in 1us time period. The data pattern is taken as D=100100100 with a time period as 300ns and pulse width of 100ns and obtained output sequence Q=100100100. Theriseandfall timearetakenas5ns. ThesupplyvoltageistakenasVdd=1.8v.

III. Comparative Analysis Of Different PulsedLatches

In the below two tables, the power and delay results of all pulsed latch circuits like Modified Hybrid Latch Flip-Flop (MHLFF), Transmission Gate Pulsed Latch (TGPL) and Static Differential Sense Amplifier Shared Pulsed Latch (SSASPL) are compared and analyzed that the Static Differential Sense Amplifier Shared Pulsed Latch has low power consumption and less delay. For all pulsed latch circuits the power consumption mainly depends on the clock power. In this SSASPL, due to the pulsed clock signal which is generated by the pulse generation circuit, the clock power is very much reduced and also reducing the overall power consumption. The SSASPL also has less delay and low area consumption due to its circuit behavior and less transistorcount.

Table.1 Power consumption ofdifferentlatches

PULSED-LATCH	POWER (us)
MHLFF	175.23
TGPL	4.81
SSASPL	1.98

Table.2 Delay comparison of differentlatches

PULSED-LATCH	DELAY (ns)
MHLFF	52
TGPL	57
SSASPL	51

IV. Design Of512-Bit Shift Register Using Static Differential Sense Amplifier Shared Pulsed Latch

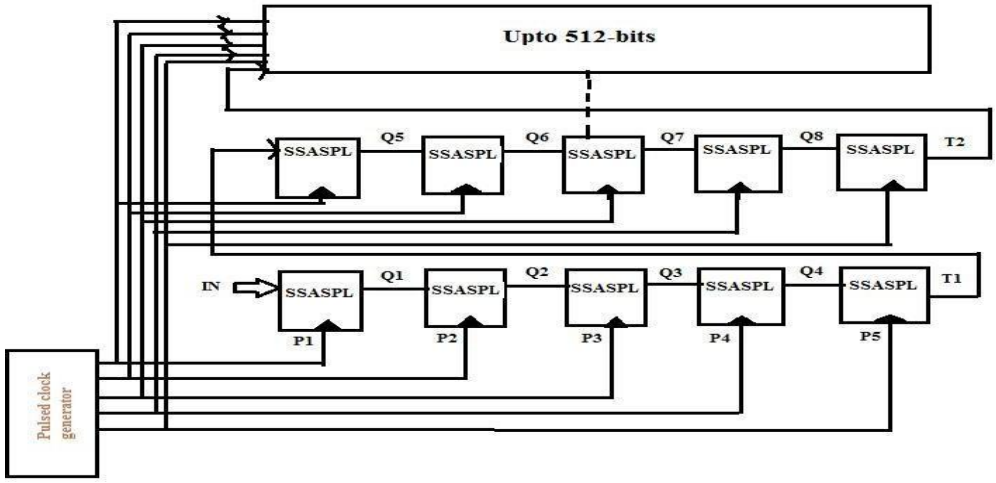

Fig.11 512-bit SSASPL shift register

The static differential sense amplifier shared pulsed latch circuit is used in designing 256-bit and 512-bit shift register due to its advantages of low power, less delay and less transistor count. The SSASPL shift register also consumes less power due to its register implementation as shown in above figure.The above register is implemented using parallel implementation. Due to this parallel implementation, the power and delay are very much reduced.The pulsed clock generator shown in above figure, generates delayed pulsed clock signals which reduces the timing violations like set up time and hold time violations. Each delayed pulsed clock signal is given to the all latches in one row and one extra latch is added at each row to store the temporary data which is given as input to the next stage. And the same process is repeated to the next row of latches with the same delayed puled clocksignals.

As shown in above Fig.10, the shift register operation is that, it shifts the data from one latch to the other latch according to the pulsed clock signal i.e, the output of one latch is given as input to the next latch. This process continues till the last 256-bit and for 512-bit shift register according to the different delayed pulsed clock signal. For all latches we are using the same five delayed pulsed clock signals simultaneously, so the clock overhead is reduced than any other shift registerimplementation.

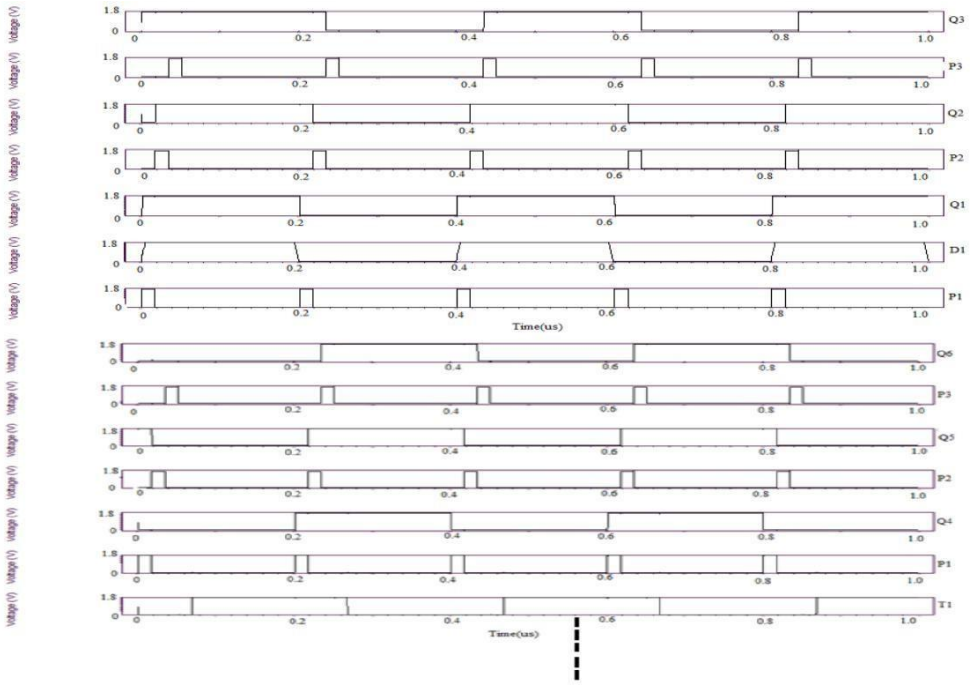

Fig.12 Simulated waveforms of 512-bit SSASPL shift register

Since the static differential sense amplifier shared pulsed latch is the best pulsed latch circuit of all pulsed latches, so it is used in designing shift register.When the clock is high whatever the input is present that is obtained at the output and when clock is low the output remains in the previous state. The output of one latchi.e Q1 is given as input to the other latchand according to the pulse P2, the output Q3 is obtained and this process continues up to 256-bits and the shift register is designed.Table.3 gives the performance comparison like power and delay of both 256-bit and 512-bit shift register.

Table.3 Performance comparison of shift register

Bits	Power (mw)	Delay (us)
256-bit	1.103	11.16
512-bit	2.512	24.32

V. Conclusion

The Static Differential Sense Amplifier Shared Pulsed Latch (SSASPL)is compared with other pulsed-latches like Modified Hybrid Latch Flip-Flop (MHLFF) and Transmission Gate Pulsed Latch (TGPL), among them SSASPL has low power consumption, low area consumption and also less delay. So this SSASPL is used in designing of256-bit and 512-bit shift register.The simulation results are obtained using 180nm technology with length of 0.18u and width of 0.5u. The same technology, same length and width are taken for all pulsed latch circuits and also for designing 256-bit and 512-bit shiftregister.

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