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Design of Energy Efficient and Size Reduced Scram Cell

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Abstract : *Semiconductor memories are a vital component of essentially any state of the art digital circuits. One among them is the Static Random Access Memory (SRAM). The dynamic power consumption contributes to about 80% of the total power consumption. In this paper a novel 4T asymmetric SRAM Cell is proposed which has reduced the dynamic power consumption by 98.58% and area occupied by 30.86% when compared to one of the existing 4T SRAM Cells. This cell is designed using 45nm technology.*

Keywords - *45nm technology, 4T SRAM cell, Reduced area occupancy, Dynamic power consumption, Semiconductor memories.*

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I. Introduction

The electronic revolution has had a profound impact on the day to day lives of the people across the world. Continuous research in this field has resulted in electronic circuits and devices with greater capabilities, better efficiency, more reliability and lesser cost.

The more we try to improve upon various parameters that govern the circuit's performance, the more are the challenges that we face. One of these challenges is the power requirement of the devices.

The power dissipation should be kept as low as possible for two main reasons. First, in the case of portable electronic devices that operate on the battery, low power consumption would mean longer battery life. Second, more power consumption directly implies more heat dissipation; and such increase in the circuit's temperature could put its performance into jeopardy.

There could be several approaches or means through which we could tackle the problem of power [1].

1. Scaling the supply voltage.
2. Redesigning the circuit which would inherently consume lesser power.
3. Using power management strategies.
4. Reducing the chip and package capacitance.

Using the above approaches, several researchers have come up with power reduction strategies which are listed below [2].

1. Clock Gating
2. Multi-threshold optimization
3. Dual Vdd
4. Clustered Voltage Scaling
5. Multi-Voltage optimization
6. Dynamic Voltage and Frequency Scaling
7. Adaptive Voltage Scaling

Area occupied by the cell is also an important parameter to be considered as reducing the area would help accommodate more SRAM cells in the same area which would in turn increase the memory capacity[5][6]. In this paper, we have focused on optimizing the dynamic power consumption and area occupied by an SRAM cell.

II. Proposed Design

Earlier it was stated that we aim to reduce the power consumption and the area occupied by the cell, but using power reduction strategies that involve additional circuitry to cut down on the power would invariably end up increasing the surface area of the overall cell. Thus we have used the approach of "employing a better circuit design" to create an SRAM cell that inherently consumes less power.

Unlike the conventional 6 transistor (6T) SRAM, our design uses 4 transistors only; i.e. 4T SRAM. The proposed design is as shown in the Fig 1.

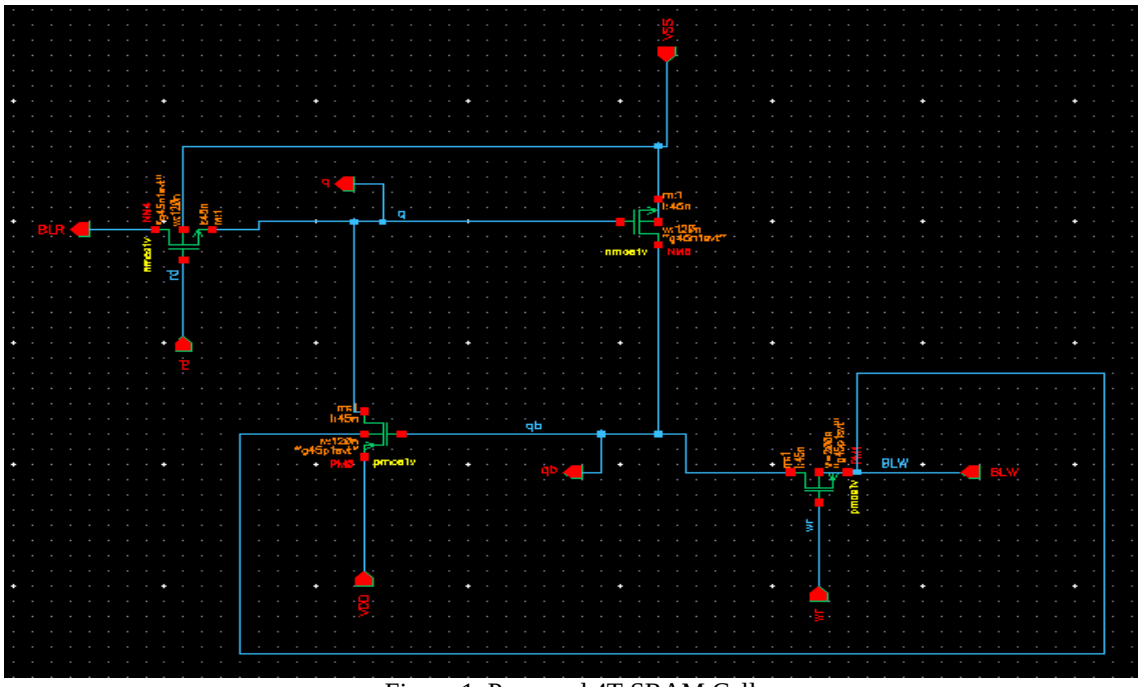


Figure 1. Proposed 4T SRAM Cell

Consider the arrangement of the transistors in Fig 1. It uses 2 NMOS and 2 PMOS transistors. Transistors PM1 and NM4 act as write access transistor and read access transistor respectively. While transistors NM0 and PM0 act as a data hold circuit. Here the pin VDD is connected to the positive power supply (1V) and the pin VSS is connected to the power supply of 0V.The operations of this cell are described below.

1. Hold States

Hold State '1' **:** Assuming zero initial condition of the circuit, it is clear that the potential at the source terminal of the PMOS transistor PM0 is at a higher potential than its gate terminal. This causes it to turn ON and allows the positive voltage to appear at its drain terminal as per the concept of pass transistor logic. This drain terminal of the PM0 which is connected to the gate of the NM0 is at a higher potential than its source which turns it ON allowing the negative voltage to appear at its drain terminal which in turn is fed back to the gate of the PM0. This creates a loop thereby holding logic '1' at the 'q' terminal.

Hold state '0'**:** This is achieved by using a technique proposed by Adam Teman [3] *et al.* in their paper "A 40 nm Sub-Threshold 5T SRAM Bit Cell with Improved Read and Write Stability". In their circuit, the bit line BLb had to be held low (logic '0') continuously for storing/holding the logic '1'. This is also observed in the paper proposed by Puna Kumar Rajak[4] *et al.* In our circuit, we hold the bit line or BLW signal high (logic '1') continuously to store/hold logic '0' at 'q'. According to the technique proposed by Adam Teman even though the write access transistor turns off after the end of write pulse, due to the effect of leakage current, the influence of the voltage at BLW is felt at the gate of the transistor PM0. This ensures that the PM0 turns OFF thereby cutting off the positive power supply to the terminal 'q'. Hence logic '0' is successfully stored.

2. Write Operation

In our design, the data bits will have to be given in their complemented form. The waveform for the write operation is shown in Fig 2.

Write '1'**:** For writing '1' to the cell, we give a logic '0' pulse to the BLW line. This will turn ON the PM0 thus 'q' gets fixed to logic '1'.

Write '0'**:** For writing '0' to the cell, we give a logic '1' pulse to the BLW line and continue to hold the BLW line at logic '1' for reasons as stated earlier in the Hold state '0'.

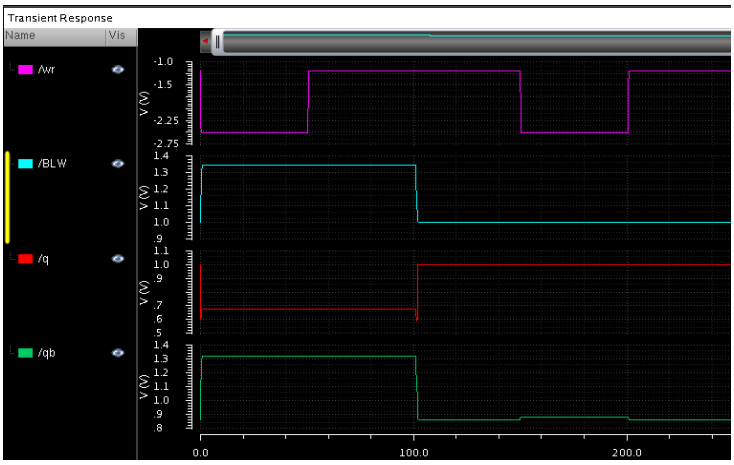
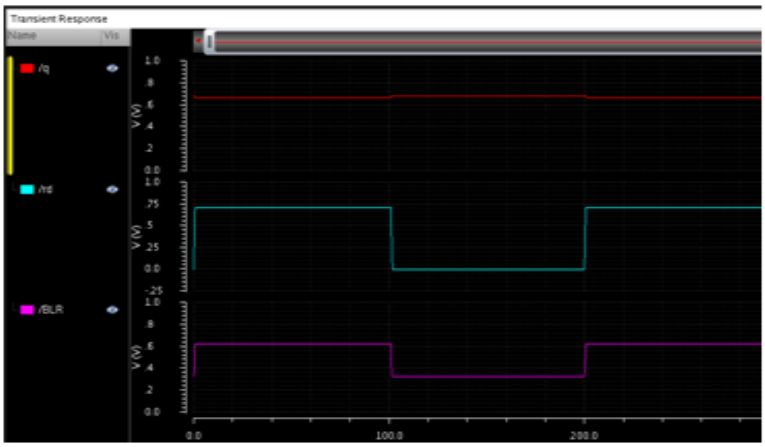


Figure 2. Waveforms for Wite Operation

3. Read Operation

Reading the logic level stored at 'q' can be done by asserting a read signal RD, which is connected to the gate of the NMOS transistor "NM4". When the read signal is asserted, the voltage levels get transferred from 'q' to the bit line BLR. This BLR is in turn connected to the Sense Amplifier which gives the final read out of the data stored in the SRAM cell. The waveforms for the read operations i.e., read'0' and read '1' is as shown in Fig 3 and Fig 4 respectively.

Figure 3. Waveforms for Read Operations '0'



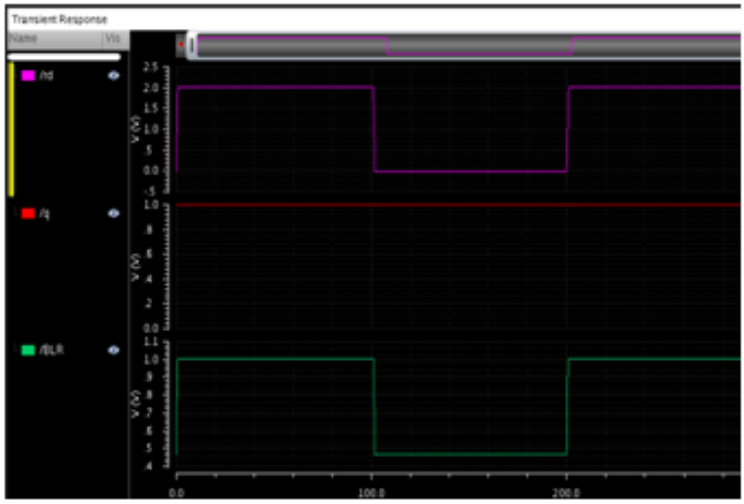


Figure 4. Waveforms for Reading '1'

The layout diagram for the proposed 4T SRAM Cell is shown in the Fig 5.

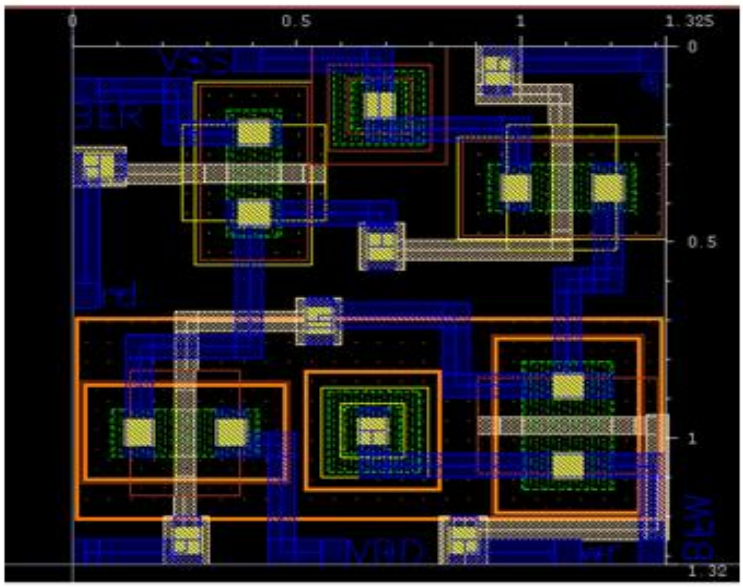


Figure 5. Layout diagram of the proposed 4T SRAM Cell

III. Results and Discussions

The proposed 4T SRAM cell is dealt on the characteristics of reduced number of transistor count, area and the power. The values tabulated of the area and power dissipated is observed in 45nm technology using the Cadence tool. Cadence tool helps us to design the circuit and verify its working. It offers various tools to meet and improve the performance of the circuit and also to reduce the power consumption. In this design we are dealing with the reduced power and area. Power is broadly classified into 3 major categories i.e. Dynamic power, Short circuit power and Static power. We have dealt with the reduction in dynamic (active) power. As later on observed in the tabulated values there is considerable reduction in the active power. The aspect ratio of the 3 transistors i.e., read access transistor (NM4), data hold transistors NM0 and PM0 is kept constant to 120nm/45nm and the write access transistor (PM1) has a value of 200nm/45nm. Fig 6 shows the instantaneous power consumed by all the transistors. The power spikes seen in the waveform represents the dynamic power consumption.

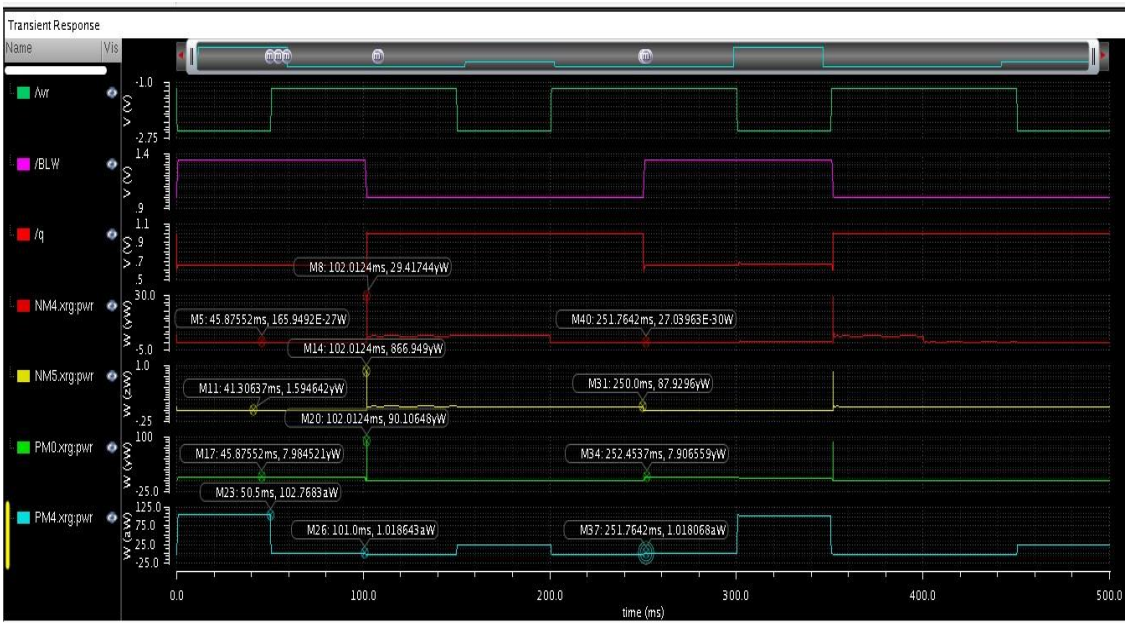


Figure 6. Waveforms for instantaneous power.

Table 1 shows the values obtained for Dynamic Power Consumption and Area occupied by the proposed 4T SRAM and the existing 4T SRAM [4].

Table 1. Comparison Table

PARAMETERS	EXISTING 4T SRAM[4]	PROPOSED 4T SRAM
POWER	7.180fW	0.102fW
AREA	2.530um^2	1.749um^2

IV. Conclusion

With the objective of achieving reduction in dynamic power consumption and area occupied, it is seen that the proposed 4T SRAM cell has 98.58% lesser dynamic power consumption and 30.86% lesser area occupancy compared to the already existing 4T SRAM cell. One of the limitations of this SRAM could be that, if the sense amplifier is not sensitive enough to discriminate the voltage levels of the order of millivolts, then there could be a possible discrepancy in the read operation. This work may further be extended by considering the delay aspect which focuses on minimizing the time required to perform the read and write operation.

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