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Performance Analysis of Fixed Width Multiplier using Baugh Wooley Algorithm

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Abstract : *This paper presents Fixed Width Baugh Wooley Multiplier which are widely used in digital signal processing (DSP) applications such as finite impulse response filter(FIR),fast Fourier transform(FFT) and discrete cosine transform (DCT).For realization of 2's complement multiplication operation Baugh-Wooley algorithm is used. Various optimization methods are applied to the multiplier design and the performance has been evaluated on the basis of area & delay analysis. Power Delay product analysis between proposed & reported multipliers has been performed. To verify the functionality of the design simulation has been done.*

Keywords - *Baugh –Wooley algorithm, Fixed Width Multiplier, Parallel Prefix Adder, Power Delay product.*

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I. Introduction

Multipliers play a pivotal role in many high performance systems such as Digital processors, FIR filters and multimedia. It dominates the chip power consumption and operation speed. Reduction in number of multiplication products avoids infinite growth of multiplication bit width [1]. Most of the DSP application require efficient and low-error fixed width multipliers, in which by directly truncating n bit LSB output of a fixed width multiplier is achieved ,that produces n-bit output product with n-bit multiplier and n-bit multiplicand. Truncation of LSB part cause to large truncation errors. To reduce truncation error many error compensation techniques have been presented. Compensation with constant correction [2]-[3] and compensation with variable correction value [4]-[10] these are the methods used to design error compensation circuit with less truncation error.

Complexity of the circuit to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches usually can be more precise. Literature [4] proposed and analyzed three methods simple fixed bias correction, partial product conditional correction, and time invariant multiplicand for producing sufficiently accurate estimate of the least significant part. In [5] error compensation value is generated by sum of most significant column of truncated part. By properly choosing the generalized index in [6] reduce the truncation error by deriving the better error-compensation bias and then construct a lower error fixed-width multiplier, which is area efficient for VLSI implementation. Variable correction methods [7-13] are employed that compensate the effect of the eliminated terms with non constant compensation function which is used to estimate the weighted sum of LSB part and to reduce the output error. Digital signal processor requires efficient and low error fixed width multiplier in terms of power consumption, both static and dynamic [14-18]. Therefore, instead of targeting them independently, there is a need to find an optimum between speed and power. This is represented by the average energy dissipated for one switching event which is known as power-delay product.

This paper presents a novel approach for performance evaluation of Fixed Width Multiplier using Baugh Wooley algorithm which is carried out on the basis of speed and power–delay product. The architectural details & performance evaluation results for proposed & reported multipliers [9] are presented.

II. Baugh Wooley Algorithm

The Baugh –Wooley multiplication algorithm is an efficient way to handle the sign bits. This technique has been developed in order to design regular multipliers, suited for 2's–complement numbers. Let us consider two n-bit numbers, P and Q to be multiplied, P and Q can be represented as

$$P = -p_{n-1}2^{n-1} + \sum_{i=0}^{n-2} p_i 2^i \tag{1}$$

$$Q = -q_{n-1}2^{n-1} + \sum_{j=0}^{n-2} q_j 2^j \quad (2)$$

Where the p_i 's and q_i 's the bits in P and Q, respectively, and p_{n-1} and q_{n-1} are the sign bits. The product, R=P×Q, is then given by following equation:

$$\begin{aligned} R &= P \times Q \\ &= \left(-p_{n-1}2^{n-1} + \sum_{i=0}^{n-2} p_i 2^i\right) \times \left(-q_{n-1}2^{n-1} + \sum_{j=0}^{n-2} q_j 2^j\right) \\ &= p_{n-1}q_{n-1}2^{2n-1} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} p_i q_j 2^{i+j} - 2^{n-1}\sum_{i=0}^{n-2} p_i q_{n-1} 2^i - 2^{n-1}\sum_{j=0}^{n-2} p_{n-1} q_j 2^j \end{aligned} \quad (3)$$

Equation (3) indicates the final product is obtained by subtracting the last two positive terms from the first two terms. Rather than do subtraction operation, we can obtain the 2's complement of the last two terms from the first two terms.

The last two terms are n-1 bits in which each that extend in binary weight from position 2^{n-1} up to 2^{2n-3}. On the other hand, the final product is 2n bits and extends in binary weight from 2^0 up to 2^{2n-1}.

At first pad each of the last two terms in the product P equation with zeros to obtain a 2n-bit number to be able to add it with the other terms. Then the padded terms extend in binary weight from 2^0 up to 2^{2n-1} [3].

Let X is one of the last two terms that can represent it with zero padding as

$$X = -0 \times 2^{2n-1} + 0 \times 2^{2n-2} + 2^{n-1}\sum_{i=0}^{n-2} p_i 2^i + \sum_{i=0}^{n-2} 0 \times 2^j \quad (4)$$

The final product R=P×Q in equation (3) becomes:

$$R = p_{n-1}q_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} p_i q_j 2^{i+j} + 2^{n-1}\sum_{i=0}^{n-2} \overline{q_{n-1}p_i}\, 2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{p_{n-1}q_j}\, 2^j - 2^{2n-1} + 2^n \quad (5)$$

III. Design of fixed width Multiplier

A. Fixed-Width Two's-Complement Multiplier

Low error area efficient fixed width two's complement multipliers [9] that receive two-bit numbers and produce a n-bit product. To design low area efficient fixed width 2's complements multiplier under different values of W, proposed error compensation bias using generalized index and then select the best index having lower error and satisfying the same value K for limited width n. Partial products for Baugh–Wooley array multiplier can be partitioned into two sections, can be rewritten as

$$P_{S\tan dared} = MP + LP = \sum_{i=0}^{2n-1} P_i 2^i$$

Where, MP is the most significant columns, and LP is the least significant columns as shown in shaded portion of Fig.1.

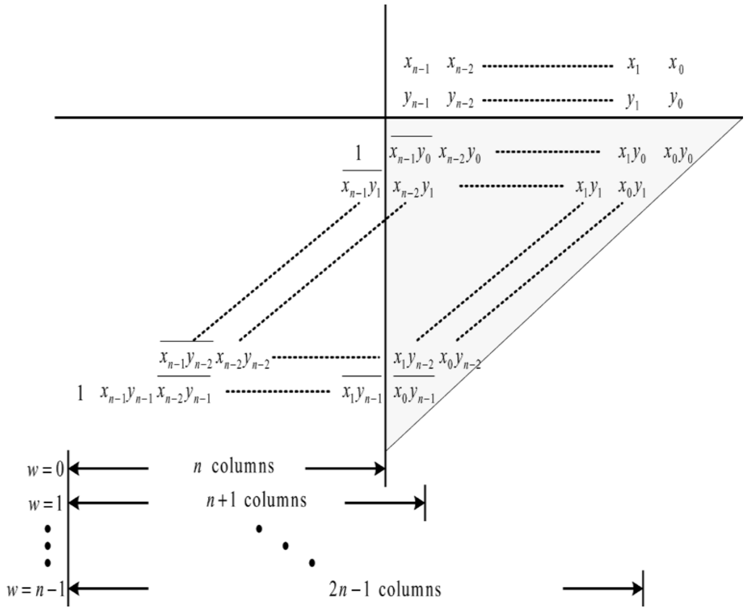

Fig. 1: n-bit multiplication Partial product array

Fixed width low error 8×8 two's complement multipliers with $\theta_{Q=0,\ W=1}$, $\theta_{Q=0,\ W=2}$ has been designed using various logic diagrams & simulated using Xilinx. Device utilization Summary is shown in Table 1 &2.

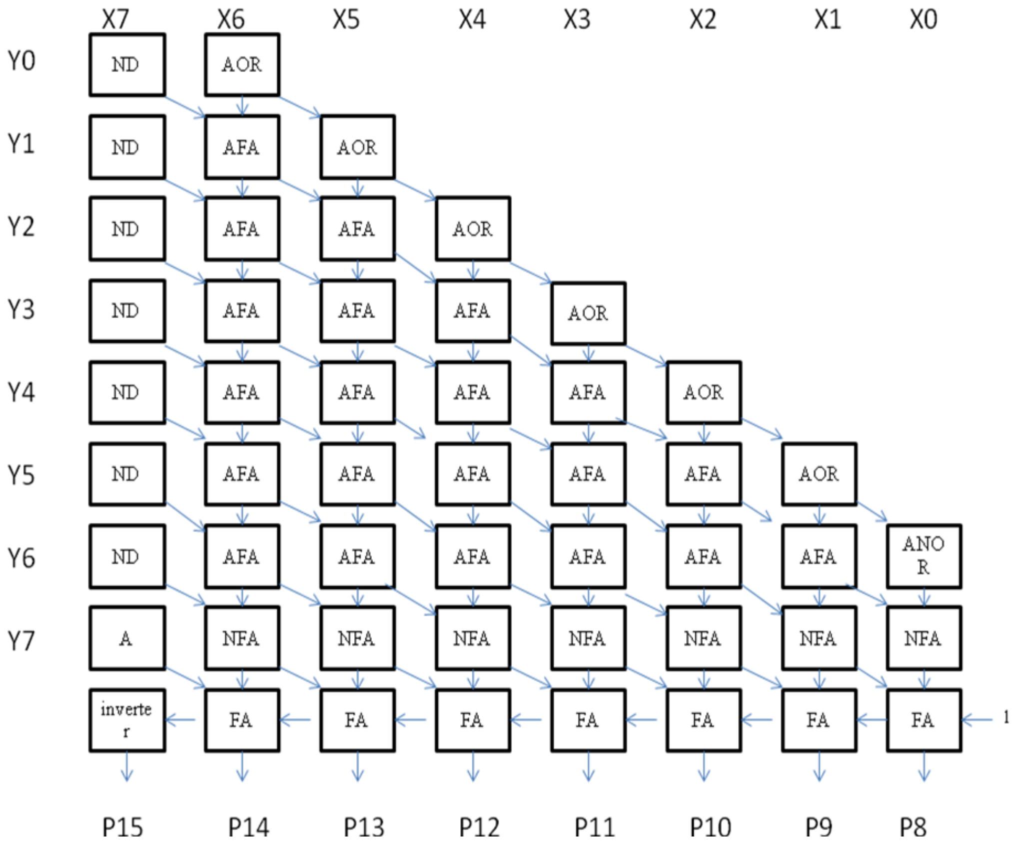

Fig. 2. (a) Design low-error fixed-width 8 × 8 two's-complement multiplier with $\theta_{Q=0}$, W=1

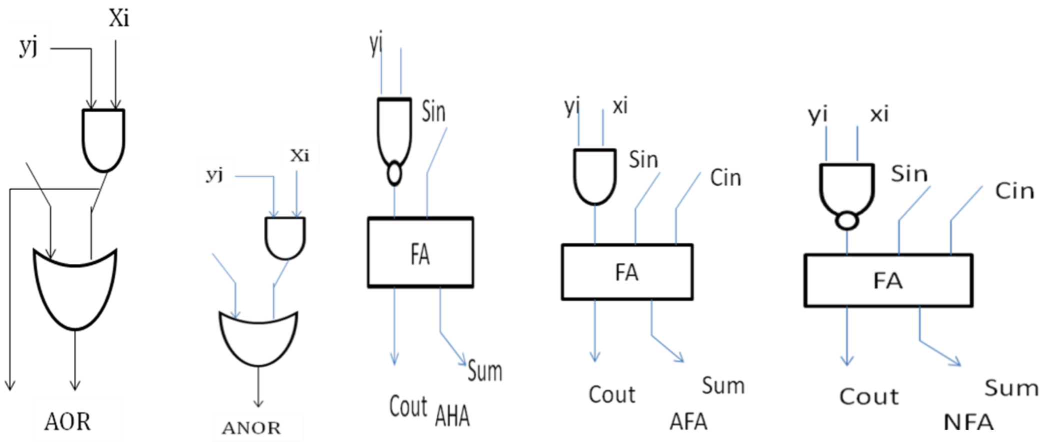

Fig. 2. (b) Logic diagrams of AOR, ANOR, AHA, AFA, and NFA.

Table 1. Device utilization summary

Logic Utilization	**Used**
Number of Slice LUTs	54
Number of Occupied Slices	32
Number of bonded IOBs	24
Maximum combinational path delay	13.005ns

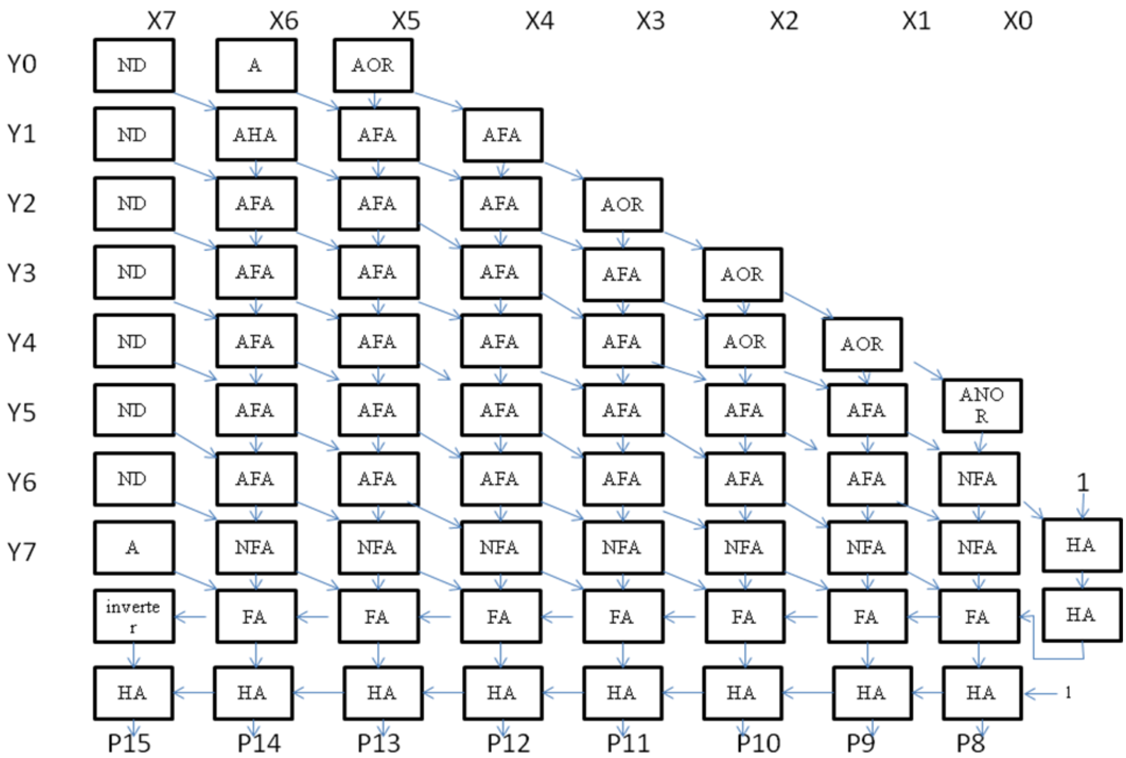

Fig. 3. (a) Design low-error fixed-width 8 × 8 two's-complement multiplier with $\theta_{Q=0}$, $_{W=2.}$

Table 2:-Device utilization summary

Logic Utilization	**Used**
Number of Slice LUTs	76
Number of Occupied Slices	37
Number of bonded IOBs	24
Maximum combinational path delay	14.706ns

B. Proposed Fixed Width Multiplier Design

Design fixed width multiplier with **a** new approach that uses three multiplication units and parallel adders, which improve the speed and power-delay product. Comparative analysis has been carried out in terms of delay reduction, area with pervious designs.

							1	$\overline{X_7Y_0}$	x6y0
							$\overline{X_7Y_1}$	x6y1	x5y1
						$\overline{X_7Y_2}$	x6y2	x5y2	x4y2
					$\overline{X_7Y_3}$	x6y3	x5y3	x4y3	X3y3
				$\overline{X_7Y_4}$	x6y4	x5y4	x4y4	x3y4	x2y4
			$\overline{X_7Y_5}$	x6y5	x5y5	x4y5	x3y5	x2y5	x1y5
		$\overline{X_7Y_6}$	x6y6	x5y6	x4y6	x3y6	x2y6	x1y6	x0y6
1	$\overline{X_7Y_7}$	x6y7	x5y7	x4y7	x3y7	x2y7	x1y7	x0y7	
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6

Multiplier output Truncated bits

Fig.4(a). Partial Product Array for n=8

This partial products array is decayed into three multiplication units which are denoted by MU1, MU2 and MU3. The building blocks for MU1, MU2, and MU3 are further shown in fig.4 (b), fig. 4(c), fig. 4(d) respectively. And these multiplication units are designed has been designed using various logic Gate & diagrams like ND, A, FA, AFA, AOR, NFA, and Inverter respectively. The design structure of these multiplication units are as follows. The three multiplication units can takes less delay to get the output product.

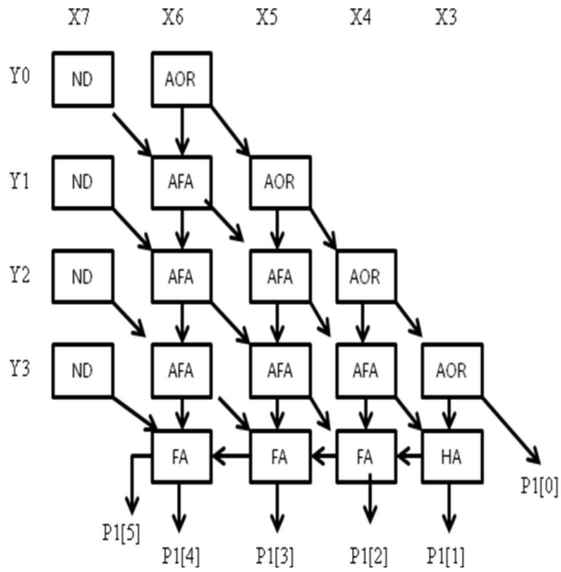

Fig 4(b) Architecture for MU1

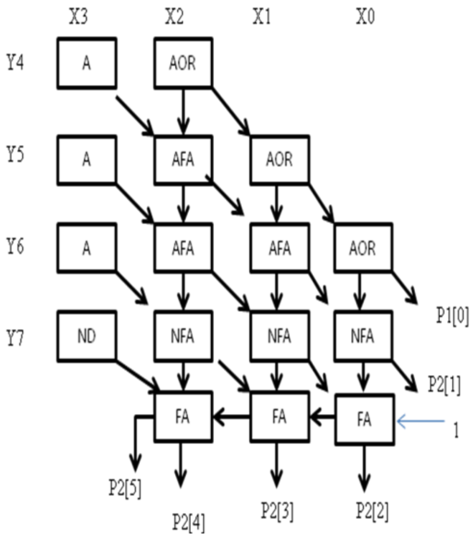

Fig 4(c) Architecture for MU2

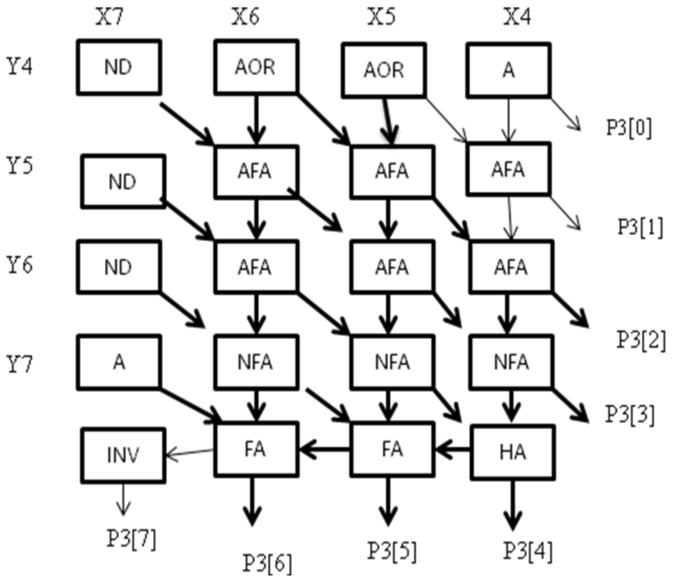

Fig 4(d) Architecture for MU3

The multiplication units MU1, MU2 and MU3 are designed using Baugh-Wooley array algorithm. For MP1 module the inputs are x[7:3] and y[3:0] generates partial products output as P1[5:0]. For MP2 module the inputs are x[3:0] & y[7:4] generates partial product output as p2[5:0].Similarly For MP3 module the inputs are x[7:4] & y[7:4] generates partial product output as p3[7:0]. These outputs are generated independently by using MU1, MU2 and MU3 which can improve the speed of the design. Final summation of partial product outputs of three multiplication units MU1, MU2 and MU3 are as shown in Fig 5.

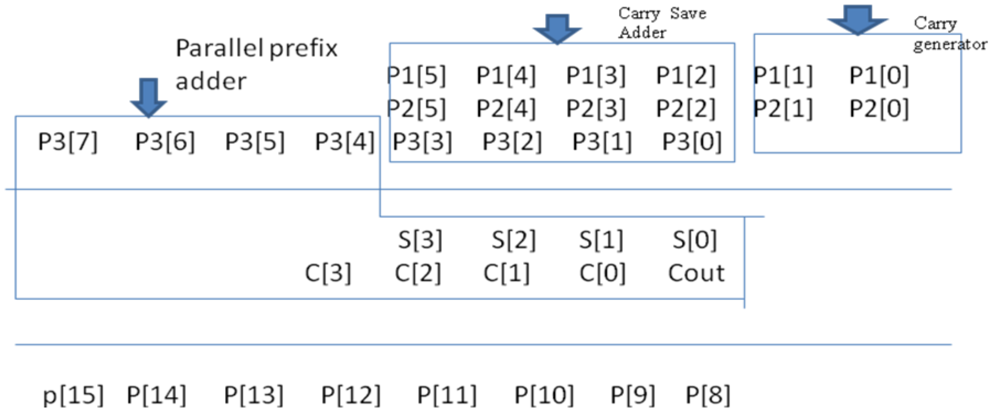

Fig.5 Partial product summation using carry save adder and parallel prefix adder

Carry generator circuit generate carry Cout using partial product bits P1 [1:0], P2 [1:0] which generate partial products P [6] & P [7].Only carry generated has propagated to next level because P[6] & P[7] product bits are truncated. Design of Carry generator circuit is shown in Fig 6. For summation of P1[5:2] ,P2[5:2] and P3[3:0] partial products carry save adder are used which generates sum bits S[3:0] along with carry bits C[3:0].For final summation of carry Cout generated by carry generator circuit and partial product bits P3[7:4] parallel prefix Kogge_stone adder is used. Final product bits P [15:7] of fixed width multiplier are generated. RTL schematic of Baugh Wooley Multiplier is as shown in fig. 7 below.

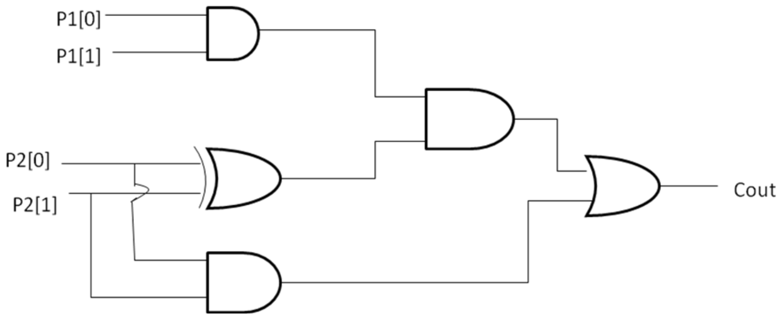

Fig.6. Carry Generator Circuit

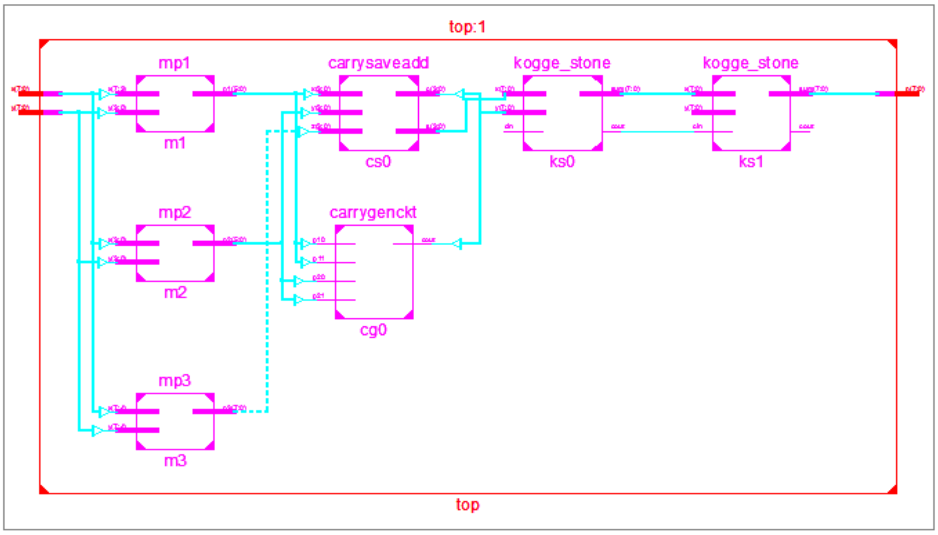

Fig.7. RTL Schematic of Fixed Width Multiplier

IV. Experimental Results

Performance Parameter Comparison analysis of Fixed-Width Two's-Complement Multipliers are summarized in theTable 3. below. Circuits are simulated using Xilinx Virtex-5 FPGA device XC5VLX110t.

TABLE 3. Performance Comparison:
PERFORMANCE PARAMETER COMPARISION [Xilinx Virtex-5 FPGA device XC5VLX110t]

N-bit	Fixed Width Multipliers	No. of Slices	No. of LUT'S	No. of bonded IOB's	delay (ns)	PDP(nJ)
		Used/Available	Used/Available	Used/Available		
8	Ref[9] W=1	32/3120	54/12,480	24/172	13.005	4.16
	Ref[9] W=2	37/3120	76/12,480	24/172	14.706	4.70
	Proposed FWM	29/3120	73/12,480	24/172	10.570	3.22

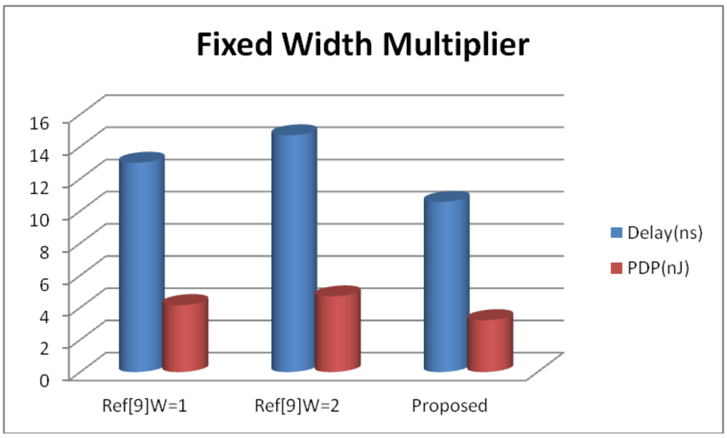

Fig.8. Comparative Analysis.

V. Conclusion

The comparative analysis and results in Fig.8 indicates that the proposed parallel fixed-width multiplier is better approach for multipliers in [9]. The design of parallel fixed-width multiplier using multiplication modules is 18.72% and 28.12% faster than the multipliers in [9]. By analyzing the data, we note that the proposed approach requires more area. Though, the power consumption of the proposed fixed width multiplier is slightly more than [9], but in terms of power delay product it improves 22.59% and 31.48% compared to [9].

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