Design and Implementation of Parking Space Detection System using Spartan FPGA

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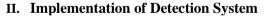
Abstract: Identification of parking space is a major time consuming process at places where the areas are fully crowded. Traffic management depends on parking space detection which will help out to clear the traffic congestion. Parking space detection system using image processing is developed and implemented. Various image processing techniques used for object recognition will be presented and its significance in vehicle detection is clarified. Smart parking lots can be designed with the proposed system along with street and highway lighting a chip or module hardware solution.

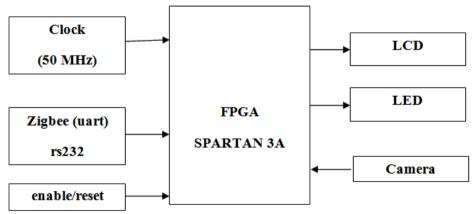
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I. Introduction

With the intention of alleviating the problems faced, systems of various functionalities have been developed. The necessity of sensors for vehicle detection has lead to the development of a variety of systems for traffic management which functions under different conditions and requirements. In the course of recognizing vehicles to determine the parking space identifying the status of the vehicles in the parking place, one of the problem that might occur include false recognition.

Image processing is a computationally intensive task which requires huge amount of computation power, especially if high resolution images are captured and used. The different vehicle models which exist would complicate the recognition process as all the variation will have to be considered in the recognition process. Occlusion would complicate the recognition process as only partial data is available for recognition. With numerous systems already developed and deployed around the world, the sensors utilized in addition to its implementation methodology are scrutinized for better understanding. Here in, the focus is directed towards the use of video image processing for vehicle detection. Image processing is well known to be computationally intensive. Therefore, the implementation of various image processing techniques in the FPGA device would also be examined. Its benefits in terms of ease of use, computation speed and aiding in relieving the burden of the central computers in a network environment would be beneficial in the system development when further explored. This is especially vital for the occupancy module to be implemented in a real time environment.





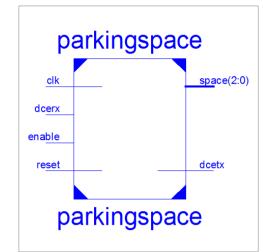


Figure 1. Proposed Parking Detection system on Spartan FPGA



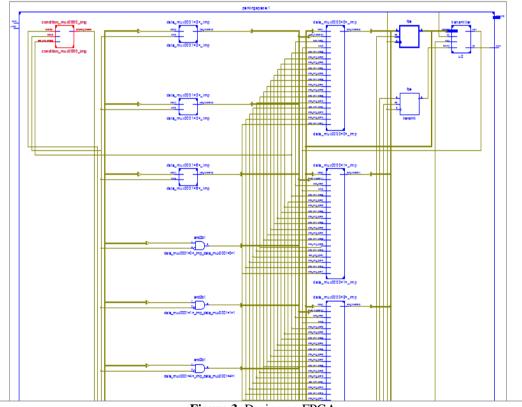


Figure 3. Design on FPGA

III. Simulation Results

Figure 4 shows that clock input is triggered for 10 ns but in FPGA implementation clock is 50 MHz. For every rising edge of the clock pulse, the module initiate transmit or receive the data. DCETX is the transmitting pin of UART. Space is the total space available for parking. RESET is applied for 20 ns to make all states to initialize position and enable is made zero for 10 ns for which module does not work.

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		0.006 ns							
Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 ns
🗓 cik	0								
🗓 dcetx	Х								
▶ 🔣 space[2:0]	XXX				XXX				
🔚 reset	1								
퉵 enable	0								
🔚 dcerx	х								



Figure 5 depicts the condition signal that the AT command for zigbee module has been transferred and module is ready to receive the reply from the module.

				4,631.667 ns						
Name	Value	4,000 ns	4,50) ns	5,000 ns	5,500 ns	6,000 ns	6,500 ns	7,000 ns	7,500 ns
🐻 clk	1									
🐻 reset	0									
🐻 enable	1									
70	0									

Figure 5 Transmitting and receiving data

														3, 158. 333 ns	
Name	Value	0 ns			500 ns	1,000 ns	 1,500 ns		2,000 n	S	2,500 ns	;	3,000	ns	3,500 ns
🐻 clk	1														
🚡 reset	0														
🚡 enable	1														
🐻 condition	0														
🕨 😽 data[7:0]	4		A	χ	T	D	9	2		4		8	Х	4	2

Figure 6. Transmitting AT command

For functioning of zigbee module an at command is being transferred and is illustrated in figure 6 and the result show the strings but ASCII value of the command is transferred an finite state machine is used to send the each ascii value as shown in Figure 7.

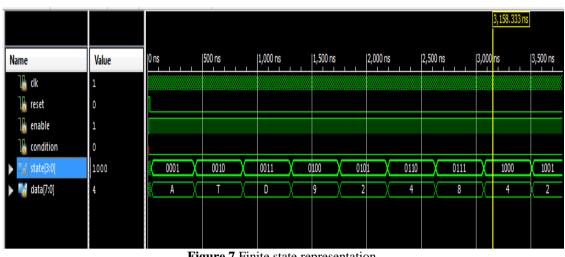


Figure 7. Finite state representation

																			3,158.333 ns		
Name	Value	0 ns			500 ns		1,00	0 ns		1,500 ns		2,000	ns		2,500	ns		3,000	ns	3,500	ns
🔓 cik	1																				
🕨 🎬 data[7:0]	00110100	01	000001	X	0101010	0 X	01000	100	001	11001	X 0011	0010	χo	011010		00	111000	DC	00110100	0011	0010
1 txd	0	Л				ЛП	Л				ΓЛ				Ш						П
1 done	0	.																			
bitcounter[3:0]	0000	CXX	00000	800	XXXXX	XXXXC	xkxx	0000	8000	XXXXX	xCXX	dooxx	XX	XXXX	XXX	CXX	XXXXX	XXX	******	x CXX	XXX
Difference in the second se	0000000000000																				
Tounter2[12:0]	0000000000000									(000000000	0000									
16 state	1												Т							11	
16 nextstate	1			Т									Г					ТГ		U –	
state_string[4:0]	00000										00000)									
Tightshiftreg[9:0]	1001101000	0000	00000	00	000000	XXXX	xkxx	0000	0000	XXXXXX	CXXX	00000	XX	XXXX	XXX	2000	XXXXX	ŝ	00000000) XXX	XXX
16 shift	1												Г								
16 load	0								Л				Л								
16 clear	0			Л							П							Л			

Figure 8. Transmitter module for UART communication

The bits are sent in a serial order with 9600 baud rate. Smart parking lots, along with street and highway lighting, can be designed with either a chip or module hardware solution. The process can be further simplified by using internet as the wireless connectivity with accurate security as the process is continuous for checking of parking spaces so self error test detection and correction methods are preferable.

IV. Conclusion

Parking space detection using Spartan FPGA is implemented and verified. Using Image processing on FPGA false recognition is eliminated and the simulation results on Xilinx are presented. Further this system can be improved by wireless connectivity. Smart parking lots can be designed with the proposed system along with street and highway lighting a chip or module hardware solution.

References

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